

4.2 An Analog Bionic Ear Processor with Zero-Crossing Detection

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Deaf patients with more than 70-80dB hearing loss cannot use a hearing aid and require a cochlear implant. The implant stimulates the auditory nerve with electrical current using 8-20 electrodes surgically implanted in the patient's cochlea. The stimulation is coded such that the logarithmic spectral energy outputs of an audio filter bank are topographically mapped to the electrode array.

For programmability, cochlear implant processing is done mostly in the digital domain by digitizing the output of a microphone front-end and feeding it to a DSP. However, the microphone front-end, A/D converter, and DSP consume a few mW of power even in power-efficient systems. In the future, an entire cochlear implant will be fully implanted inside the body of the patient and will be required to run on a 100mAh battery with at most 1000 wireless recharges and no battery replacement for at least 30 years. To achieve these specifications, a chip that implements most of the cochlear implant processing in the analog domain is presented in this paper. In this chip digitization is delayed to the very end while there is still room for 750 μ W of stimulation power. The use of analog processing to substantially reduce power in portable systems of moderate complexity appears to be an emerging technology direction [1].

Figure 4.2.6 shows a die photo of our 9.23 \times 9.58mm² chip implemented in a 1.5 μ m AMI BiCMOS process. The chip builds on and improves on some of our prior works that implemented a high PSRR microphone and microphone front end with 100 μ W power consumption [2], subthreshold micropower component circuits for a spectral channel [3, 4, 5], and a preliminary 51dB 470 μ W spectral-channel bank [6]. Several new circuits are implemented in this chip including a programmable AGC that compresses 75dB at the input into 55dB internal dynamic range (IDR) for the 16 spectral channels, a zero-crossing detection circuit that reports zero crossings in each channel with 10 μ s precision (at 10kHz) and almost no power overhead, and active fourth-order programmable bandpass filters that sharpen filter bandwidths. In addition, biasing, distribution, and calibration circuits are introduced in this chip to ensure the robust operation of the analog processor in the presence of power supply noise, temperature variations, and parameter mismatch.

The input to the chip is current from the drain of a Knowles FG3329 electret microphone and the output of the chip is a 7-bit number that represents the log spectral envelope energy of each of 16 channels with a sampling rate for each channel programmable from 500Hz to 2kHz. The output bits of the chip can be used to drive electrode DACs in a sequential fashion and implement continuous interleaved sampling (CIS), a well-known stimulation paradigm. There are 373 bits on the chip that allow adjustment of 86 parameters to maintain programmability.

Figure 4.2.1 shows the AGC circuit: Wide-linear-range transconductance amplifiers implement a VGA as a G_m -and-R configuration. The gain of the VGA is controlled by the bias current i_{Control} which modulates the transconductance of the G_m amplifier. An envelope detector with asymmetric attack and release filters [4]

detects the amplitude of the output and outputs a current i_{ED} that is converted by the translinear circuit to i_{Gain} . The maximum-gain circuit sets i_{Control} to be the minimum of i_{Gain} and i_{MAX} as described below. The translinear circuit implements an input-output function $i_{\text{Gain}} = i_{\text{SCALE}}(i_{\text{REF}}/i_{\text{ED}})^{G_1/G_2}$ such that increasing output amplitudes reduces the gain of the VGA. A DAC that alters the value of G_2 sets the compression ratio of the AGC. The i_{SCALE} DAC is set such that at a maximum output amplitude when $i_{\text{ED}} = i_{\text{REF}}$, the gain of the VGA is near 1, independent of the compression ratio. The i_{MAX} DAC determines the maximum gain of the VGA at small input amplitudes where it is typically smaller than i_{Gain} . The knee of the AGC is determined by i_{MAX} , the large-signal gain set by i_{SCALE} , and by the compression ratio. The maximum-gain circuit adapts a Wilson current mirror to take two inputs i_{MAX} and i_{Gain} and output i_{Control} as the minimum of the two input currents. The circuit works because negative feedback automatically reduces the current through M_1 and M_3 to the smaller of i_{MAX} or i_{Gain} .

Figure 4.2.2 shows the implementation of the zero-crossing detection circuit: In the Class AB envelope detector described in [4], the I_{in} current from a G_m transconductor is rectified by being switched between M_n and M_p . The voltages $V_{\text{out}}^{\text{TOP}}$ and $V_{\text{out}}^{\text{BOT}}$ are served via the amplifier A to move up and down and to turn on M_n and turn off M_p or vice versa while maintaining a two-diode voltage drop between them. By sensing the level of these two voltages in the comparator implemented by transistors M_5 , M_6 and M_7 and digitizing with the inverter implemented by M_8 and M_9 , a zero-crossing output that registers a sign change is obtained.

Figure 4.2.3 shows the frequency-response curves of the output bits of the chip on all 16 spectral channels which have been set to span the speech spectral range with even spacing in log units. The second-order roll-off on each skirt of the filter and the logarithmic A/D in each channel result in linear slopes on the input-output curves as expected. Figure 4.2.4(A) at the top shows a spectrogram output of the chip's bits in response to the phoneme /i/. The presence of two formant or dominant frequencies is clearly evident. Figure 4.2.4(B) shows that when the zero-crossing outputs of the chip are also used, a frequency sharpening algorithm can be applied such that a sharper spectral response is obtained without compromising timing resolution. The table of Fig. 4.2.5 shows the power consumption of our processor operating on a 2.8V supply with 1kHz sampling and at a Q of 4, a Q-setting that trades off spectral resolution versus timing resolution in a manner liked by patients.

References:

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- [2] M. Baker, and R. Sarpeshkar, "A Low-Power High-PSRR Current-Mode Microphone Preamplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1671-1678, 2003.
- [3] C. Salthouse, and R. Sarpeshkar, "A Practical Micropower Programmable Bandpass Filter for use in Bionic Ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63-70, 2003.
- [4] S. Zhak, M. Baker, and R. Sarpeshkar, "A Low-Power Wide Dynamic Range Envelope Detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1750-1753, 2003.
- [5] J.-J. Sit and R. Sarpeshkar, "A micropower logarithmic A/D with offset and temperature compensation," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 308-319, 2004.
- [6] M. Baker, T. Lu, C. Salthouse, J.-J. Sit, S. Zhak, and R. Sarpeshkar, "A 16-channel Analog VLSI Processor for Bionic Ears and Speech Recognition Front Ends," *Proc. IEEE CICC*, pp. 521-526, 2003.

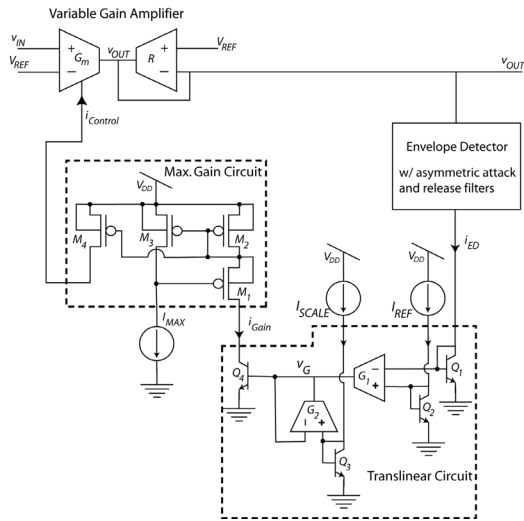


Figure 4.2.1: The AGC circuit with a programmable knee implemented by the maximum gain circuit.

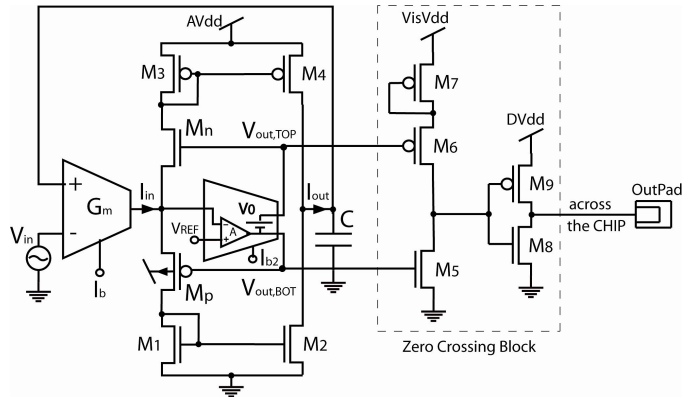


Figure 4.2.2: The circuit for zero-crossing detection.

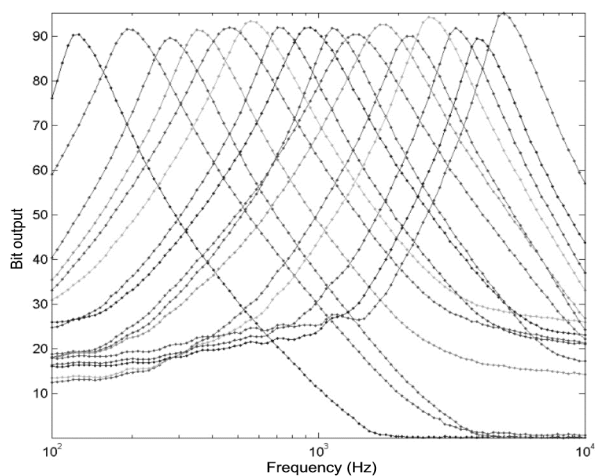


Figure 4.2.3: Bit outputs from each of the 16 channels in response to a swept sine wave, showing band-pass frequency responses with Q=4.

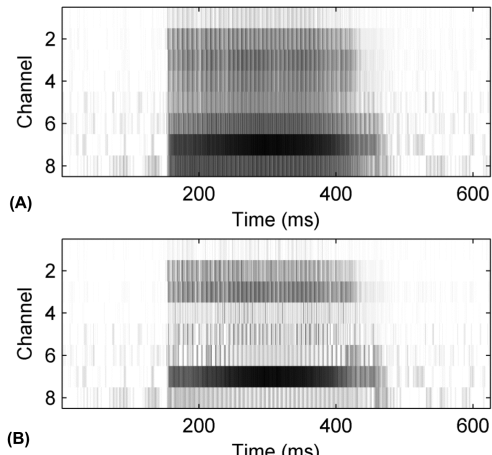


Figure 4.2.4: Spectrogram-like plots for the vowel /i/. (A) Amplitude outputs from the chip were used to construct a spectrogram. (B) With the use of zero-crossing information, the frequency resolution was sharpened without degrading the timing resolution.

Portion of System	Power Consumption
Microphone Front End Circuit and Microphone Bias	106.4μW
Automatic Gain Control Circuit	28μW
Bandpass Filters	37.8μW
Envelope Detectors	18.2μW
Logarithmic A/D and Digital CIS Output	56μW
Bias Circuits	4.2μW
Entire Chip Processor	251μW

Figure 4.2.5: Power consumption of various portions of the processor.

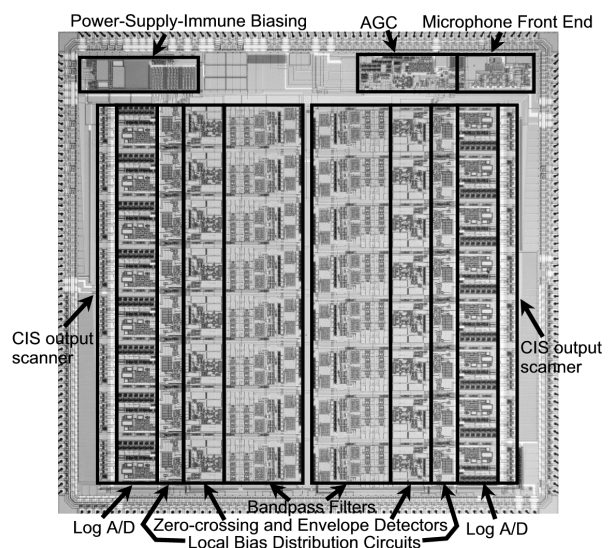


Figure 4.2.6: Chip micrograph.