Efficient Processing of Deep Neural Networks: A Tutorial and Survey

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***Abstract*—Deep neural networks (DNNs) are currently widely used for many artificial intelligence (AI) applications including computer vision, speech recognition, and robotics. While DNNs deliver state-of-the-art accuracy on many AI tasks, it comes at the cost of high computational complexity. Accordingly, techniques that enable efficient processing of deep neural network to improve *energy-efficiency* and *throughput* without sacrificing performance accuracy or increasing hardware cost are critical to enabling the wide deployment of DNNs in AI systems.**

This article aims to provide a comprehensive tutorial and survey about the recent advances towards the goal of enabling efficient processing of DNNs. Specifically, it will provide an overview of DNNs, discuss various platforms and architectures that support DNNs, and highlight key trends in recent efficient processing techniques that reduce the computation cost of DNNs either solely via hardware design changes or via joint hardware design and network algorithm changes. It will also summarize various development resources that can enable researchers and practitioners to quickly get started on DNN design, and highlight important benchmarking metrics and design considerations that should be used for evaluating the rapidly growing number of DNN hardware designs, optionally including algorithmic co-design, being proposed in academia and industry.

The reader will take away the following concepts from this article: understand the key design considerations for DNNs; be able to evaluate different DNN hardware implementations with benchmarks and comparison metrics; understand trade-offs between various architectures and platforms; be able to evaluate the utility of various DNN design techniques for efficient processing; and understand of recent implementation trends and opportunities.

I. Introduction

Deep neural networks (DNNs) are currently the foundation for many modern AI applications [1]. Since the breakthrough application of DNNs to speech recognition [2] and image recognition [3], the number of applications that use DNNs has exploded. These DNNs are employed in a myriad of applications from self-driving cars [4], to detecting cancer [5] to playing complex games [6]. In many of these domains, DNNs are now able to exceed human accuracy. The superior performance of DNNs comes from its ability to extract high-level features from raw sensory data after using statistical learning over a large amount of data to obtain an effective representation of an input space. This is different from earlier approaches that use hand-crafted features or rules designed by experts.

The superior accuracy of DNNs, however, comes at the cost of high computational complexity. While general-purpose compute engines, especially graphics processing units (GPUs), have been the mainstay for much DNN processing, increasingly there is interest in providing more specialized acceleration of the DNN computations. This article aims to provide an overview of DNNs, the various tools for understanding their behavior, and techniques being explored to efficiently accelerate their computations.

This paper is organized as follows:

- Section II provides background on the context of why DNNs are important, their history and applications.
- Section III gives an overview of the basic components of DNNs and popular DNN models currently in use.
- Section IV describe the various resources used for DNN research and development.
- Section V describes the various hardware platforms used to process DNN and the various optimizations to improve throughput and energy without impacting performance accuracy (i.e., produces bit-wise identical results).
- Section VI discusses how mixed-signal circuits and new memory technologies can be used for near-data processing to address the challenging data movement that dominates throughput and energy consumption of DNNs.
- Section VII describes various joint algorithm and hardware optimizations that can be performed on DNNs to improve both throughput and energy while trying to minimize impact on performance accuracy.
- Section VIII describes the key metrics that should be considered when comparing various DNNs designs.

II. Background on Deep Neural Networks (DNN)

In this section, we describe the position of deep neural networks (DNNs) in the context of AI in general and some of the concepts that motivated its development. We will also present a brief chronology of the major steps in its history, and some current domains to which it is being applied.

A. Artificial Intelligence and DNNs

Deep neural networks, also referred to as deep learning, are part of the broad field of artificial intelligence (AI), which is the science and engineering of creating intelligent machines that have the ability to achieve goals like humans do, according

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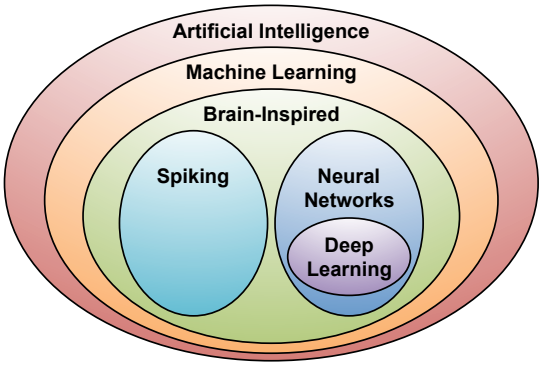


Fig. 1. Deep Learning in the context of Artificial Intelligence.

to John McCarthy, the computer scientist who coined the term in the 1950s. The relationship of deep learning to the whole of artificial intelligence is illustrated in Fig. 1.

Within artificial intelligence is a large sub-field called machine learning, which was defined in 1959 by Arthur Samuel as the field of study that gives computers the ability to learn without being explicitly programmed. That means there will be a single program which is created and then, outside the notion of programming, that program will be trained or learn how to do some intelligent activity and then it will be able to do it. This is in contrast to purpose-built programs whose behavior is defined by hand-crafted heuristics that explicitly and statically define its behavior.

The advantage of an effective machine learning algorithm is clear. Instead of the laborious and hit-or-miss approach of creating a distinct, custom program to solve each individual problem in a domain, the single machine learning algorithm simply needs to learn, via a processes called *training*, to handle each new problem.

Within the machine learning field, there is an area that is often referred to as brain-inspired computation. Since the brain is currently the best "machine" we know for learning and solving problems, it is a natural place to look for a machine learning approach. Therefore, a brain-inspired computation is a program or algorithm that takes some aspect of its basic form or functionality from the way the brain works. This is in contrast to attempts to create a brain, but rather the program aims to emulate some aspect of how we understand the brain to operate.

Although scientists are still exploring the details of how the brain works, it is generally believed that the main computational element of the brain is the neuron. There are approximately 86 billion neurons in the average human brain. The neuron themselves are connected together with a number of elements entering them called dendrites and an element leaving them called an axon. The neuron accepts the signals entering it via the dendrites, performs a computation on those signals, and generates a signal on the axon.

The axon of one neuron branches out and is connected to the dendrites of many other neurons. The connections between a branch of the axon and a dendrite is called a synapse. There are estimated to be 10^{14} to 10^{15} synapses in the average human brain.

A key characteristic of the synapse is that it can scale the value crossing it. That scaling factor can be referred to as a *weight*, and the way the brain is believed to learn is through changes to the weights associated with the synapses. Thus, different weights result in different responses to an input. Note that learning is the adjustment of the weights in response to a learning stimulus, while the organization (what might be thought of as the program) of the brain does not change. This characteristic makes the brain an excellent inspiration for a machine-learning-style algorithm.

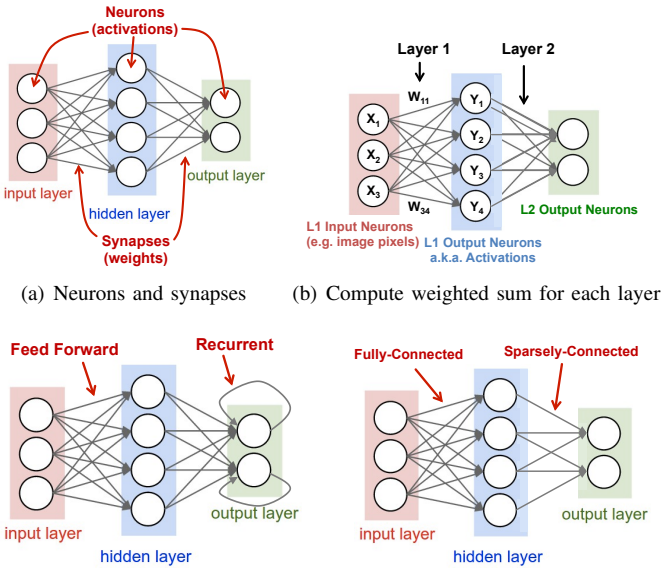
Within the brain-inspired computing paradigm there is a subarea called spiking computing. In this subarea, inspiration is taken from the fact that the communication on the dendrites and axons are spike-like pulses and that the information being conveyed is not just based on a spike's amplitude. Instead, it also depends on the time the pulse arrives and that the computation that happens in the neuron is a function of not just a single value but the width of pulse and the timing relationship between different pulses. An example of a project that was inspired by the spiking of the brain is the IBM TrueNorth [7]. In contrast to spiking computing, another subarea of brain-inspired computing is called neural networks, which is the focus of this article.

B. Neural Networks and Deep Neural Networks (DNNs)

Neural networks take their inspiration from the notion that a neuron's computation involves a weighted sum of the input values. These weighted sums correspond to the value scaling performed by the synapses and the combining of those values in the neuron. Furthermore, the neuron doesn't just output that weighted sum, since the computation associated with a cascade of neurons would then be a simple linear algebra operation. Instead there is a functional operation within the neuron that is performed on the combined inputs. This operation appears to be a non-linear function that causes a neuron to generate an output only if the inputs cross some threshold. Thus by analogy, neural networks apply a non-linear function to the weighted sum of the input values. We look at what some of those non-linear functions are later.

Fig. 2(a) shows diagrammatic picture of a computational neural network. The parts of the diagram are an input layer that receives some values. Those values are propagated to the neurons in the middle layers to the network, which is frequently called the the 'hidden layer' of the network. The weighted sums from one or more hidden layers are ultimately propagated to the 'output layer', which presents the final outputs of the network to the user. To align brain-inspired terminology with neural networks, the outputs of the *neurons* are often referred to as *activations*, and the *synapses* are often referred to as *weights* as shown in Fig. 2(a). We will used the activation/weight nomenclature in this article.

Fig. 2(b) shows an example of the computation at each layer, $y_j = f(\sum_{i=1}^{3} W_{ij} \times x_i)$ where W_{ij} are the weights, x_i are the input activations, y_j are the output activations, and $f(\cdot)$ is a non-linear activation function described in Section III-2.



(a) Neurons and synapses (b) Compute weighted sum for each layer

(c) Feedforward versus feedback (recurrent) networks (d) Fully connected versus sparse

Fig. 2. Simple Neural Network Example (Figure adopted from [8].)

Within the domain of neural networks, we have an area called *deep learning*. The original neural networks had very few layers in the network. In deep networks there are many more layers in the network. Networks today have five to more than a thousand of layers.

A current interpretation of the activity for vision applications in the many layers of these deep networks is that after entering all the pixels of an image into the first layer of the network, the weighted sums of that layer can be interpreted as the representing the presence of different low-level features in the image. At subsequent layers these features are combined into a measure of the likely presence of higher and higher level features, e.g. lines are combined into shapes, which are further combined into sets of shapes. And finally, given all this information the network provides a probability that these high-level features comprise a particular object.

Although this area is popularly called deep learning, the fundamental computation consists of various forms of deeply layered neural nets. Therefore, we will generally use the terminology *deep neural networks (DNNs)* in this article.

C. Inference versus Training

Since DNNs are an instance of a machine learning algorithm, the basic program does not change as it learns to perform its given tasks. In the specific case of DNNs, this learning involves determining the value of the weights in the network. This learning is referred to as *training* the network.

Once trained, the program can be run performing the network computation using the weights determined by the training. This operation of using the network to perform it task is referred to as *inference*.

In this section, we will use image classification, as shown in Fig. 4, as a driving example for training a DNN. When we evaluate a DNN, we give an input image and the output of the DNN is a vectors of scores, one for each object class; the class with the highest score indicates the most likely class of object in the image. The overarching goal for training a DNN is to determine how to set the weights to maximize the score of the correct class (as given from the labeled training data), and minimize the scores of the other incorrect classes. The gap between the ideal correct scores and the scores computed by the DNN based on its current weights is referred to as the *loss* (L). Thus the goal of training DNNs is to find a set of weights to minimize the average loss over a large dataset.

The weights (w_{ij}) are updated using a hill-climbing optimization process called gradient decent. A multiple of the gradient of the loss relative to each weight, which is the partial derivative of the loss for the weight, is used to update the weight (i.e., updated $w_{ij}^{t+1} = w_{ij}^{t} - \alpha \frac{dL}{dw_{ij}}$, where α is called the learning rate). Note that this gradient indicates how the weights should change in order to reduce the loss. The process is repeated iteratively to reduce the overall loss.

The gradient itself is efficiently computed through a process called *back-propagation* where the impact of the loss is passed backwards through the network to compute how the loss is affected by each weight.

This back-propagation computation is, in fact, very similar in form to the computation used for inference. Thus, techniques for efficiently performing inference can sometimes be useful for performing training. It is important to note, however, that due to the gradients use for hill-climbing, the precision requirement for training is higher than inference. Thus many of the reduced precision techniques discussed in Section VII are limited to inference only.

A variety of techniques are used to improve the efficiency and robustness of training. For example, often the loss from multiple sets of input data, i.e., a *batch*, are collected before a weight update is performed; this helps to speed up and stabilize the training process.

There are multiple ways to train the weights. The most common approach, described above, is called *supervised learning*, where all the training samples are labelled. *Unsupervised learning* is another approach where all the training samples are not labeled and essentially the goal is to find structure or clusters in the data. *Semi-supervised learning* falls in between the two approaches where only a small subset of the training data is labeled (e.g., use unlabeled data to define the cluster boundaries, and use the small amount of labeled data to label the clusters). Finally, *reinforcement learning* can be used to train a DNN to be a policy network such that given an input, it can output a decision on what action to take next and receive the corresponding reward; the process of training this network is to make decisions that maximize the received rewards (i.e., a reward function), and the training process must balance exploration (trying new actions) and exploitation (using actions that are known to give high rewards).

Another commonly used approach to determine weights is *fine-tuning*, where previously-trained weights are used as initialization and then weights are adjusted for a new dataset (e.g., transfer learning) or for a new constraint (e.g., reduced precision). This results in faster training as compared to starting from a random initialization, and can sometime result in better

DNN Timeline

- 1940s - Neural networks were proposed
- 1960s - Deep neural networks were proposed
- 1989 - Neural net for recognizing digits (LeNet)
- 1990s - Hardware for shallow neural nets (Intel ETANN)
- 2011 - Breakthrough DNN-based speech recognition (Microsoft)
- 2012 - DNNs for vision start supplanting hand-crafted approaches (AlexNet)
- 2014+ - Rise of DNN accelerator research (Neuflow, DianNao...)

Fig. 3. A concise history of neural networks

accuracy.

This article will focus the efficient processing of DNN inference rather than training, since DNN inference is often performed on embedded devices (rather than the cloud) where resources are limited as discussed in more detail later.

D. Development History

Although neural nets were proposed in the 1940s, the first practical application didn't appear until the late 1980s with the LeNet network for hand-written digit recognition [9]. Such systems are widely used for digit recognition on checks. However, the early 2010s have seen a blossoming of DNN-based applications with highlights such as Microsoft's speech recognition system in 2011 [2] and the AlexNet system for image recognition in 2012 [3]. A brief chronology of deep learning is shown in Fig. 3.

The deep learning successes of the early 2010s are believed to be a confluence of three factors. The first factor is the amount of available information to train the networks. To learn a powerful representation (rather than using hand-crafted approach) requires a large amount of training data. For example, Facebook receives over 350 millions images per day, Walmart creates 2.5 Petabytes of customer data hourly and YouTube has 300 hours of video uploaded every minute. As a result, the cloud providers and many businesses have a huge amount of data to train their algorithms.

The second factor is the amount of compute capacity available. Semiconductor and computer architecture advances have continued to provide increased computing capability, and we appear to have crossed a threshold where the large amount of computation of the DNN weighted sums, which is required both for using the DNN and in even greater degree for learning the weights, has become available for running the algorithms in a reasonable amount of time.

The successes of these early DNN applications opened the floodgates of algorithmic development. It also inspired the development of several (largely open source) frameworks that make it even easier for large numbers of researchers and practitioners to explore and use DNN networks. Combining these efforts contributed to the third factor, which is the evolution of the algorithmic techniques that improved accuracy significantly and broadened to domains to which DNNs are being applied.

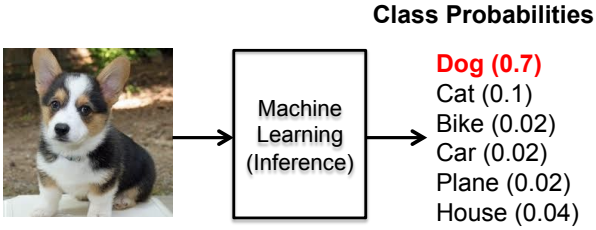


Fig. 4. Image classification task.

An excellent example of the successes in machine learning can be illustrated with the ImageNet challenge [10]. This challenge is a contest involving several different components. The first component is an image classification task where algorithms that are given an image must identify what is in the image, as shown in Fig. 4. The training set consists of 1.2 million images each of which is labeled with one of 1000 object categories that the image contains. And then the algorithm must accurately identify objects in a test set of images, which hasn't previously seen.

The graph in Fig. 5 shows the performance of the best entrant in the ImageNet contest over a number of years. One sees that the accuracy of the algorithms initially had an error rate of 25% or more. In 2012, a group from the University of Toronto used graphics processing units (GPUs) for their high compute capability and a deep neural network approach, namely AlexNet, and dropped the error rate by approximately 10% [3]. Their accomplishment resulted in an outpouring of deep learning style algorithms that have resulted in a steady stream of improvements.

In conjunction with the trend to deep learning approaches for the ImageNet challenge, there has a been a corresponding increase in the number of entrants using GPUs. From 2012 when only 4 entrants used GPUs to 2014 when almost all the entrants (110) were using them. This reflects the almost complete switch from traditional computer vision approaches to deep learning-based approaches for the competition.

In 2015, the ImageNet winning entry, ResNet [11], exceeded human-level accuracy with a top-5 error rate[1] below 5%. Since then, the error rate has dropped below 3% and more focus is now being placed on more challenging components of the challenge, such as object detection and localization. These successes are clearly a contributing factor to the wide range of applications to which DNNs are being applied.

E. Applications of DNN

Many applications can benefit from DNNs ranging from multimedia to medical space. In this section, we will provide examples of areas where DNNs are currently making an impact and highlight emerging areas where DNNs hope to make an impact in the future.

- **Image and Video** Video is arguably the biggest of the big data. It accounts for over 70% of today's Internet

[1]The top-5 error rate is measured based on whether the correct answer appears in one of the top 5 categories selected by the classifier.

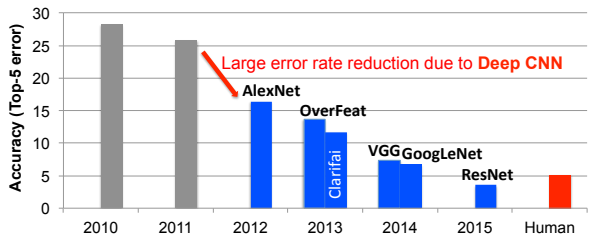


Fig. 5. Results from the ImageNet Challenge [10].

traffic [12]. For instance, over 800 million hours of video is collected daily worldwide for video surveillance [13]. Computer vision is necessary to extract the meaningful information from the video. DNNs have significantly improved the accuracy of many computer vision tasks such as image classification [10], object localization and detection [14], image segmentation [15], and action recognition [16].

- **Speech and Language** DNNs have significantly improved the accuracy of speech recognition [17] as well as many related tasks such as machine translation [2], natural language processing [18], and audio generation [19].
- **Medical** DNNs have played an important role in genomics to gain insight into the genetics of diseases such as autism, cancers, and spinal muscular atrophy [20–23]. They have also been used in medical imaging to detect skin cancer [5], brain cancer [24] and breast cancer [25].
- **Game Play** Recently, many of the grand AI challenges involving game play has also been overcome using DNNs. These successes also required innovations in training techniques and many rely on reinforcement learning [26], where the network training uses feedback from the consequences of the networks own outputs. DNNs surpassed human level accuracy in playing Atari [27] as well as Go [6], where an exhaustive search of all possibilities is not feasible due to the number of possible moves.
- **Robotics** DNNs have been successful in the domain of robotics tasks such as grasping with a robotic arm [28], motion planning for ground robots [29], visual navigation [4, 30], control to stabilize a quadcopter [31] and driving strategies for autonomous vehicles [32].

DNNs are already widely used in the multimedia applications (e.g., computer vision, speech recognition) today. Looking forward, we expect that DNNs will likely play an increasingly important role in the medical and robotics fields, as discussed above, as well as finance (e.g., for trading, energy forecasting, and risk assessment), infrastructure (e.g., structural safety, and traffic control), weather forecasting and event detection [33].

Efficient processing for all these myriad applications domains will depend on the any solutions being adaptable and scalable to be able to serve the new and varied forms of networks that these applications may employ.

F. Embedded versus Cloud

The various applications and aspects of DNN processing (training versus inference) have different computational needs. Specifically, training requires a large dataset[2] and significant computational resources for multiple iterations, and thus is typically performed on the cloud. The inference on the other hand can happen on the either the cloud or at the edge (e.g., IoT or mobile).

In many applications, it would be desirable to have the DNN inference processing near the sensor. For instance, in computer vision applications, such as measuring wait times in stores, traffic patterns, it would be desirable to use computer vision to extract the meaningful information from the video right at the image sensor rather than in the cloud to reduce the communication cost. For other applications such as autonomous vehicles, drone navigation and robotics, local processing is desired since the latency and security risk of relying on the cloud are too high. However, video involves a large amount of data, which is computationally complex to process; thus, low cost hardware to analyze video is challenging yet critical to enabling these applications.

Speech recognition enables us to seamlessly interact with electronic devices, such as smartphones. While currently most of the processing for applications such as Apple Siri and Amazon Alexa voice services is in the cloud, it is desirable to perform the recognition on the device itself to reduce latency and dependence on connectivity, and to increase privacy.

The embedded platforms that perform DNN inference processing have stringent energy consumption, compute and memory cost limitations. When DNN inference is performed in the cloud, there are often strong latency requirements for applications such as speech recognition. Therefore, in this article, we will focus on the compute requirements for inference processing rather than training.

III. Overview of DNNs

DNNs come in a wide variety of shapes and sizes depending on the application. The popular shapes and sizes are also evolving rapidly to improve accuracy and efficiency. The input to all DNNs is a set of values representing the information to be analyzed by the network. These values can be pixels of an image, sampled amplitudes of an audio wave or the numerical representation of the state of some system or game.

The networks that process the input come in two major forms: feed forward and recurrent as shown in Fig. 2(c). In feed-forward networks all of the computation is performed as a sequence of operations on the outputs of a previous layer. The final set of operations generates the output of the network, for example a probability that an image contains a particular object, the probability that an audio sequence contains a particular word, a bounding box in an image around an object or the proposed action that should be taken. In such DNNs, the network has no memory and the output for an input is always the same irrespective of the sequence of inputs previously given to the network.

In contrast, recurrent networks, of which Long Short Term Memory networks (LSTMs) [34] are a popular variant, have internal memory to allow long-term dependencies to affect

[2]One of the major drawbacks of DNNs is its need for large datasets to prevent over-fitting during training.

the output. In these networks, some intermediate operations generate values that are stored internally to the network and used as inputs to other operations in conjunction with the processing of a later input. In this article, we will focus on feed-forward networks as to-date little attention has been given to hardware acceleration specifically of recurrent networks.

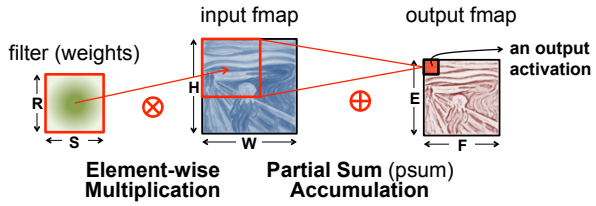
DNNs can be composed of *fully-connected* (FC, also referred to as multi-layer perceptrons) as shown in the leftmost layer of Fig. 2(d). In a fully-connected layer, all output activations are composed of a weighted sum of all input activations (i.e., all outputs are connected to all inputs). This requires a significant amount of storage and computation. Thankfully, in many applications, we can remove some connections between the activations by setting the weights to zero without affecting accuracy. This results in a *sparsely-connected layer*. A sparsely connected layer is illustrated in the rightmost layer of Fig. 2(d).

We can also make the computation more efficient by limiting the number of weights that contribute to an output. This sort of structured sparsity can arise if each output is only a function of a fixed-size window of inputs. Even further efficiency can be gained if the same set of weights are used in the calculation of every output. This *weight sharing* can significantly reduce the storage requirements for weights.

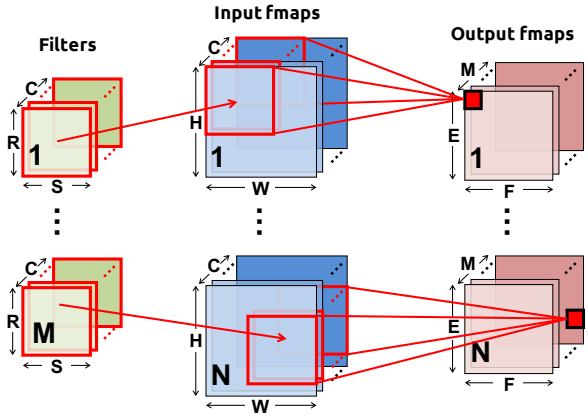
An extremely popular windowed, weight-shared network arises by structuring the computation as a convolution, as shown in Fig. 6(a), where the output is computed using only a small neighborhood of activations for the weighted sum (i.e., the filter has a limited receptive field, and all weights beyond a certain distance from the input is set to zero), and where the same set of weights are shared for every output (i.e., the filter is space invariant). This is a form of structured sparsity is orthogonal to the sparsity that occurs from network pruning as described in Section VII-B2. Accordingly, a *convolutional neural network* (CNN) is a popular form of DNN [35].

1) Convolutional Neural Networks (CNNs): CNNs are composed of multiple *convolutional layers* (CONV), as shown in Fig. 7, where each layer generates a higher-level abstraction of the input data, called a *feature map* (fmap), that preserves essential yet unique information. Modern CNNs are able to achieve superior performance by employing a very deep hierarchy of layers. CNN, also known as *ConvNets*, are widely used in a variety of applications including image understanding [3], speech recognition [36], game play [6], robotics [28], etc. The paper will focus on its use in image processing, specifically for the task of image classification [3].

Each of the CONV layers in the CNN is primarily composed of high-dimensional convolutions as shown in Fig. 6(b). In this computation there are a set of 2-D *input feature maps* (ifmaps), each of which is called a *channel*. Each channel is convolved with a distinct 2-D filter from the stack of filters, one for each channel. The results of the convolution at each point are summed across all the channels. In addition, a 1-D bias can be added to the filtering results, but some recent networks [11] remove its usage from part of the layers. The result of this computation is one channel of *output feature map* (ofmap). Additional stacks of 2-D filters can be used on the same input to create additional output channels. Finally, multiple stacks of input feature maps may be processed together as a *batch* to potentially improve reuse of the filter weights.



(a) 2-D convolution in traditional image processing



(b) High dimensional convolutions in CNNs

Fig. 6. Dimensionality of convolutions.

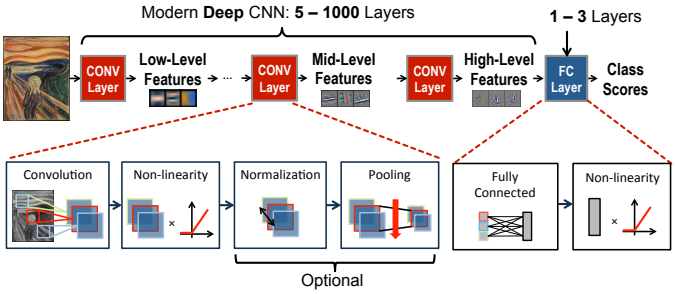


Fig. 7. Convolutional Neural Networks.

Given the shape parameters in Table I, the computation of a CONV layer is defined as

$$\mathbf{O}[z][u][x][y] = \mathbf{B}[u] + \sum_{k=0}^{C-1} \sum_{i=0}^{R-1} \sum_{j=0}^{R-1} \mathbf{I}[z][k][Ux+i][Uy+j] \times \mathbf{W}[u][k][i][j],$$
$$0 \leq z < N, 0 \leq u < M, 0 \leq x, y < E, E = (H - R + U)/U. \quad (1)$$

O, **I**, **W** and **B** are the matrices of the ofmaps, ifmaps, filters and biases, respectively. U is a given stride size. Fig. 6(b) shows a visualization of this computation (ignoring biases).

To align the terminology of CNNs with the generic DNN,

- filters are composed of weights (i.e., synapses)
- input images are composed of pixels (i.e., input neurons to first layer)
- input and output feature maps (ifmaps, ofmaps) are composed of activations (i.e., input and output neurons)

Shape Parameter	Description
N	batch size of 3-D fmaps
M	# of 3-D filters / # of ofmap channels
C	# of ifmap/filter channels
H	ifmap plane width/height
R	filter plane width/height (= H in FC)
E	ofmap plane width/height (= 1 in FC)

TABLE I
SHAPE PARAMETERS OF A CONV/FC LAYER.

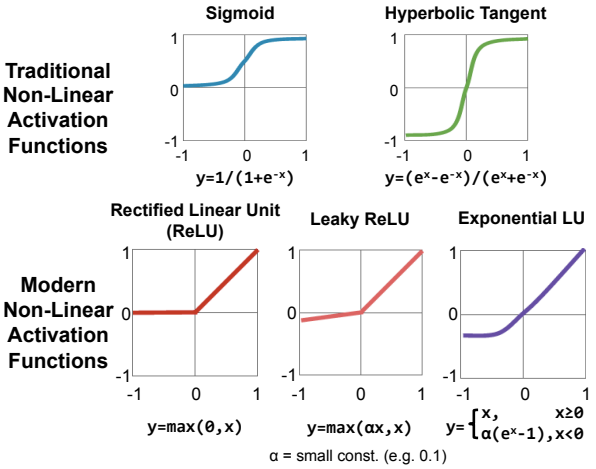


Fig. 8. Various forms of non-linear activation functions (Figure adopted from Caffe Tutorial [43]).

From five [3] to even more than a thousand [11] CONV layers are commonly used in recent CNN models. A small number, e.g., 1 to 3, of fully-connected (FC) layers are typically applied after the CONV layers for classification purposes. A FC layer also applies filters on the ifmaps as in the CONV layers, but the filters are of the same size as the ifmaps. Therefore, it does not have the weight sharing property of CONV layers. Eq. (1) still holds for the computation of FC layers with a few additional constraints on the shape parameters: $H = R$, $E = 1$, and $U = 1$.

In addition to CONV and FC layers, various optional layers can be found in a DNN such as the non-linearity (NON), pooling (POOL), and normalization (NORM). Each of these layers can be configured as discussed next.

2) Non-Linearity: A non-linear activation function is typically applied after each convolution or fully connected computation. Various non-linear functions are used to introduce non-linearity into the DNN as shown in Fig. 8. These include conventional non-linear functions such as sigmoid or hyperbolic tangent as well as rectified linear unit (ReLU) [37], which has become popular in recent years due to its simplicity and its ability to enable fast training. Variations of ReLU, such as leaky ReLU [38], parametric ReLU [39], and exponential LU [40] have also been explored for improved accuracy. Finally, a non-linearity called maxout, which takes the max value of two intersecting linear functions, has shown to be effective in speech recognition tasks [41, 42].

3) Pooling: Pooling enables the network to be robust and invariant to small shifts and distortions and is applied to each channel separately. It can be configured based on the size of its receptive field (e.g., 2×2) and the type of pooling (e.g., max or average), as shown in Fig. 9. Typically the pooling occurs on non-overlapping blocks (i.e., the stride is equal to the size of the pooling). Usually a stride of greater than one is used such that there is a reduction in the dimension of the representation (i.e., feature map).

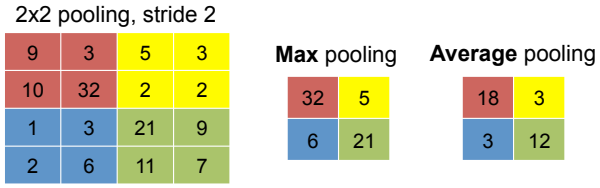


Fig. 9. Various forms of pooling (Figure adopted from Caffe Tutorial [43]).

4) Normalization: Controlling the input distribution across layers can help to significantly speed up training and improve accuracy. Accordingly, the distribution of the layer input activations (σ, μ) are normalized such that it has a zero mean and a unit standard deviation. In batch normalization, the normalized value is further scaled and shifted, as shown in Eq. (2), the parameters (γ, β) are learned from training [44]. ϵ is a small constant to avoid numerical problems. Prior to this, local response normalization [3] was used, which was inspired by lateral inhibition in neurobiology where excited neurons (i.e., high values activations) should subdue its neighbors (i.e., low value activations); however, batch normalization is now considered standard practice in the design of CNNs.

$$y = \frac{x - \mu}{\sqrt{\sigma^2 + \epsilon}}\gamma + \beta \tag{2}$$

A. Popular DNN Models

Many DNN models have been developed over the past two decades. Each of these models has a different "network architecture" in terms of number of layers, filter shapes (i.e., filter size, number of channels and filters), layer types, and connections between layers. Understanding these variations and trends is important for incorporating the right flexibility in any efficient DNN engine.

Although the first popular DNN, LeNet [45], was published in the 1990s, it wasn't until 2012 that the AlexNet [3] was used in the ImageNet Challenge [10]. We will give an overview of various popular DNNs that competed in and/or won the ImageNet Challenge [10] as shown in Fig. 5, most of whose models with pre-trained weights are publicly available for download; the DNN models are summarized in Table II. Two results for top-5 error results are reported. In the first row, the accuracy is boosted by using multiple crops from the image, and an ensemble of multiple trained models (i.e., the DNN needs to be run several times); these are results that are used to compete in the ImageNet Challenge. The second row reports the accuracy if only a single crop was used (i.e., the DNN is run only once), which is more consistent with what would be deployed in real applications.

LeNet [9] was one of the first CNN approaches introduced in 1989. It was designed for the task of digit classification in grayscale images of size 28×28. The most well known

version, LeNet-5, contains two convolutional layers and two fully connected layers [45]. Each convolutional layer uses filters of size 5×5 (1 channel per filter), with 6 filters in the first layer and 16 filters in the second layer. Average pooling of 2×2 is used after each convolution and a sigmoid is used for the non-linearity. In total, the LeNet requires 60k weights and 341k MACs per image. LeNet led to CNNs' first commercial success, as it was deployed in ATMs to recognize digits for check deposits.

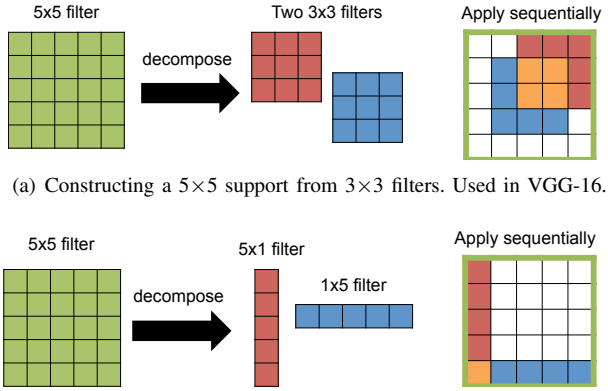
AlexNet [3] was the first CNN to win the ImageNet Challenge in 2012. It consists of five convolutional layers and three fully connected layers. Within each convolutional layer, there are 96 to 384 filters and the filter size ranges from 3×3 to 11×11, with 3 to 256 channels each. In the first layer, the 3 channels of the filter correspond to the red, green and blue components of the input image. A ReLU non-linearity is used in each layer. Max pooling of 3×3 is applied to the outputs of layers 1, 2 and 5. To reduce computation, a stride of 4 is used at the first layer of the network. AlexNet introduced the use of Local Response Normalization (LRN) in layers 1 and 2 before the max pooling; however, LRN was no longer used in subsequent CNNs as it was replaced with batch normalization. One important factor that differentiates AlexNet from LeNet is that the filters are much larger and the shapes vary from layer to layer. To reduce the number of weights in second layer, the 96 output channels of the first layer are split into two groups of 48 input channels for the second layer, such that the filters in the second layer only have 48 channels. Similarly, the weights in fourth and fifth layer are also split into two groups. In total, AlexNet requires 61M weights and 724M MACs to process one 227×227 input image.

Overfeat [46] has a very similar architecture to AlexNet with five convolutional layers and three fully connected layers. The main differences are that the number of filters is increased for layers 3 (384 to 512), 4 (384 to 1024), and 5 (256 to 1024), layer 2 is not split into two groups, the first fully connected layer only has 3072 channels rather than 4096, and the input size is 231×231 rather than 227×227. As a result, the number of weights grows to 144M and the number of MACs grows to 2.8G per image. Overfeat has two different models: fast (described here) and accurate. The accurate model used in the ImageNet Challenge gives a 0.65% lower top-5 error rate than the fast model at the cost of 1.9× more MACs

VGG-16 [47] goes deeper to 16 layers consisting of 13 convolutional layers and 3 fully connected layers. In order to balance out the cost of going deeper, larger filters (e.g., 5×5) are built from multiple smaller filters (e.g., 3×3), which have fewer weights, to achieve the same receptive fields as shown in Fig. 10(a). As a result, all the convolutional layers have the same filter size of 3×3. In total, VGG-16 requires 138M weights and 15.5G MACs to process one 224×224 input image. VGG has two different models: VGG-16 (described here) and VGG-19. VGG-19 gives a 0.1% lower top-5 error rate than VGG-16 at the cost of 1.27× more MACs.

GoogLeNet [48] goes even deeper with 22 layers. It introduced an inception module, shown in Fig. 11, which is composed of parallel connections, whereas previously there was only a single serial connection. Different sized filters (i.e., 1×1, 3×3, 5×5), along with 3×3 max-pooling, are used for each parallel connection and their outputs are concatenated for the inception output. Using multiple filter sizes has the effect of processing the input at multiple scales. For improved training speed, GoogLeNet is designed such that the weights and the activations, which are stored for back propagation during training, could all fit into the GPU memory. In order to reduce the number of weights, 1×1 filters are applied as a "bottleneck" to reduce the number of channels for each filter [49]. The 22 layers consist of three convolutional layers, followed by 9 inceptions layers (each of which are two convolutional layers deep), and one fully connected layer. Since its introduction in 2014, GoogleNet (also referred to as Inception) has multiple versions: v1 (described here), v3 [3] and v4. v3 decomposes the convolutions by using smaller 1-D filters as shown in Fig. 10(b) to reduce number of MACs and weights in order to go deeper to 42 layers. In conjunctions with batch normalization [44], v3 achieves over 3% lower top-5 error than v1 with 2.5× increase in computation [50]. v4 uses residual connections [51], described the next section, for at 0.4% reduction in error.

ResNet [11], also known as Residual Net, uses residual



(a) Constructing a 5×5 support from 3×3 filters. Used in VGG-16.

(b) Constructing a 5×5 support from 1×5 and 5×1 filter. Used in GoogleNet/Inception v3 and v4.

Fig. 10. Decomposing larger filters into smaller filters.

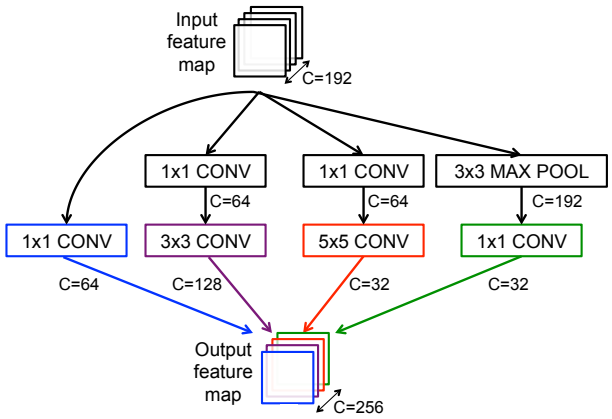
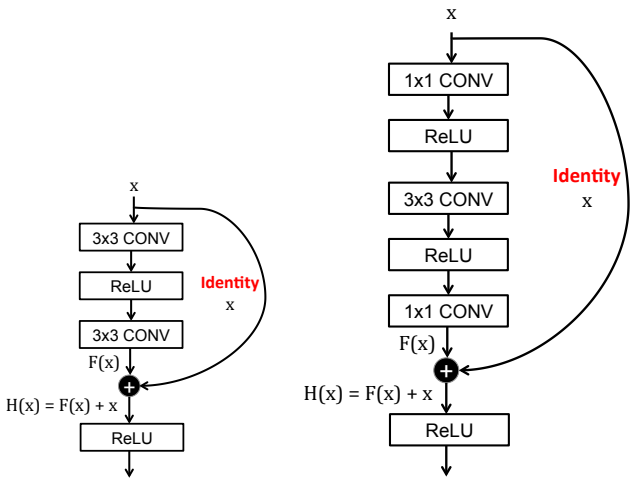


Fig. 11. Inception module from GoogleNet [48] with example channel lengths. Note that each CONV layer is followed by a ReLU (not drawn).

[3] v2 is very similar to v3.



(a) Without bottleneck (b) With bottleneck

Fig. 12. Shortcut module from ResNet [11]. Note that ReLU following last CONV layer in short cut is *after* the addition.

connections to go even deeper (34 layers or more). It was the first entry DNN in ImageNet Challenge that exceeded human-level accuracy with a top-5 error rate below 5%. One of the challenges with deep networks is the vanishing gradient. As the error back-propagates through the network the gradient shrinks, which affects the ability to update the weights in the earlier layers for very deep networks. Residual net introduces a "short cut" module which contains an identity connection such that the "weight" layers (i.e., CONV layers) can be skipped as shown in Fig. 12. Rather than learning the function for the weight layers $F(x)$, the short cut module learns the residual mapping ($F(x) = H(x) - x$). Initially, $F(x)$ is zero and the identity connection is taken; then gradually during training, the actual forward connection through the weight layer is used. This is similar to the LSTM networks that are used for sequential data. ResNet also uses the "bottleneck" approach of using 1×1 to reduce the number of weight parameters. As a result, the two layers in the short cut module are replaced by three layers (1×1, 3×3, 1×1) where the 1×1 reduces and then increases (restores) the weights. ResNet-50 consists of one convolutional layers, followed by 16 short cut layers (each of which are three convolutional layers deep), and one fully connected layer; it requires 25.5M weights and 3.9G MAC per image. There are various versions of ResNet with multiple depths (e.g., *without bottleneck:* 18, 34; *with bottleneck:* 50, 101, 152). The ResNet with 152 layers was the winner of the ImageNet Challenge requiring 11.3G MACs and 60M weights. Compared to ResNet-50, it reduces the top-5 error by around 1% at the cost of 2.9× more MACs and 2.5× more weights.

Several trends can be observed in the popular DNNs shown in Table II. Increasing the depth of the network tends to provide higher accuracy. Controlling for number of weights, a deeper network can support a wider range of non-linear functions that are more discriminative and also provides more levels of hierarchy in the learned representation [11, 47, 48, 52]. The number of filter shapes continues to vary across layers, thus flexibility is important. Furthermore, most of the computation has been placed on convolutional layers rather than fully connected. In addition, the number of weights in the fully connected layers is reduced and in most recent networks (since GoogLeNet) the convolutional layers also dominates in terms of weights. Thus, the focus of hardware implementations should be on addressing the efficiency of the convolutional layers, which are increasingly important.

IV. DNN DEVELOPMENT RESOURCES

One of the key factors that has enabled the rapid development of DNNs is the set of development resources that have been made available by the research community and industry. These resources are also key to the development of DNN accelerators by providing characterizations of the workloads and facilitating the exploration of trade-offs in model complexity and accuracy. This section will describe these resources such that those who are interested in this field can quickly get started.

A. Frameworks

For ease of DNN development and to enable sharing of trained networks, several deep learning frameworks have been developed from various sources. These open source libraries contain software libraries for DNNs. Caffe was made available in 2014 from UC Berkeley [43]. It supports C, C++, Python and MATLAB. Tensorflow was released by Google in 2015, and supports C++ and python; it also supports multiple CPU and GPUs. It has more flexibility than Caffe, with the computation expressed as dataflow graphs to manage the tensors (multidimensional arrays). Another popular framework is Torch, which was developed by Facebook and NYU and supports C, C++ and Lua. There are several other frameworks such as Theano, MXNet, CNTK, which are described in [57].

The existence of such frameworks not only are a convenient aid for DNN researchers and application designers, but they are also invaluable for engineering high performance or more efficient DNN computation engines. For example, most frameworks can use Nvidia's cuDNN library for rapid execution on Nvidia GPUs. This acceleration is transparent to the user of the framework. Similarly, transparent incorporation of dedicated hardware accelerators can be achieved as was done with the Eyeriss chip [58].

Finally, these frameworks are a valuable source of workloads for hardware researchers. They can be used to drive experimental designs for different workloads, for profiling different workloads and for exploring hardware software trade-offs.

B. Models

Pretrained DNN models can be downloded from various websites [53–56] for the various different frameworks. It should be noted that even for the same DNN (e.g., AlexNet) the accuracy of these models can vary by around 1 to 2% depending on how the model was trained, and thus the results do not always exactly match the original publication.

Metrics	LeNet 5	AlexNet	Overfeat fast	VGG 16	GoogLeNet v1	ResNet 50
Top-5 error†	n/a	16.4	14.2	7.4	6.7	5.3
Top-5 error (single crop)†	n/a	19.8	17.0	8.8	10.7	7.0
Input Size	28×28	227×227	231×231	224×224	224×224	224×224
# of CONV Layers	2	5	5	13	57	53
Depth in # of CONV Layers	2	5	5	13	21	49
Filter Sizes	5	3,5,11	3,5,11	3	1,3,5,7	1,3,7
# of Channels	1, 20	3-256	3-1024	3-512	3-832	3-2048
# of Filters	20, 50	96-384	96-1024	64-512	16-384	64-2048
Stride	1	1,4	1,4	1	1,2	1,2
Weights	2.6k	2.3M	16M	14.7M	6.0M	23.5M
MACs	283k	666M	2.67G	15.3G	1.43G	3.86G
# of FC Layers	2	3	3	3	1	1
Filter Sizes	1,4	1,6	1,6,12	1,7	1	1
# of Channels	50, 500	256-4096	1024-4096	512-4096	1024	2048
# of Filters	10, 500	1000-4096	1000-4096	1000-4096	1000	1000
Weights	58k	58.6M	130M	124M	1M	2M
MACs	58k	58.6M	124M	130M	1M	2M
Total Weights	60k	61M	146M	138M	7M	25.5M
Total MACs	341k	724M	2.8G	15.5G	1.43G	3.9G
Pretrained Model Website	[53]‡	[54, 55]	n/a	[54–56]	[54–56]	[54–56]

TABLE II

SUMMARY OF POPULAR DNNS [3, 11, 45, 47, 48]. †ACCURACY IS MEASURED BASED ON TOP-5 ERROR ON IMAGENET [10]. ‡THIS VERSION OF LENET-5 HAS 431K WEIGHTS FOR THE FILTERS AND REQUIRES 2.3M MACS PER IMAGE, AND USES RELU RATHER THAN SIGMOID.

C. Popular Datasets for Classification

It is important to factor in the difficulty of the task when comparing different DNN models. For instance, the task of classifying handwritten digits from the MNIST dataset [59] is much simpler than classifying an object into one of a 1000 classes as is required for the ImageNet dataset [10](Fig. 13). It is expected that the size of the classifier or network (i.e. number of weights) and the number of MACs will be larger for the more difficult task than the simpler task and thus require more energy and have lower throughput. For instance, LeNet-5[45] is designed for digit classification, while AlexNet[3], VGG-16[47], GoogLeNet[48], and ResNet[11] are designed for the 1000 class image classification.

There are many AI tasks that come with publicly available datasets in order to evaluate the accuracy of a given DNN. Public datasets are important for comparing the accuracy of different approaches. The simplest and most common task is image classification. Image classification involves being given an entire image, and selecting 1 of N classes that it most likely belongs to. There is no localization or detection.

MNIST is a widely used dataset for digit classification that was introduced in 1998 [59]. It consists of 28×28 pixel grayscale images of handwritten digits. There are 10 classes (for 10 digits) and 60,000 training images and 10,000 test images. LeNet-5 was able to achieve an accuracy of 99.05% when MNIST was first introduced. Since then the accuracy has increased to 99.79% using regularization of neural networks with dropconnect [60]. Thus, MNIST is now considered a fairly easy dataset.

CIFAR is a dataset that consists of 32×32 pixel colored images of of various objects, which was released in 2009 [61]. CIFAR is a subset of the 80 million tiny image dataset [62]. CIFAR-10 is composed of 10 mutually exclusive classes. There are 50,000 training images (5000 per class) and 10,000 test images (1000 per class). Restricted Boltzmann Machine (RBM) with fine-tuning was able to achieve 64.84% accuracy on CIFAR-10 when it was first introduced [63]. Since then the accuracy has increased to 96.53% using fractional max pooling [64].

ImageNet is a large scale image dataset was first introduced in 2010; the dataset stabilized in 2012 [10]. It contains images of 256×256 pixel in color, with 1000 classes. The classes are defined using the WordNet as a backbone to handle disambiguous words meanings and combining together synonyms into the same object category. In otherwords, there is a hierarchy for the ImageNet categories. The 1000 classes were selected such that there is no overlap in the ImageNet hierarchy. The ILSVRC dataset contains many fine-grained categories including 120 different breeds of dogs. There are 1.3M training images (732 to 1300 per class), 100,000 testing images (100 per class) and 50,000 validation images (50 per class).

The accuracy of the ImageNet challenge are reported using two metrics: Top-5 and Top-1 error. Top-5 error means that if any of the top 5 scoring categories are the correct category, it is counted as a correct classification. The Top-1 requires that the top scoring category be correct. In 2012, the winner of the ImageNet Challenge (AlexNet) was able to achieve an accuracy of 83.6% for the top-5 error (which is substantially better than the 73.8% which was second place that year that did not use DNNs); it achieved 61.9% on the top-1 of the validation set. In 2016, the highest accuracy was 96.0% for top-5 error.

In summary of the various image classification datasets, it is clear that MNIST is a fairly easy dataset, while ImageNet is a challenging one with a wider coverage of classes. Thus in terms of evaluating the accuracy of a given DNN, it is important to consider that dataset upon which the accuracy is measured.

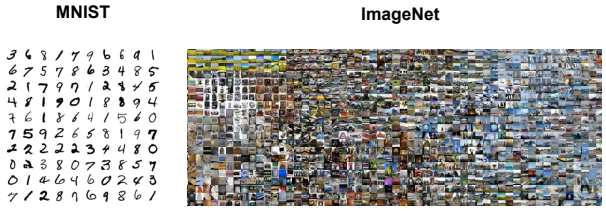


Fig. 13. MNIST (10 classes, 60k training, 10k testing) [59] vs. ImageNet (1000 classes, 1.3M training, 100k testing)[10] dataset.

D. Datasets for Other Tasks

Since the accuracy of the state-of-the-art DNNs are performing better than human level accuracy on image classification task, ImageNet has started to focus on more challenging tasks such as single-object localization and object detection. For single-object localization, the target object must be localized and classified (1000 classes). The DNN outputs the top five categories and top five bounding box location. There is no penalty for identifying an object that is in the image but not included in the ground truth. For object detection, all objects in the image must of localized and classified (200 classes). The bounding box for all objects in these categories must be labeled. Objects that are not labeled are penalized as is duplicate detections.

Beyond ImageNet, there are also other popular image datasets for computer vision tasks. For object detection, there is the PASCAL VOC (2005-2012) dataset that contains 11k images representing 20 classes (27k object instances, 7k of which has detailed segmentation) [65]. For object detection, segmentation and recognition in context, there is the MS COCO dataset with 2.5M labeled instances in 328k images (91 object categories) [66]; compared to ImageNet, COCO has fewer categories but more instances per category, which is useful for precise 2-D localization. It has more labeled instances per image to potentially help with contextual information.

Most recently even larger scale dataset have been made available. For instance, Google has an Open Images dataset with over 9M images [67], spanning 6000 categories. There is also a Youtube dataset with 8M videos (0.5M hours of video) covering 4800 classes [68]. Google also release an audio dataset comprised of 632 audio event classes and a collection of 2M human-labeled 10-second sound clips [69]. These large datasets will be evermore important as DNN become deeper with more weight parameters to train.

Undoubtedly, both larger datasets and datasets for new domains will serve as important resources for profiling and exploring the efficiency of future DNN engines.

V. Hardware for DNN Processing

Due to the popularity of DNNs, many recent hardware platforms have special features that target DNN processing. For instance, the Intel Knight Landing CPU features special vector instructions for deep learning; the Nvidia PASCAL GP100 GPU features 16-bit floating point (FP16) arithmetic support to perform two FP16 operation on a single precision core for faster deep learning. Systems have also been built specifically for DNN processing such as Nvidia DGX-1 and Facebook's Big Basin custom DNN server [70]. DNN inference has also been demonstrated on various embedded System-on-Chips (SoC) such as Nvidia Tegra and Samsung Exynos as well as FPGAs. Accordingly, it's important to have a good understanding of how the processing is being performed on these platforms, and how application specific accelerators can be designed for DNNs for further improvement in throughput and energy efficiency.

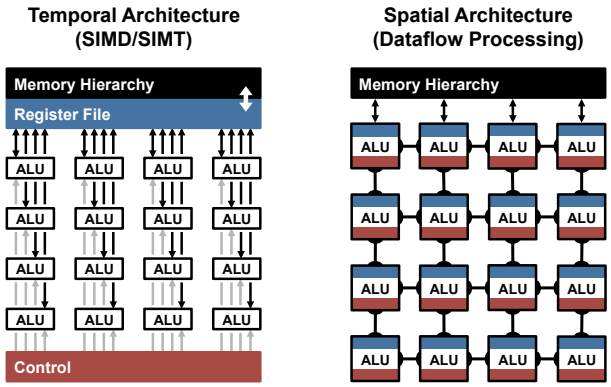


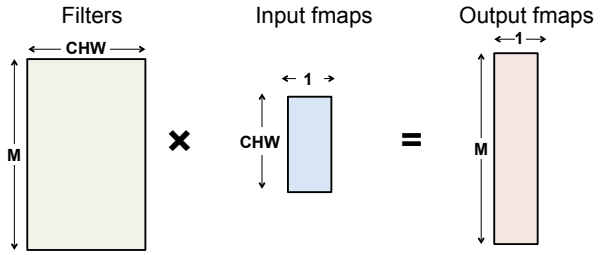
Fig. 14. Highly-parallel compute paradigms.

The fundamental component of both the CONV and FC layers are the multiply-and-accumulate (MAC) operations, which can be easily parallelized. In order to achieve high performance, highly-parallel compute paradigms are very commonly used, including both temporal and spatial architectures as shown in Fig. 14. The temporal architectures, also called SIMD or SIMT, appears mostly in CPUs or GPUs. It uses a centralized control for a large number of ALUs. These ALUs can only fetch data from the memory hierarchy and cannot communicate data with each other. In contrast, spatial architectures use dataflow processing, i.e., the ALUs form a processing chain so that they can pass data from one to another directly. Sometimes each ALU can have its own control logic and local memory, called a scratchpad or register file. We refer the an ALU with its own local memory as a processing engine (PE). Spatial architectures are commonly used for DNNs in ASIC designs. In this section, we will discuss the different design strategies for efficient processing on these different platforms, without any impact on accuracy (i.e., all approaches in this section produce bit-wise identical results); specifically,

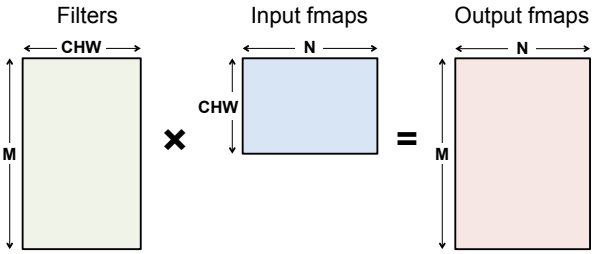
- For *temporal* architectures such as CPUs and GPUs, we will discuss how *computational transforms* on the kernel can reduce the number of multiplications to *increase throughput*.
- For *spatial* architectures used in accelerators, we will discuss how *dataflows* can increase data reuse from low cost memories in the memory hierarchy to *reduce energy consumption*.

A. Accelerate Kernel Computation on CPU and GPU Platforms

CPUs and GPUs use temporal architectures such as SIMD or SIMT to perform the MACs in parallel. All the ALUs share the same control and memory (register file). On these platforms, both the FC and CONV layers are often mapped to a matrix

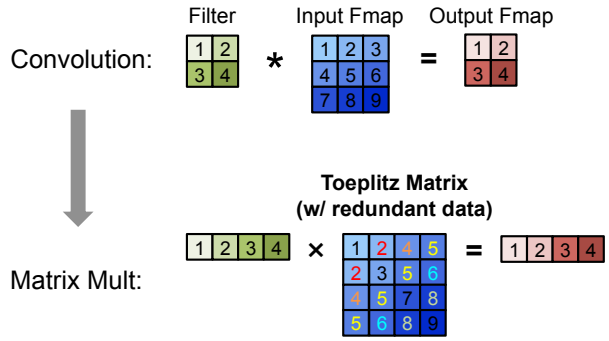


(a) Matrix Vector multiplication is used when computing a single output feature map from a single input feature map.

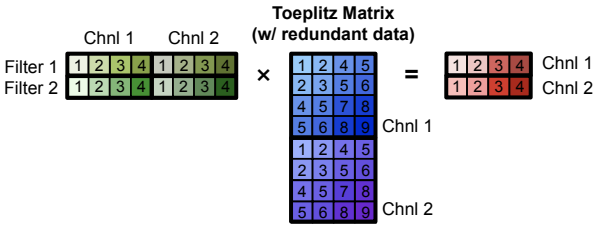


(b) Matrix Multiplications is used when computing N output feature maps from N input feature maps.

Fig. 15. Mapping to matrix multiplication for fully connected layers



(a) Mapping convolution to Toeplitz matrix.



(b) Extend Toeplitz matrix to multiple channels and filters

Fig. 16. Mapping to matrix multiplication for convolutional layers

multiplication (i.e., the kernel computation). Fig. 15 shows how a matrix multiplication is used for the FC layer. The height of the filter matrix is the number of filters and the width is the number of weights per filter (input channels (C) $\times$ width (W) $\times$ height (H), since $R = W$ and $S = H$ in the FC layer); the height of the input feature maps matrix is the number of activations per input feature map ($C \times W \times H$), and the width is the number of input feature maps (one in Fig. 15(a) and N in Fig. 15(b)); finally, the height of the output feature map matrix is the number of channels in the output feature maps (M), and the width is the number of output feature maps (N), where each output feature map of the FC layer is $1\times1\times$output channels (M).

The CONV layer in a DNN can also be mapped to a matrix multiplication using the Toeplitz matrix as shown in Fig. 16. The downside for using matrix multiplication for the CONV layers is that there is redundant data in the input feature map matrix as highlighted in Fig. 16(a). This can lead to either inefficiency in storage, or a complex memory access pattern.

There are software libraries designed for CPUs (e.g., OpenBLAS, Intel MKL, etc.) and GPUs (e.g., cuBLAS, cuDNN, etc.) that optimize for matrix multiplications. The matrix multiplication is tiled to the storage hierarchy of these platforms, which are on the order of a few megabytes at the higher levels.

The matrix multiplications on these platforms can be further sped up by applying computational transforms to the data to reduce the number of multiplications, while still giving the same bitwise result. Often this can come at a cost of increased number of additions and a more irregular data access pattern.

Fast Fourier Transform (FFT) [71, 72] is a well known approach, shown in Fig. 17 that reduces the number of multiplications from O($N_o^2 N_f^2$) to O($N_o^2 log_2 N_o$), where the output size is $N_o \times N_o$ and the filter size is $N_f \times N_f$. To perform the convolution, we take the FFT of the filter and input feature map, and then perform the multiplication in the frequency domain; we then apply an inverse FFT to the resulting product to recover the output feature map in the spatial domain. However, there are several drawbacks to using FFT: (1) the benefits of FFTs decrease with filter size; (2) the size of the FFT is dictated by the output feature map size which is often much larger than the filter; (3) the coefficients in the frequency domain are complex. As a result, while FFT reduces computation, it requires larger storage capacity and bandwidth. Finally, a popular approach for reducing complexity is to make the weights sparse, which will be discussed in Section VII-B2; using FFTs makes it difficult for this sparsity to be exploited.

Several optimizations can be performed on FFT to make it more effective for DNNs. To reduce the number of operations, the FFT of the filter can be precomputed and stored. In addition, the FFT of the input feature map can be computed once and used to generate multiple channels in the output feature map. Finally, since an image contains real values, its Fourier Transform is symmetric and this can be exploited to reduce storage and computation cost.

Other approaches include Strassen [73] and Winograd [74], which rearrange the computation such that the number of multiplications scale from O(N^3) to O($N^{2.807}$) and 2.5$\times$ for a 3$\times$3 filter, respectively, at the cost of reduced numerical stability, increased storage requirements, and specialized processing depending on the size of the filter.

In practice, different algorithms might be used for different filter shapes and sizes (e.g., FFT for filters greater than 5$\times$5, and Winograd for filters 3$\times$3 and below). The platform libraries would need to be flexible enough to support these different approaches.

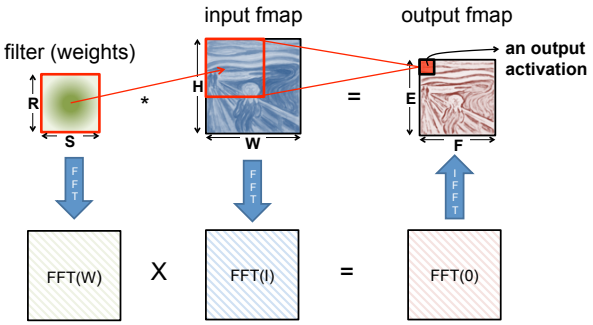


Fig. 17. FFT to accelerate DNN.

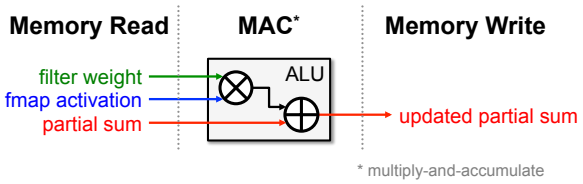


Fig. 18. Read and write access per MAC.

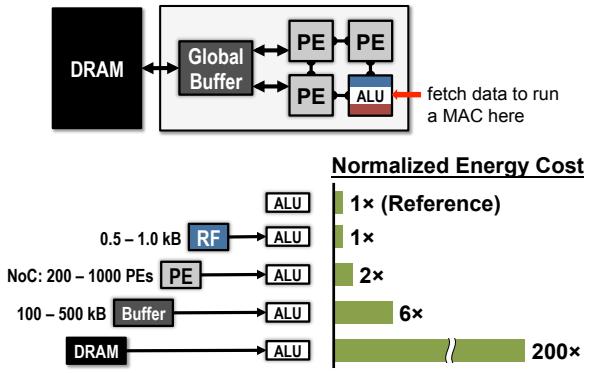


Fig. 19. Memory hierarchy and data movement energy [76].

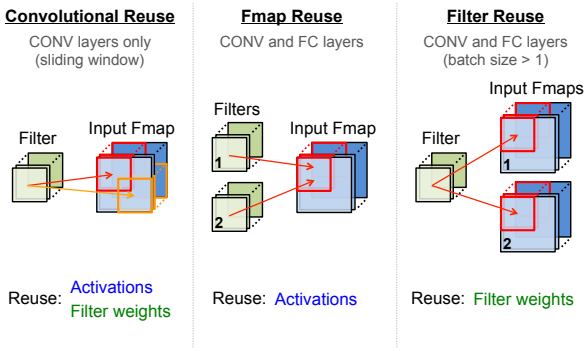


Fig. 20. Data reuse opportunities in DNNs [76].

B. *Energy-Efficient Dataflow for Accelerators*

For DNNs, the bottleneck for processing is in the memory access. Each MAC requires three memory reads (for filter weight, fmap activation, and partial sum) and one memory write (for the updated partial sum) as shown in Fig. 18. In the worst case, all of the memory accesses have to go through the off-chip DRAM, which will severely impact both of the throughput and energy efficiency. For example, in AlexNet, to support its 724M MACs, nearly 3000M DRAM accesses will be required. Furthermore, DRAM accesses require up to several orders of magnitude higher energy than computation [75].

Accelerators, such as spatial architectures as shown in Fig. 14, provide an opportunity to reduce the energy cost of data movement by introducing several levels of local memory hierarchy with different energy costs as shown in Fig. 19. This includes a large global buffer with a size of several hundreds kilobytes that connects to DRAM, a inter-PE network that can pass data directly between the ALUs, and a register file (RF) within each processing element (PE) with a size of a few kilobytes or less. The multiple levels of memory hierarchy help to improve energy efficiency by providing low-cost data accesses. For example, fetching the data from the RF or neighbor PEs is going to cost 1 or 2 orders of magnitude lower energy than from DRAM.

Accelerators can be designed to support specialized processing dataflows that leverage this memory hierarchy. The dataflow decides what data gets read into which level of memory hierarchy and when are they getting processed. Since theres no randomness in the processing of DNNs, it is possible to design a fixed dataflow that can optimize for the best energy efficiency. The optimized dataflow minimizes access from the expensive levels of the memory hierarchy. Large memories that can store a significant amount data consume more energy than smaller memories. For instance, DRAM which can store gigabytes of memory consume two orders of magnitude higher energy per access than a small on-chip memory of a few kilobytes. Thus, every time a piece of data is moved from an expensive level to a lower cost level, we want to reuse that piece of data as much as possible to minimize subsequent accesses. The challenge is the storage capacity of these low cost memories are limited. Thus we needed to explore different dataflows that maximize reuse under these constraints.

For DNNs, we investigate dataflows that exploit three forms of input data reuse (convolutional, feature map and filter) as shown in Fig. 20. For convolutions reuse, the same input feature map activations and filter weights are used within a given channel, just in different combinations for different products. For feature map reuse, multiple filters are applied to the same feature map, so the input feature map activations are used multiple times across filters. Finally, for filter reuse, when multiple input feature maps are processed (referred to as a batch), so the filter weights are used multiple times across input features maps.

If we can harness the three types of data reuse by storing the data in the local memory hierarchy and accessing them multiple times without going back to the DRAM, it can save a significant amount of DRAM accesses. For example, in AlexNet, the number of DRAM reads can be reduced by up to 500× in the CONV layers. The local memory can also be used for partial sum accumulation, so they do not have to reach DRAM. In the best case, if all data reuse and accumulation can be achieved by the local memory hierarchy, the 3000M DRAM accesses in AlexNet can be reduced to only 61M.

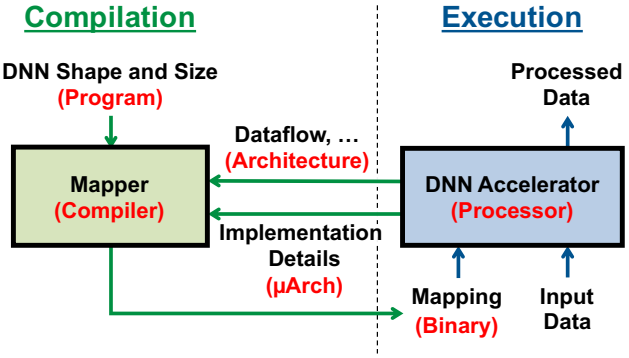
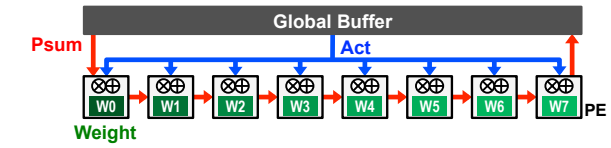
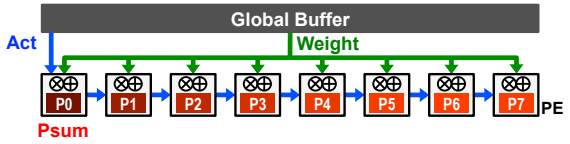


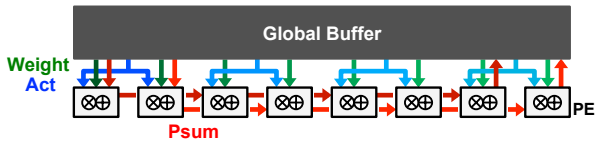
Fig. 21. An analogy between the operation of DNN accelerators (texts in black) and that of general-purpose processors (texts in red). Figure adopted from [77].



(a) Weight Stationary



(b) Output Stationary



(c) No Local Reuse

Fig. 22. Dataflows for DNNs [76].

The operation of DNN accelerators is analogous to that of general-purpose processors as illustrated in Fig. 21 [77]. In conventional computer systems, the compiler translates the program into machine-readable binary codes for execution; in the processing of DNNs, the mapper translates the DNN shape and size into a hardware-compatible mapping for execution. While the compiler usually optimizes for performance, the mapper optimizes for energy efficiency.

The following taxonomy (Fig. 22) can be used to classify these DNN dataflows in recent work [78–89] based on their data handling characteristics [76]:

1) Weight stationary (WS): The weight stationary dataflow is designed to minimize the energy consumption of reading weights by maximizing the accesses of weights from the register file (RF) at the PE (Fig. 22(a)). Each weight is read from DRAM into the RF of each PE and stays stationary for further accesses. The processing runs as many MACs that use the same weight as possible while the weight is present in the RF; it maximizes convolutional and filter reuse of weights. The inputs and partial sums must move through the spatial array and global buffer. The input fmap activations are broadcast to all PEs and then the partial sums are spatially accumulated across the PE array.

One example of previous works that implement weight stationary dataflow is nn-X, or neuFlow [81], which uses eight 2-D convolution engines for processing a 10×10 filter. There are total 100 MAC units, i.e. PEs, per engine each having a weight that stays stationary for processing. The input fmap activations are broadcast to all MAC units and the partial sums are accumulated across the MAC units. In order to accumulate the partial sums correctly, additional delay storage elements are required, which are counted into the required size of local storage. Other weight stationary examples are found in [78–80, 82, 83].

2) Output stationary (OS): The output stationary dataflow is designed to minimize the energy consumption of reading and writing the partial sums (Fig. 22(b)). It keeps the accumulation of partial sums for the same output activation value local in the RF. In order to keep the accumulation of each partial sum stationary in the RF, one common implementation is to stream the input activations across the PE array and broadcast the weight to all PEs in the array.

One example that implements the output stationary dataflow is ShiDianNao [85], where each PE handles the processing for each output activation value by fetching the corresponding input activations from neighboring PEs. The PE array implements dedicated network to pass data horizontally and vertically. Each PE also has data delay registers to keep data around for the required amount of cycles. At the system level, the global buffer streams the input activations and broadcasts the weights into the PE array. The partial sums are accumulated inside each PE and then get streamed out back to the global buffer. Other examples of output stationary are found in [84, 86].

There are multiple possible variants of output stationary as shown in Fig. 23, since the output activations that get processed at the same time can come from different dimensions. For example, the variant OS_A targets the processing of CONV layers, and therefore focuses on the processing of output activations from the same channels at a time in order to maximize data reuse opportunities. The variant OS_C targets the processing of FC layers, and focuses on generating output activations from all different channels, since each channel only has one output activation. The variant OS_B is something in between OS_A and OS_C. Example of variants OS_A, OS_B, and OS_C are [85], [84], and [86], respectively.

3) No local reuse (NLR): While small register files are efficient in terms of energy (pJ/bit), they are inefficient in terms area (μm^2/bit). In order to maximize the storage capacity, and minimize the off-chip memory bandwidth, no local storage is allocated to the PE and instead all that area is allocated to the global buffer to increase its capacity (Fig. 22(c)). This no local reuse dataflow differs from the previous dataflows in that nothing stays stationary inside the PE array. As a result, there will be increased traffic on the spatial array and to the global buffer for all data types. Specifically, it has to multicast the activations, single-cast the filter weights, and then spatially accumulate the partial sums across the PE array.

In an example of the no local reuse dataflow from

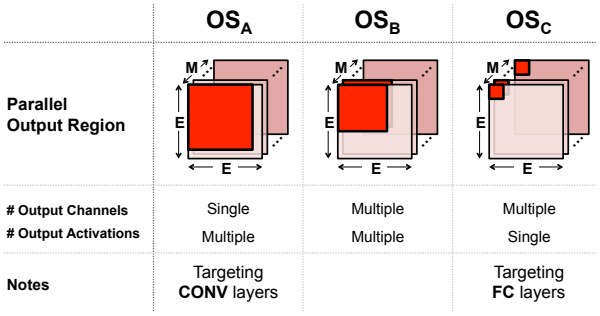
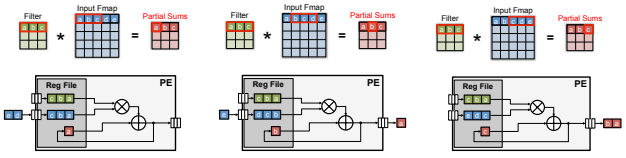


Fig. 23. Variations of output stationary [76].



(a) Step 1 (b) Step 2 (c) Step 3

Fig. 24. 1-D Convolutional reuse within PE for Row Stationary Dataflow [76].

UCLA [87], the filter weights and input activations are read from the global buffer, processed by the MAC units with custom adder trees that can complete the accumulation in a single cycle, and the resulting partial sums or output activations are then put back to the global buffer. Another example is DianNao [88], which also reads input activations and filter weights from the buffer, and processes them through the MAC units with custom adder trees. However, DianNao implements specialized registers to keep the partial sums in the PE array, which helps to further reduce the energy consumption of accessing partial sums. Other examples of no local reuse dataflow are found in [89].

4) Row stationary (RS): A row stationary dataflow is proposed in [76], which aims to maximize the reuse and accumulation at the RF level for *all* types of data (weights, pixels, partial sums) for the overall energy efficiency. This differs from WS or OS dataflows, which optimize for only weights and partial sums, respectively.

The row stationary dataflow assigns the processing of a 1-D row convolution into each PE for processing as shown in Fig. 24. It keeps the row of filter weights stationary inside the RF of PE and then streams the input activations into the PE. The PE does the MACs for each sliding window at a time, which uses just one memory space for the accumulation of partial sums. Since there are overlaps of input activations between different sliding windows, the input activations can then be kept in the RF and get reused. By going through all the sliding windows in the row, it completes the 1-D convolution and maximize the data reuse and local accumulation of data in this row.

With each PE processing a 1-D convolution, we can aggregate multiple PEs to complete the 2-D convolution as shown in Fig. 25. For example, to generate the first row of output activations, three 1-D convolutions are required. Therefore, we can use three PEs in a column, each running

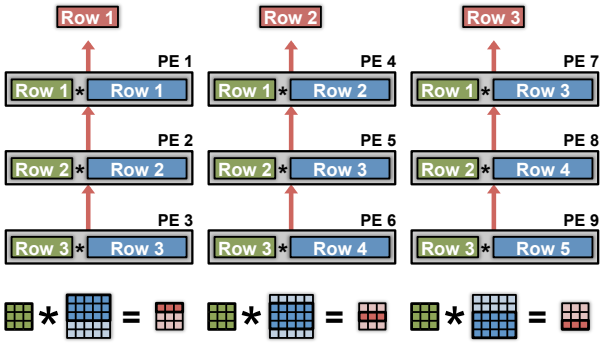


Fig. 25. 2-D convolutional reuse within spatial array for Row Stationary Dataflow [76].

one of the three 1-D convolutions. The partial sums are further accumulated vertically across the three PEs to generate the first output row. To generate the second row of output, we use another column of PEs, where three rows of input activations are shifted down by one row, and use the same rows of filters to perform the three 1-D convolutions. Additional columns of PEs are added until all rows of the output are complete (i.e., the number of columns equals the number of output rows).

This 2-D array of PEs enables other forms of reuse to reduce accesses to the more expensive global buffer. For example, each filter row is reused across multiple PEs horizontally. Each row of input activations is reused across multiple PEs diagonally. And each row of partial sums are further accumulated across the PEs vertically. Therefore, 2-D convolutional data reuse and accumulation are maximized inside the 2-D PE array.

To address the high-dimensional convolution of the CONV layer (i.e., multiple fmaps, filters, and channels), multiple rows can be mapped onto the same PE as shown in Fig. 26. The 2-D convolution is mapped to a set of PEs, and the additional dimensions are handled by interleaving or concatenating the additional data. For filter reuse within the PE, different rows of fmaps are concatenated and run through the same PE as a 1-D convolution. For input fmap reuse within the PE, different filter rows are interleaved and run through the same PE as a 1-D convolution. Finally, to increase local partial sum accumulation across within the PE, filter rows and fmap rows from different channels are interleaved, and run through the same PE as a 1-D convolution. The partial sums from different channels then naturally get accumulated inside the PE. T

The number of filters, channels, and fmaps that can be processed at the same time is programmable, and there exists an optimal mapping for the best energy efficiency, which depends on the shape configuration of the DNN as well as the hardware resources provided, e.g., the number of PEs and the size of the memory in the hierarchy. Since all of the variables are known before runtime, it is possible to build a compiler to perform this optimization off-line to configure the hardware running RS dataflow for different DNNs as shown in Fig. 27.

One example that implements the row stationary dataflow is Eyeriss [90]. It consists of a 14×12 PE array, a 108KB global buffer, ReLU and fmap compression units as shown

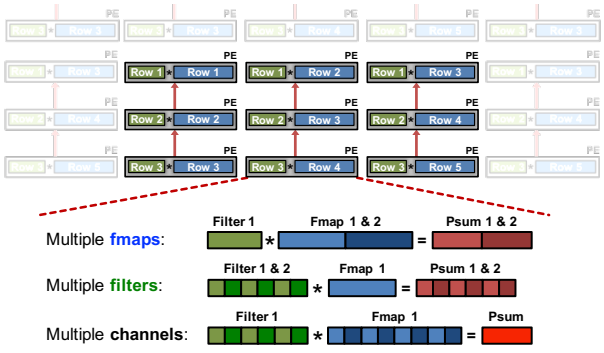


Fig. 26. Multiple rows of different input feature maps, filters and channels are mapped to same PE within array for additional reuse in Row Stationary Dataflow [76].

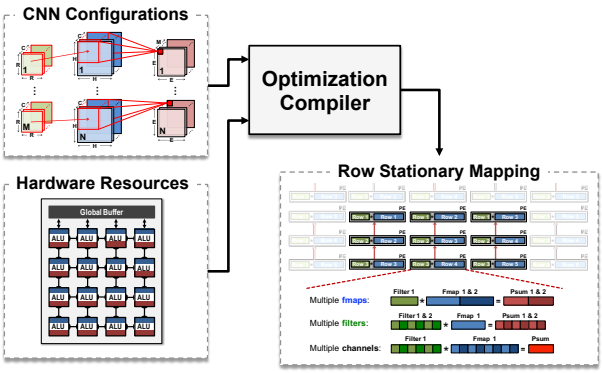


Fig. 27. Mapping optimization takes in hardware and DNNs shape constraint to determine optimal energy dataflow [76].

in Fig. 28. The chip communicates with the off-chip DRAM using a 64-bit bidirectional data bus to fetch data into the global buffer. The global buffer then streams the data into the PE array for processing.

In order to support the RS dataflow, two problems need to be solved in the hardware design. First, how can the fixed-size PE array accommodate different layer shapes? Second, although the data will be passed in a very specific pattern, it still changes with different shape configurations. How can the fixed design achieves passing data in different patterns?

Two mapping strategies are used to solve the first problem as shown in Fig. 29. First, replication can be used to map shapes that do not use up the entire PE array. For example, in the third to fifth layers of AlexNet, each 2-D convolution only uses

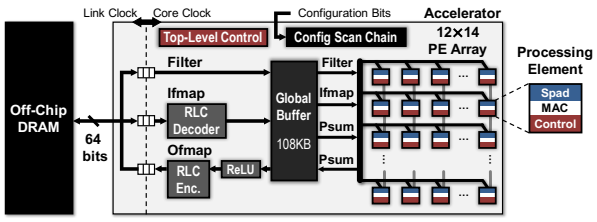


Fig. 28. Eyeriss DNN accelerator [90].

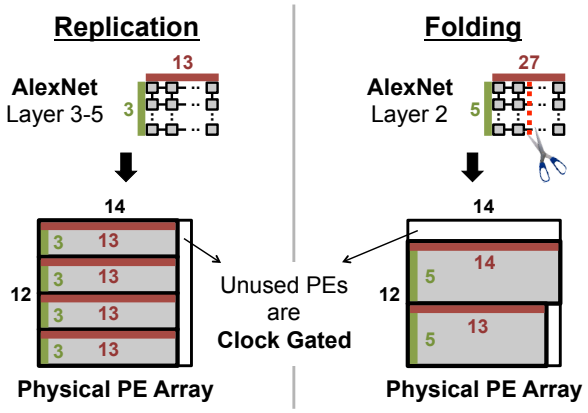


Fig. 29. Mapping uses replication and folding to maximized utilization of PE array [90].

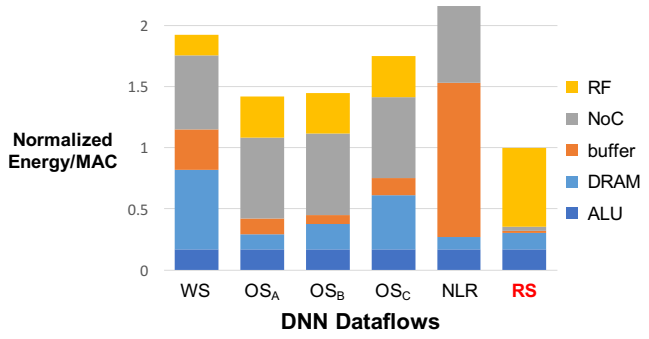
a 13×3 PE array. This structure is then replicated four times, and run different channels and filters in each replication. The second strategy is called folding. For example, in the second layer of AlexNet, it requires a 27×5 PE array to complete the 2-D convolution. In order to fit it into the 14×12 physical PE array, it is folded into two parts, 14×5 and 13×5, and each are vertically mapped into the physical PE array. Since not all PE are used by the mapping, the unused PEs can be clock gated to save energy consumption.

A custom multicast network is used to solve the second problem about flexible data delivery. The simplest way to pass data to multiple destinations is to broadcast the data to all PEs and let each PE decide if it has to process the data or not. However, it is not very energy efficient especially when the size of PE array is large. Instead, a multicast network is used to send data to only the places where it is needed.

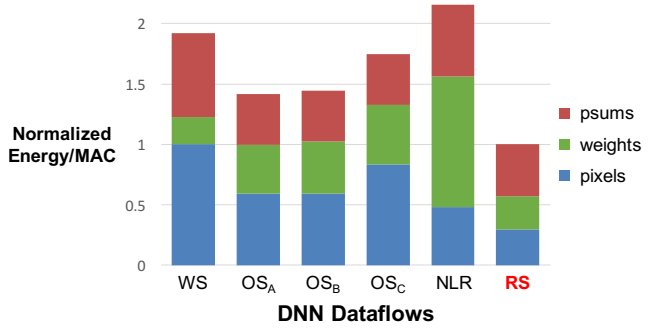
5) Energy comparison of different dataflows: For the evaluation of different dataflows, we use the same total area and number of PEs (256) in a spatial architecture for all dataflows. The local memory (register file) at each processing element (PE) on the order of 0.5 – 1.0kB and a shared memory (global buffer) on the order of 100 – 500kB. The sizes of these memories are selected to be comparable to a typical accelerator for multimedia processing, such as video coding [91]. The memory sizes are further adjusted for the needs of each dataflow under the same area constraint. For example, since the no local reuse dataflow does not require any RF in PE, it is allocated with a much larger global buffer. The simulation uses the layer configurations from AlexNet with a batch size of 16. The simulation also takes into account the fact that accessing different levels of memory hierarchy requires different energy cost.

Fig. 30 compares the chip and DRAM energy consumption of each dataflow for the CONV layers of AlexNet. The WS and OS dataflows have the lowest energy consumption for accessing weights and partial sums, respectively. However, the RS dataflow has the lowest total energy consumption since it optimizes for the overall energy efficiency instead of only for a certain data type.

Fig. 30(a) shows the same results with breakdown in terms of



(a) Energy breakdown across memory hierarchy



(b) Energy breakdown across data type

Fig. 30. Comparison of energy efficiency between different dataflows in the CONV layers of AlexNet [3]: (a) breakdown in terms of storage levels and ALU, (b) breakdown in terms of data types. OS_A, OS_B and OS_C are three variants of the OS dataflow that are commonly seen in different implementations [76].

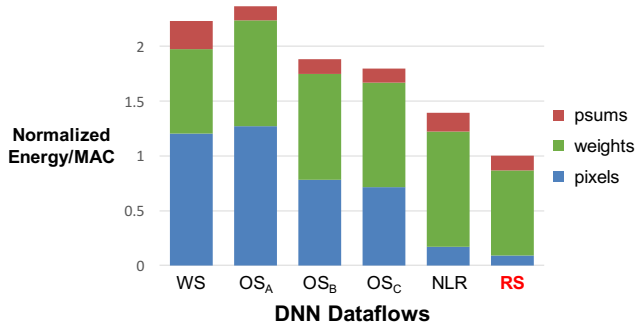


Fig. 31. Comparison of energy efficiency between different dataflows in the FC layers of AlexNet [76].

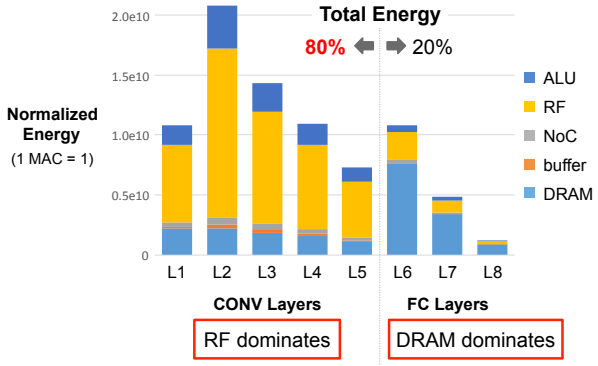


Fig. 32. Energy breakdown across layers of the AlexNet [76]. RF energy dominates in convolutional layers. DRAM energy dominates in the fully connected layer. Convolutional layer dominate energy consumption.

memory hierarchy. The RS dataflow consumes the most energy in the RF, since by design most of the accesses have been moved to the lowest level of the memory hierarchy. This helps to achieve the lowest total energy consumption since RF has the lowest energy per access. The NLR dataflow has the lowest energy consumption at the DRAM level, since it has a much larger global buffer and thus higher on-chip storage capacity compared to others. However, most of the data accesses in the NLR dataflow is from the global buffer, which still has a relatively large energy consumption per access compared to accessing data from RF or inside the PE array. As a result, the overall energy consumption of the NLR dataflow is still farily high. Overall, RS dataflow uses 1.4× to 2.5× lower energy than other dataflows.

Fig. 31 shows the energy efficiency between different dataflows in the FC layers of AlexNet. Since there is not as much data reuse in the FC layers as in the CONV layers, all dataflows spend a significant amount of energy for reading weights. However, RS dataflow still has the lowest energy consumption because it optimizes for the energy of accessing input activations and partial sums. For the OS dataflows, OS_C now consumes lower energy than OS_A since it is designed for the FC layers. Overall, RS still consumes 1.3× lower energy compared to other dataflows at the batch size of 16.

Fig. 32 shows the RS dataflow design with energy breakdown in terms of different layers of AlexNet. In the CONV layers, the energy is mostly consumed in the RF, while in the FC layers, the energy is mostly consumed by DRAM. However, most of the energy is consumed by the CONV layers, which takes around 80% of the energy. As recent DNN models go deeper with more CONV layers, the ratio between number of CONV and FC layers only gets larger. Therefore, moving forward, significant effort should be placed on energy optimizations for CONV layers.

Finally, up until now, we have been looking at architectures with relatively limited storage on the order of a few hundred kilobytes. With much larger storage, on the order of a few megabytes, additional dataflows can be consider such as Fused-Layers which looks at dataflow optimizations across layers [92].

VI. Near-Data Processing

In the previous section, we highlighted that data movement dominates energy consumption. While spatial architectures bring the memory closer to the computation (e.g., into the PE), there have also been efforts to bring the high density memories closer to the computation or integrate the computation into the memory itself. In embedded systems, there have also been efforts to bring the computation right into the sensor where the data is first collected. In this section, we will discuss how data movement can be reduced by moving the processing near the

data using mixed-signal circuit design and advanced memory technologies.

In many of these works, analog processing is needed which has the drawback of increased sensitivity to circuit or device non-idealities. As a result, the computation has be performed at reduced precision; there are however techniques to reduce the precision with minimal impact on accuracy as discussed Section VII. Another factor to take into consideration is that DNNs are often trained in the digital domain; thus for analog processing, there will be an overhead for analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC) that must be accounted for in the overall cost.

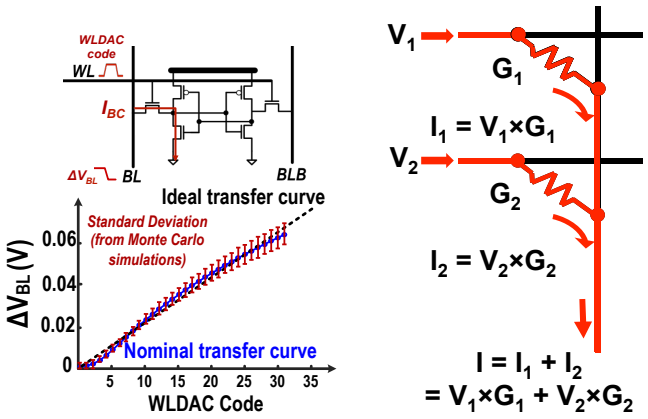
A. DRAM

In recent years, there has been significant research on advanced storage technology to reduce access energy for high density memories, such as DRAMs. For instance, *embedded DRAM (eDRAM)* brings the high density memory on-chip in order to reduce the energy cost of switching off-chip capacitance [93]. eDRAM is 2.85× higher density than SRAM and 321× more energy efficient than DRAM (DDR3). An additional benefit of bringing DRAM on-chip is that it enables a larger number of ports and therefore higher memory bandwidth. The downside of eDRAM is that it often has lower density than off-chip DRAM and can increase the cost of the chip. An example of using eDRAM for DNN processing can be found in DaDianNao [89], which uses 36MB of eDRAM to store the weights for the fully-connected layers.

3-D memory, such as Micron's Hyper Memory Cube (HMC) [94], stacks the DRAM on top of the logic using through silicon vias (TSV); this results in an order of magnitude higher bandwidth and up to 5× reduction in energy consumption relative to existing 2-D DRAMs. There have been several recent works that explore the use of HMC for DNN processing. Neurocube [95] uses HMC with SIMD processors integrated into the logic die of the HMC to bring the computation closer to memory. Tetris [96] explores the use of HMC with the Eyeriss [76] spatial architecture and row stationary dataflow. It proposes allocating more area to the computation than the on-chip memory (i.e., larger PE array and smaller global buffer) in order to exploit the low energy and high throughput properties of the HMC. It also adapts the dataflow to account for the HMC memory and smaller on-chip memory. Tetris achieves a 1.5× reduction in energy consumption and 4.1× increase in throughput over a baseline system with conventional 2-D DRAM.

B. SRAM

The multiply and accumulate operation can be directly integrated into the bit-cell in an SRAM array [97], as shown in Fig. 33(a). A 5-bit DAC is used to drive the word line (WL) to voltage that represent the feature vector, while the bit-cells store the binary weights ±1. The bit-cell current (I_{BC}) is effectively a product of the value of the feature vector and the value of the weight stored in the bit-cell; the currents from the column are added together to discharge the bitline (V_{BL}). This approach gives 12× energy savings over reading the 1-bit weights from



(a) Multiplication performed by bit-cell (Figure from [97])

(b) G_i is conductance of resistive memory (Figure from [99])

Fig. 33. Analog computation by (a) SRAM bit-cell and (b) non-volatile resistive memory.

the SRAM and performing the computation separately. The DAC must account for the non-linear bit-line discharge with respect to the WL voltage. This is considered a weak classifier due to the variations in the bitcell and that only binary weights are used; boosting is needed to combine the weak classifiers to form a strong classifier [98].

C. Non-volatile Resistive Memories

The multiply and accumulate operation can be also directly integrated into advanced *non-volatile* memories by using them as programmable resistive elements, commonly referred to as *memristors* [100]. Specifically, a multiplication is performed with the resistor's conductance as the weight, the voltage as the input, and the current is the output as shown in Fig. 33(b). The addition is done by summing the currents of different memristors with Kirchhoff's current law. This is the ultimate form of a weight stationary dataflow, as the weights are always held in place. The advantages of this approach include reduced energy consumption since computation is embedded within memory which reduces data movement, and increased density since memory and computation can be densely packed with a similar density as DRAM [101][4]

There are several popular candidates for non-volatile resistive memory devices include Phase change memory (PCM), Resistive RAM (RRAM or ReRAM), Conductive bridge RAM (CBRAM), and Spin transfer torque magnetic RAM (STT-MRAM) [102]. These devices have different tradeoffs in terms of endurance (i.e., how many times it can be written), retention time, write current, density (i.e., cell size), variations and speed.

This approach has several drawbacks as described in [103]. First, it suffers from the reduced precision and ADC/DAC overhead of analog processing described earlier. Second, the array size can be limited as the wire dominates energy for array sized of 1k×1k and IR drop along the write can degrade the read accuracy. Third, the writing energy can be costly, in

[4]They can be inserted between the cross-point of two wires and avoids the need for an access transistor.

some cases requiring multiple pulses. Finally, the emerging technologies can also suffer from device-to-device and cycle-to-cycle variations with non-linear conductance across the range.

There have been several recent works that explore the use of memristors for processing in memory for DNNs. ISAAC [99] proposes replacing the eDRAM with memristors. To address the limited precision support, ISAAC proposes computing a 16-bit dot product operation with 8 memristors each storing 2-bits; a 1-bit$\times$2-bit multiplication is performed at each memristor, where a 16-bit input requires 16 cycles to complete. In other words, it is trading off area and time for increased precision. ISAAC arranges its 25.1M memristors in a hierarchical structure to avoid issues with large arrays. PRIME [104] uses memristors to compute the product of a 3-bit input and 4-bit weight with dynamic fixed point to support a 6-bit output. Two memristors can be combined to support 6-bit input and 8-bit weight. The 256$\times$256 memristors array can operate either as a 4-bit multi-level cell computation or a 1-bit single level cell storage. It should be noted that results from ISAAC and PRIME are obtained from simulations.

The ADC overhead can be avoided by training the weights directly in the analog domain. This is demonstrated in [105] using a fabricated 12$\times$12 memristor array that performs a linear classification on a 3$\times$3 binary image to generate three outputs. The weights are stored in a differential form. Including the bias, a total of 60 memristors are used.

D. Sensors

In certain applications, such as image processing, the data movement from the sensor itself can account for a significant portion of the system energy consumption. Thus there has also been work on performing the computation as close as possible to the sensor. In particular, much of the work focuses on moving the computation into the analog domain such that the ADC within the sensor, which accounts for a significant portion of the sensor power, can be avoided. However, as mentioned earlier, lower precision is required for analog computation due to circuit non-idealities.

In [106], the matrix multiplication is integrated into the ADC, where the most significant bits of the multiplications are performed using switch capacitors in an 8-bit successive approximation format. This is extended in [107] to not only perform multiplications, but also the accumulation in the analog domain. It is assumed that 3-bits and 6-bits are sufficient to represent the weights and activations, respectively. This reduces the number of ADC conversions in the sensor by 21$\times$. RedEye [108] takes this approach even further by performing the entire convolution layer (including convolution, max pooling and quantization) in the analog domain at the sensor. It should be noted that [106] and [107] report measured results from fabricated test chips, while results in [108] are from simulations.

It is also feasible to embed the computation not just before the ADC, but into the sensor itself. For instance, in [109] an Angle Sensitive Pixels sensor is used to compute the gradient of the input, which along with compression, reduces the sensor bandwidth by 10$\times$. In addition, since the first layer of the DNN often outputs a gradient-like feature map, it maybe possible to skip the computations in the first layer, which further reduces energy consumption as discussed in [88].

VII. Co-design of DNN models and Hardware

Co-design of the DNN model and the DNN hardware can provide further improvement in processing efficiency. Traditionally, the DNN models were designed to maximize accuracy without much consideration of the implementation complexity. However, this can lead to designs that are challenging to implement and deploy. Co-design of the DNN model and hardware can be effective in jointly maximizing accuracy and throughput, while minimizing energy and cost, which increases the likelihood of adoption. This approach has been demonstrated for other important and widely use multimedia applications such as video compression. Previously, video standards were mostly focused on algorithm development. Going from MPEG-2 to H.264/AVC gave a 2$\times$ improvement in coding efficiency at the cost of 4$\times$ increase in decoder complexity [110]. More recently, the latest video coding standard H.265/HEVC [111] used co-design of algorithms and hardware; as a result, it achieved an additional 2$\times$ improvement in coding efficiency over to H.264/AVC [112] at the cost of only 2$\times$ increase in decoder complexity. In this section, we will highlight various efforts that have been made towards the co-design of DNN models and hardware. Note that unlike Section V, techniques proposed in this section can change the accuracy; although the goal is to minimize the change in accuracy while substantially reducing energy consumption and increasing throughput.

The approaches can be loosely grouped into the following categories:

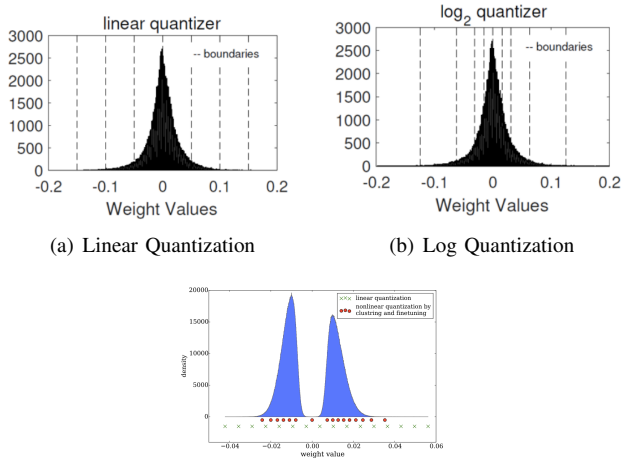
- Reduce precision of operations and operands. This includes going from floating point to fixed point, reducing the bit-width, moving to the logarithmic domain and weight sharing.
- Reduce number of operations and model size. This includes techniques such as compression, pruning and compact network architectures.

A. Reduce Precision

Quantization involves mapping data to a smaller set of quantization levels. The ultimate goal is to minimize the error between the reconstructed data from the quantization levels and the original data.

The number of quantization level reflects the *precision* and ultimately the number of bits (usually log_2 of the number of levels); thus, *reduced precision* refers to reducing the number of levels, and thus the number of bits, used to represent the data. Benefits of reduced precision include reduced storage cost and/or reduced computation requirements.

There are several ways to map the data to the quantization levels. The simplest method is a linear mapping with uniform distance between each quantization level (Fig. 34(a)). Another approach is to use a simple function such as a *log function* (Fig. 34(b)) where the distance between the levels varies; this often can be implemented with simple logic such as a shift. Finally, a more complex mapping function can be used where



(a) Linear Quantization (b) Log Quantization

(c) Non-Linear Quantization

Fig. 34. Various methods of quantization. (Figures from [113, 114])

the quantization levels are determined or learned from the data (Fig. 34(c)), e.g., using k-means clustering; for this approach, the mapping is usually implemented with a look up table.

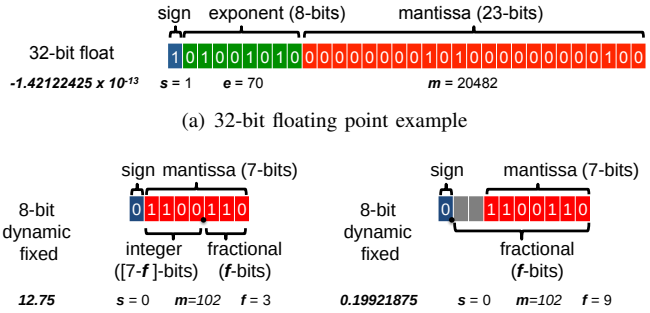
Finally, the quantization can be fixed (i.e., the same method of quantization for all data types and layers, filters, and channels in the network); or it can be variable (i.e., different methods of quantization can be used for weights and activations, and different layers, filters, and channels in the network).

We will now walk through the various forms of quantization that has been explored in recent works for improving the efficiency of DNNs. We will highlight their impact on storage and computation cost as well as their impact on performance accuracy.

32-bit floating point is commonly used on platforms such as GPUs and CPUs, and has a wide dynamic range from 10^{-38} to 10^{38}, which is more than sufficient for both weights and activations in the current state-of-the-art DNN models. While a wide dynamic range can be beneficial for accuracy, it requires high energy and area cost; thus, recent works have investigated reducing the numerical precision (i.e., quantization) in order to reduce the computation and storage cost. For instance, using 8-bit fixed point with a dynamic range of 0 to 127 has the following impact [75]:

- An 8-bit fixed point adder consumes 3.3× less energy (3.8× less area) than a 32-bit fixed point adder, and 30× less energy (116× less area) a 32-bit floating point adder. The energy and area of a fixed-point adder scales approximately linearly with the number of bits.
- An 8-bit fixed point multiply consumes 15.5× less energy (12.4× less area) than a 32-bit fixed point multiply, and 18.5× less energy (27.5× less area) than a 32-bit floating point multiply. The energy and area of a fixed-point multiply scales approximately quadratically with the number of bits.

Reducing the precision also reduces the energy and area cost for storage. The energy cost of reading from and writing to memory (i.e., memory access) is often greater than the computation itself. For instance, reading a 32-bit value from an



(a) 32-bit floating point example

(b) 8-bit dynamic fixed point examples

Fig. 35. Various methods of number representations.

8kB SRAM requires 1.35× and 5.55× more energy than a 32-bit floating-point multiplication and addition, respectively [75]. The memory access energy also increases for larger capacity memories due to the switching capacitance of the bit lines and word lines. Finally, very large capacity memories, in the gigabytes range, are often placed off-chip in DRAM, which increases the energy by over two orders of magnitude. Note that changing from floating point to fixed point, without reducing bitwidth, does not reduce the energy or area cost of the memory.

Most of the recent works focus on reducing the precision of the weights rather than the activations (with some exceptions [115]), since weights directly increase the storage capacity requirement, while the impact of activations on storage capacity depends on the network architecture and dataflow. Most of the recent works also focus on reducing the precision for the inference rather than training (with some exceptions [84, 116, 117]) due to the sensitivity of the gradients to quantization. Various techniques used to reduce precision are summarized in Table III.

1) Linear quantization: The first step of reducing precision is usually to convert values and operations from floating point to fixed point. A 32-bit floating point number, as shown in Fig. 35(a), is represented by $(-1)^s \times m \times 2^{(e-127)}$, where s is the sign bit, e is the 8-bit exponent, and m is the 23-bit mantissa, and covers the range of 10^{-38} to 10^{38}.

An N-bit fixed point number is represented by $(-1)^s \times m \times 2^{-f}$, where s is the sign bit, m is the (N-1)-bit mantissa, and f determines the location of the decimal point and acts as a scale factor. For instance, for an 8-bit integer, when $f = 0$, the dynamic range is -128 to 127, whereas when $f = 10$, the dynamic range is -0.125 to 0.124023438. *Dynamic* fixed point representation allows f to vary based on the desired dynamic range as shown in Fig. 35(b). This is useful for DNNs, since the dynamic range of the weights and activations can be quite different. In addition, the dynamic range can also vary across layers and layer types (e.g., convolutional vs. fully connected). Using dynamic fixed point, the bitwidth can be reduced to 8 bits for the weights and 10 bits for the activations without any fine-tuning of the weights [118]; with fine-tuning, both weights and activations can reach 8-bits [119].

To guarantee no precision loss in a fixed-point multiply and accumulate (MAC) operation, weights and input activations with N-bit fixed-point precision would require an N-bit×N-bit

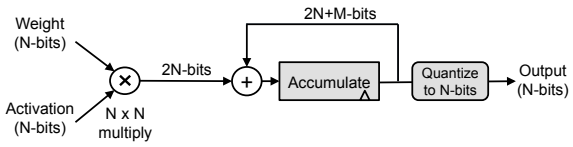


Fig. 36. Reducing the precision of multiply and accumulate (MAC).

multiplication which generates a 2N-bit output product; that output would be accumulated with 2N+M-bit precision, where M is determined based on the largest filter size $log_2(C \times R \times S$ from Fig. 6(b)), which is in the range of 10 to 16 bits for the popular DNNs described in Section III-A. After accumulation, the precision of the final output activation is typically reduced to N-bits [84, 118], as shown in Fig. 36, without significant impact on accuracy. This is done based on the assumption that distribution of the weights and activations are centered near zero such that the accumulation would not move only in one direction; this is particularly true when batch normalization is used.

The reduction in bitwidths is not only done in research, but has also impacted recent commercial platforms for DNN processing. For instance, Google's Tensor Processing Unit (TPU) which was announced in May 2016, was designed for 8-bit integer arithmetic [120]. Similarly, Nvidia's PASCAL GPU, which was announced in April 2016, also has 8-bit integer instructions for deep learning inference [121]. In general purpose platforms such as CPUs and GPUs, the main benefit of using 8-bit computation is an increase in throughput, as four 8-bit operations rather than one 32-bit operation can be performed for a given clock cycle.

While general purpose platforms usually support 8-bit, 16-bit and/or 32-bit operations, it has been shown that the minimum bit precision for DNNs can actually vary in a more fine grained manner. For instance, the weight precision can vary between 4 and 10 bits for AlexNet across different layers without significant impact to accuracy (i.e., a change of less than 1%) [122, 123]. This fine-grained variation can be exploited for increased throughput or reduced energy consumption with specialized hardware. For instance, if bit-serial processing is used, where the number of clock cycles to complete an operation is proportional to the bitwidth, adapting to fine-grain variations in bit precision of the weights can result in a 2.24× speed up versus 16-bits [124]. Alternatively, a multiplier can be designed such that its critical path reduces based on the bit precision as fewer adders are needed to resolve the product; this can be combined with voltage scaling for a 2.56× energy savings versus 16-bits [125]. While these bit scaling results are reported relative to 16-bit, it would be interesting to see their impact relative to the maximum precision required across layers (e.g., 9-bits for [124] and [125]).

The bit precision can be reduced even more aggressively to binary precision; this area of research is often referred to as binary nets. BinaryConnect (BC) [126] introduced the concept of binary weights (i.e., -1 and 1), where using a binary weight reduced the multiplication in the MAC to addition and subtraction only. This was later extended in Binarized Neural Networks (BNN) [127] that uses binary weights *and* activations, which reduces the MAC to an XNOR. However, BC and BNN have an accuracy loss of 19% and 29.8% for AlexNet, respectively, relative to using 32-bit floating point for top-5 error on ImageNet [128].

Various approaches were introduced in Binary Weight Nets (BWN) and XNOR-nets to reduce the accuracy loss [128]. This included multiplying the outputs with a scale factor to recover the dynamic range (i.e., the weights were effectively -w and w, where w is the l_1-norm of the weights in the filter), keep the first and last layers a 32-bit floating point precision, and perform normalization before convolution. With these changes, BWN reduces the accuracy loss for AlexNet to 0.8%, while XNOR-Nets reduces the loss to 11%. This can also be thought of as a form of weights sharing, to be discussed next in Section VII-A2, where only two weights are used per layer. Alternatively, Quantized Neural Networks (QNN) [116] and DoReFaNet [117] allow the activations to have 2-bits, while the weights remain at 1-bit; in QNN, this reduces the accuracy loss to 6.5%.

Most recently, the use of Ternary Weight Nets (TWN) has been proposed, which allows the weights to also take on a value of zero (i.e., -w, 0, w) [129]. This requires an additional bit compared to binary weights; however, since some weights are zero, the sparsity can be exploited for reducing computation and storage, which can potentially cancel out the cost. TWN has a 3.7% accuracy loss compared to 32-bit floating point precision. Trained Ternary Quantization (TTQ) proposes using different trained scales for each weight (i.e., -w_1, 0, w_2), which reduces the accuracy loss for AlexNet to 0.6% [130].

2) Non-linear quantization: The previous work described involves linear quantization where the levels are uniformly spaced out. It has been shown that the distribution of the weights and activations are not uniform [114, 115], and thus a non-linear quantization can potentially improve accuracy. Specifically, there have been two popular approaches taken in recent works: (1) log domain quantization; (2) learned quantization or weight sharing.

Log domain quantization If a logarithmic distribution is assumed, the values are more equally distributed across levels as shown in Fig 34(b), which can result in more effective use of each level. For instance, using 4 bits in linear quantization results in a 27.8% loss in accuracy versus 5% loss for log base-2 quantization on VGG-16 [113]. Furthermore, the weights and/or activations can be quantized to powers of two and the multiplication can be replaced with a bit-shift [115, 119].[5] The accuracy can also be improved by dividing the large and small weights into different groups and iteratively quantizing and re-training the weights as demonstrated in Incremental Network Quantization (INQ) [131].

Weight Sharing forces several weights to share a single value. This reduces the number of unique weights. One example is to group weights by using a hashing function and use one value for each group [132]. The weights can also be grouped by the k-means algorithm [114]. Both the shared weights and an

[5]Although multiplications do not account for significant portion of the total energy.

Reduce Precision Method		Bitwidth		Accuracy loss vs. 32-bit float (%)
		Weights	Activations	
Dynamic Fixed Point	**w/o fine-tuning [118]**	8	10	0.4
	w/ fine-tuning [119]	8	8	0.6
Reduce weight	**Ternary Weight Networks (TWN) [129]**	2*	32 (float)	3.7
	Trained Ternary Quantization (TTQ) [130]	2*	32 (float)	0.6
	BinaryConnect [126]	1	32 (float)	19.2
	Binary Weight Network (BWN) [128]	1*	32 (float)	0.8
Reduce weight and activation	**Quantized Neural Networks (QNN) [116]**	1	2*	6.5
	Binarized Neural Networks (BNN) [127]	1	1	29.8
	XNOR-net [128]	1*	1	11
Non-linear Quantization	**Incremental Network Quantization (INQ) [131]**	5	32 (float)	-0.2
	LogNet [115]	5 (conv), 4 (fc)	4	3.2
	Deep Compression [114]	8 (conv), 4 (fc)	16	0
		4 (conv), 2 (fc)	16	2.6

TABLE III
METHODS TO REDUCE NUMERICAL PRECISION FOR ALEXNET. ACCURACY MEASURED FOR TOP-5 ERROR ON IMAGENET. *NOT APPLIED TO FIRST AND/OR LAST LAYERS

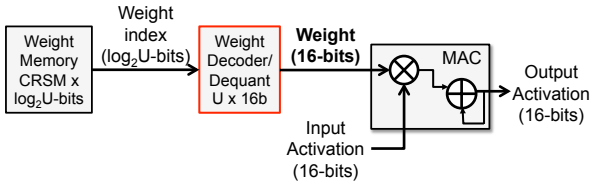
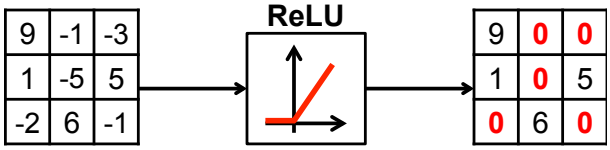
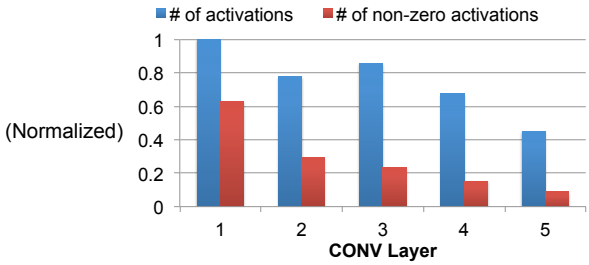


Fig. 37. Weight sharing hardware.



(a) ReLU non-linearity



(b) Distribution of activation after ReLU of AlexNet

Fig. 38. Sparsity in activations due to ReLU.

index indicating which weight to use at each position of the filter are stored. This leads to a two step process to fetch the weight: (1) read the weight index; (2) using the weight index, read the shared weights. This approach can reduce the cost of reading and storing the weights if the weight index (log_2 of the number of unique weights) is less than the bitwidth of the weight itself.

For instance, in Deep Compression [114], the number of unique weights per layer is reduced to 256 for convolutional layers and 16 for fully-connected layers in AlexNet; as a result, the 8-bit and 4-bits weight indexes, respectively, require less storage than the 16-bit shared weights. Assuming there are U unique weights and the size of the filters in the layer is C×R×S×M from Fig. 6(b), there will be energy savings if reading from a $CRSM \times log_2 U$-bit memory plus a U×16-bit memory (as shown in Fig. 37) cost less than reading from a $CRSM$×16-bit memory. Note that unlike the previous quantization methods, the weight sharing approach does not reduce the precision of the MAC computation itself and only reduces the weight storage requirement.

B. Reduce Number of Operations and Model Size

There is on-going research on reducing the number of operations and model size as well. They can loosely be classified into exploiting activation statistics, network pruning, network architecture design and knowledge distillation.

1) Exploiting Activation Statistics: The ReLU non-linearity sets all negative values to zero as shown in Fig. 38(a). As a result, the output activations of the feature maps after the ReLU are sparse as shown in Fig. 38(b), where we see sparsity of 19% to 63% for AlexNet. This sparsity gives ReLU an implementation advantage over non-linearities such as sigmoid, etc.

We can exploit the sparsity for energy and area savings using compression, particularly off-chip DRAM access which is expensive. With a simple run length coding that involves signaling non-zero values of 16-bits and then runs of zeros up to 32, we can reduce the external memory bandwidth of the activations by 2.1× [58]. For the overall bandwidth, including weights, we get 1.5× reduction. This simple run length compression is within 5-10% of the theoretical entropy limit.

In addition to compression, the hardware can also be modified such that it skips reading the weights and performing the MAC for zero valued activations. This can reduce energy cost by 45% [90]. Rather than just gating the read and MAC computation, the hardware could also skip the cycle to increase the throughput by 1.37× [133].

The activations can be made to be even more sparse by pruning the low valued activations. For instance, if all activations with small values are pruned, this can be translated into an additional 11% speed up [133] or 2× power reduction [134] with little impact on accuracy. Aggressively pruning more activations can provide additional throughput improvement at a cost of reduced accuracy.

2) Network Pruning: To make network training easier, the networks are usually over-parameterized. Therefore, a large amount of weights in a network are redundant and can be removed or set to zero. This process is called network pruning. Aggressive network pruning often requires some fine-tuning of the weights to maintain the original accuracy. This was first proposed in 1989 through a technique called optimal brain damage [135]. The idea was to compute the impact of each weight on the training loss (discussed in Section II-C), referred to as the weight saliencies. The low-saliency weights were removed and the remaining weights were fine-tuned; this process was repeated until the desired weight reduction and accuracy were reached.

In 2015, a similar idea was applied to modern DNNs in [136]. Rather than using the saliency as a metric, which is too difficult to compute for the large-scaled DNNs, the pruning was simply based on the magnitude of the weights. Small weights were pruned and the model was fine-tuned to restore the accuracy. Without fine-tuning the weights, about 50% of the weights can be pruned. With fine-tuning, over 80% of the weights are pruned. Overall this approach can reduce the number of weights in AlexNet by 9× and the number of MACs by 3×. Most of the weight reduction comes from the fully-connected layers (9.9× for fully-connected layers versus 2.7× for convolutional layers).

However, the number of weights alone is not a good metric for energy. For instance, in AlexNet, the number of weights in the fully-connected layer is much larger than in the convolutional layer; however, the energy of the convolutional layer is much higher than the fully-connected layer [76]. Rather than using the number of weights and MAC operations as proxies for energy, the pruning of the weights can be directly driven by energy itself [137]. An energy evaluation method can be used to estimate the DNN energy and account for the data movement as shown in Fig. 39; this energy estimation tool is available at [138]. The resulting energy values for popular DNN models are shown in Fig. 40(a). Energy-aware pruning can then be used to prune weights based on energy to reduce the overall energy across all layers by 3.7× for AlexNet, which is 1.74× more efficient than magnitude-based approaches [136] as shown in Fig. 40(b). As mentioned previously, it is well known that AlexNet is over-parameterized. The energy-aware pruning can also be applied to GoogleNet, which is already a small DNN model, for a 1.6× energy reduction.

Custom hardware is needed to support the efficient processing of sparse weights. As mentioned previously, the DNN processing can be represented as a matrix-vector multiplication, as shown in Fig. 15(a), where the matrix is composed of the weights and the vector is composed of the input activations. For convolutions, a Toeplitz matrix is used for the weights. This sparse weight matrix should be stored in a compressed format; the compression can be applied either in row or column order. A compressed sparse row (CSR) format, as shown in Fig. 41(a), is often used to perform Sparse Matrix-Vector multiplication. However, the input vector needs to be read in multiple times even though only a subset of it is used since each row of the matrix is sparse. Alternatively, a compressed sparse column (CSC) format, as shown in Fig. 41(b), can be used, where

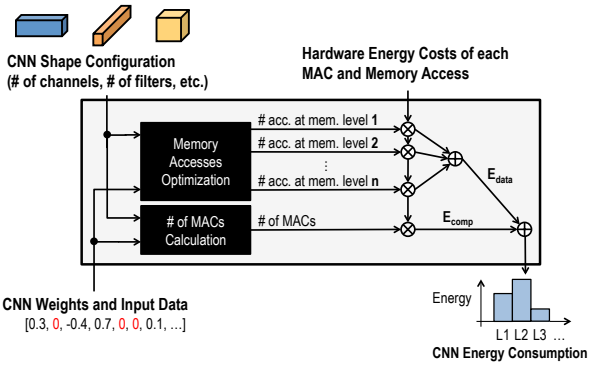
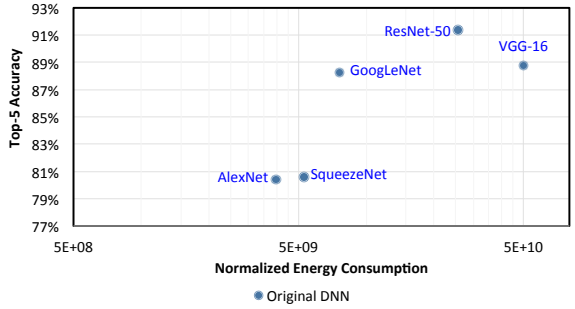
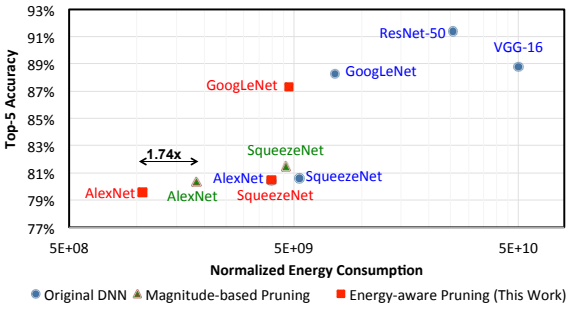


Fig. 39. Energy estimation methodology [137].



(a) Energy versus accuracy trade-off of popular DNN models.

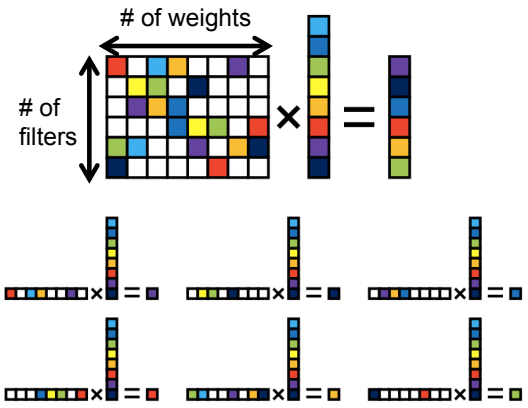


(b) Impact of energy-aware pruning.

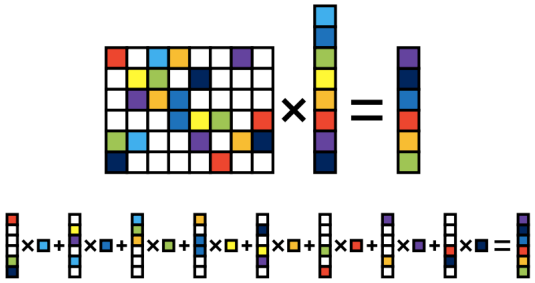
Fig. 40. Energy values estimated with methodology in [137].

the output is updated several times, and only one element of the input vector is read at a time [139]. The CSC format will provide an overall lower memory bandwidth than CSR if the output is smaller than the input, or in the case of DNN, if the number of filters is *not* significantly larger than the number of weights in the filter ($C \times R \times S$ from Fig. 6(b)). Since this is often true, CSC can be an effective format for sparse DNN processing.

EIE [140] demonstrates the sparse matrix-vector multiplication specifically for DNNs. It stores weights column-wise in a run-length format (non-zero weights followed by run-length of zeros; the start location of each column needs to also be stored since it is variable length). When the input is not zero, the column is read and the output is updated. To handle the sparsity, additional logic must keep track of the location which output should be updated.



(a) Compressed sparse row (CSR)



(b) Compressed sparse column (CSC)

Fig. 41. Storage format for sparse matrix-vector multiplications (Figure from [139]).

Similar to compressing the sparse activations discussed in Section VII-B1, the sparse weights after pruning can also be compressed to reduce memory access bandwidth. For instance, Huffman coding reduces storage and bandwidth requirements for weights by 20 to 30% [114].

3) Compact Network Architectures: The number of weights and operations can be reduced by improving the network architecture itself. The trend is to replace a large convolutional layer with a series of smaller convolutional layers, which have fewer weights in total, such that overall they have the same effective receptive field (i.e., the region the filter uses from input image to compute an output). This can be achieved in the architecture design phase (before training) or through decomposing filters in a trained network (after training). The latter one can take advantage of the trained networks and avoid the hassle of training networks from scratch. However, it is less flexible than the former one. For example, existing methods can only decompose a layer in a trained network into a series of layers without non-linear layers between them.

a) Before Training: In recent DNNs, filters with a smaller width and height are used more frequently because concatenating several of them can emulate a larger filter as shown in Fig. 10. For example, one 5×5 convolution can be replaced with two 3×3 convolutions. Alternatively, one N×N convolution can be decomposed into two 1-D convolutions, one 1×N and one N×1 convolution [50]; this basically imposes a restriction that the 2-D filter must be separable, which is a common constraint in image processing [141]. However, this decomposition only works well for layers whose feature maps have the width and height ranging from 12 to 20. Similarly, a 3-D convolution can be replaced by a set of 2-D convolutions (i.e., applying only on one of the input channels) followed by 1×1 3-D convolutions [142]. The order of the 2-D convolutions and 1×1 3-D convolutions can be switched.

1×1 convolutional layers can also be used to reduce the number of filter channel in the next layer, by reducing the number of input channels next layer with relatively smaller computation cost as demonstrated in [11, 48, 49]; this is also referred to a 'bottleneck' as discussed in Section III-A. For this purpose, the number of 1×1 filters has to be less than the number of channels in the 1×1 filter. For example, 32 filters of 1×1×64 can transform an input with 64 channels to an output of 32 channels and reduce the number of filter channels in the next layer to 32. SqueezeNet uses many 1×1 to aggressively reduce the number of weights [143]. It proposes a *fire* module that first squeezes the network with the 1×1 convolution filters and then expands it with multiple 1×1 and 3×3 convolution filters. It achieves an overall 50× reduction in number of weights compared to AlexNet, while maintaining the same accuracy. It should be noted, however, that reducing the number of weights does not necessarily reduce energy; for instance, SqueezeNet consumes more energy than AlexNet, as shown in Fig. 40(a).

b) After Training: Tensor decomposition can be used to decompose filters in a trained network without impacting the accuracy. It treats weights in a layer as a 4-D tensor and breaks it into a combination of smaller tensors (i.e., several layers). Low-rank approximation can then be applied to further increase the compression rate at the cost of accuracy degradation, which can be restored by network fine-tuning.

This approach is demonstrated using Canonical Polyadic (CP) decomposition, a high-order extension of singular value decompositiion that can be solved by various methods, such as a greedy algorithm [144] or a non-linear least-square method [145]. Combining CP-decomposition with low-rank approximation achieves 4.5× speed-up on CPUs [145]. However, CP-decomposition cannot be computed in a numerically stable way when the dimension of the tensor, which represents the weights, is larger than two [145]. To alleviate this problem, Tucker decomposition is adopted instead in [146].

4) Knowledge Distillation: Using a deep network or averaging the predictions of different models (i.e. ensemble) gives a better accuracy than using a single shallower network. However, the computational complexity is also higher. To get the best of both worlds, knowledge distillation transfers the knowledge learned by the complex model (teacher) to the simpler model (student). The student network can therefore achieve the accuracy unachievable by training it with the same dataset directly [147, 148]. For example, the speech recognition accuracy of the student net is improved by 2% by using knowledge distillation, and it is close to the accuracy of the teacher net, which is an ensemble of 10 networks with the same architecture as the student net [149].

Fig. 42 shows the simplest knowledge distillation method [147]. The softmax layer is commonly used as the output layer in the image recognition networks to generate the

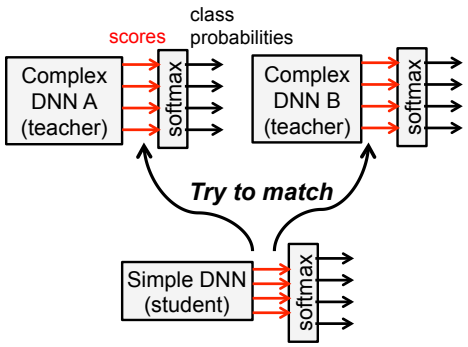


Fig. 42. Knowledge distillation to match class scores of a small DNN to ensemble of large DNNs.

class probabilities from the class scores; it squashes the class scores into values between 0 and 1 that sum up to 1. For this knowledge distillation method, the class scores of the teacher DNN (or an ensemble of teacher DNNs) are used as the soft targets, and the objective is to minimize the squared difference between the soft targets and the class scores of the student DNN. The reason for using the class scores as the soft targets instead of the class probabilities is that the small values in the soft targets contain much of the information. These small values become almost zero after applying softmax. Alternatively, a more general way is to use the class probabilities as the soft target by making the softmax layer generate softer class probabilities [149]. Finally, the intermediate representations of the teacher DNN can also be incorporated as the extra hints to train the student DNN [150].

VIII. Benchmarking Metrics for DNN Evaluation and Comparison

In recent years, there has been a significant amount of research on efficient processing of DNNs. We should consider several key metrics to compare the various strengths and weaknesses of different designs and proposed techniques. These metrics should cover important attributes such as accuracy/robustness, power/energy consumption, throughput/latency and cost. Reporting all these metrics is important in order to provide a complete picture of the trade-offs made by a proposed design or technique. We have prepared a website to collect these metrics from various publications [151].

In terms of *accuracy* and *robustness*, it is important that the accuracy be reported on widely-accepted datasets as discussed in Section IV. The difficulty of the dataset should be considered when measuring the accuracy. For instance, the MNIST dataset for digit recognition is significantly easlier than the ImageNet dataset. As a result, a DNN that performs well on MNIST may not necessarily perform well on ImageNet. Thus it is important that the same dataset and task is used when comparing accuracies of different DNN models; currently ImageNet is preferred since it presents a challenge for DNNs, as opposed to MNIST, which can also be addressed with simple non-DNN techniques. To demonstrate primarily hardware innovations, it would be desirable to report results for widely-used DNN models (e.g., AlexNet, GoogLeNet) whose accuracy and robustness have been well studied and tested.

Power and *energy* are important when considering processing both in the cloud and in embedded devices that have stringent power ceiling or limited battery capacity, respectively. Energy-efficiency is necessary for battery-operated devices such as smart phones, smart sensors, UAVs, and wearables. Local processing on battery-operated devices is preferred over the cloud for certain applications due to latency, privacy or communication bandwidth limitations. Low power dissipation is also desirable for processing in vehicles and data centers to reduce cooling costs. It is also important to not only address the power and energy consumption of the chip, but also external memory accesses which contribute significantly to the system power.

High-throughput is necessary to deliver real-time performance for interactive applications such as navigation and robotics. For data analytics, high-throughput means that more data can be analyzed in a given amount of time. As the amount of visual data is growing exponentially, high-throughput big data analytics becomes important, particularly if an action needs to be taken based on the analysis (e.g., security or terrorist prevention; medical diagnosis).

Low latency is necessary for real-time interactive applications. Latency measures the time between when the pixel arrives to a system and when the result is generated. Latency is measured in terms of seconds, while throughput is measured in operations/second. Often high throughput is obtained by batching multiple images/frames together for processing; this results in multiple frame latency (e.g., at 30 frames per second, a batch of 100 frames results in a 3 second delay). This delay is not acceptable for real-time applications, such as high-speed navigation where it would reduce the time available for course correction.

Hardware cost is in large part dictated by the amount of on-chip storage and the number of cores. Typical embedded processors have limited on-chip storage on the order of a few hundred kilobytes. Since there is a trade-off between the amount of on-chip memory and the external memory bandwidth, both metrics should be reported. Similarly, there is a correlation between the number of cores and the throughput. In addition, while many cores can be built on a chip, the number of cores that can actually be used at a given time should be reported. It is often unrealistic to assume peak utilization and performance due to limitations of mapping and memory bandwidth. Accordingly, the power and throughput should be reported for running actual DNNs as opposed to only reporting theoretical limits.

A. Metrics for DNN Models

To evaluate the properties of a given DNN model, we should consider the following elements:

- The accuracy of the model in terms of the top-5 error on datasets such as ImageNet. Also, what type of data augmentation that was used (e.g., multiple crops, ensemble models).
- For the DNN model, either a well known model should be used, or the parameters of the model should be reported,

Metrics	AlexNet		GoogLeNet v1	
	dense	sparse	dense	sparse
Top-5 error	19.6	20.4	11.7	12.7
Number of CONV Layers	5	5	57	57
Depth in (Number of CONV Layers)	5	5	21	21
Filter Sizes	3,5,11		1,3,5,7	
Number of Channels	3-256		3-832	
Number of Filters	96-384		16-384	
Stride	1,4		1,2	
NZ Weights	2.3M	351k	6.0M	1.5M
NZ MACs	395M	56.4M	806M	220M
FC Layers	3	3	1	1
Filter Sizes	1,6		1	
Number of Channels	256-4096		1024	
Number of Filters	1000-4096		1000	
NZ Weights	58.6M	5.4M	1M	870k
NZ MACs	14.5M	1.9M	635k	663k
Total NZ Weights	61M	5.7M	7M	2.4M
Total NZ MACs	410M	58.3M	806M	221M

TABLE IV
METRICS FOR POPULAR DNN MODELS. SPARSITY IS ACCOUNT FOR BY REPORTING NON-ZERO (NZ) WEIGHTS AND MACS.

including number of layers, filter sizes, number of filters and number of channels.
- The number of weights impact the storage requirement of the model and should be reported. If possible, the number of non-zero weights should be reported since this reflects the theoretical minimum storage requirements.
- The number of MACs that needs to be performed should be reported as it is somewhat indicative of the number of operations and throughput of the given DNN. If possible, the number of non-zero MAC should also be reported since this reflects the theoretical minimum compute requirements.

Table IV shows how these metrics are reported for various well known DNNs. The accuracy is reported for the case where only a single crop for a single model is used for classification, such that the number of weights and MACs in the table are consistent.[6] Note that accounting for number of non-zero (NZ) operations significantly reduces the number of MACs and weights. Since the number of NZ MACs relies on input, we propose using the publicly available 50,000 validation images from ImageNet for the computation. Finally, there are various methods to reduce the weights in a DNN (e.g., pruning). Table IV reports the metrics for sparse DNNs pruned with [137], which gives a significant reduction in the number of NZ weights and MACs.

B. Metrics for DNN Hardware

To measure the efficiency of the DNN hardware, we consider several metrics:

- The energy-efficiency of the design in terms of energy per non-zero MAC (non-zero weights and activations) in conjunction with the bitwidth of the MACs.
- The off-chip bandwidth (e.g., DRAM bandwidth) should be reported in terms of off-chip access per non-zero MAC (non-zero weights and activations) in conjunction with the bitwidth of the MACs.
- The area efficiency measures the cost of the chip and accounts for the size and type of memory (e.g., registers or SRAM) and amount of control logic. It should be reported in terms of the core area in squared millimeters per multiplier along with process technology.
- The throughput should be reported based on run time for various DNN models in order to account for mapping and memory bandwidth effects. This provides a more useful and informative metric than peak throughput.

Each processor should report its specifications as shown in Table V for the Eyeriss chip [58]. In addition, it should be reported whether the results are measured or obtained from simulation. If obtained from simulation, it should be clarified whether it is from synthesis or post place and route and what library corner was used.

In addition, for each DNN model used to benchmark the processor, the following should be reported: the batch size (which affects off-chip access), the number of bits per operand, the energy per non-zero MAC, the off-chip access per non-zero MAC, the run time and the power consumption.

Finally, different platforms will have different implementation-specific metrics. For instance, for an FPGA, the specific device should be reported, along with the utilization of resources such as DSP, BRAM, LUT and FF; performance density such as GOPs/slice can also be reported.

IX. SUMMARY

The use of deep neural networks (DNNs) has seen explosive growth in the past few years. They are currently widely used for many artificial intelligence (AI) applications including computer vision, speech recognition and robotics and are often delivering better than human accuracy. However, while DNNs can deliver this outstanding accuracy, it comes at the cost of high computational complexity. Consequently, techniques that enable efficient processing of deep neural network to improve *energy-efficiency* and *throughput* without sacrificing *accuracy* with cost-effective hardware are critical to expanding the the deployment of DNNs in both existing and new domains.

Creating an system for efficient DNN processing should begin with understanding the current and future applications and the specific computations required both now and the potential evolution of those computations. This article surveys a number of the current applications, focusing on computer vision applications, the associated algorithms, and the data being used to drive the algorithms. These applications, algorithms and input data are experiencing rapid change. So extrapolating these trends to determine the degree of flexibility desired to handle next generation computations, thus, become an important ingredient of any design project.

During the design-space exploration process, it is critical to understand and balance the important system metrics. For DNN computation these include the accuracy, energy, throughput and hardware cost. Evaluating these metrics is, of course, key,

[6]Often to increase accuracy, multiple crops of an image are used to account for misalignment; in addition, an ensemble of multiple models can be used where each model has different weights due to different training settings, such as using different initializations or datasets, or even different architectures. If multiple crops and models are used, then the number of MACs and weights required would increase.

Metrics	Eyeriss	
Process Technology	65nm LP TSMC (1.0V)	
Core area (mm^2) per multiplier	0.073	
On-chip memory per multiplier	1.14 kB	
Measured or Simulated	Measured	
If Simulated, Syn or PnR	n/a	
DNN Model	AlexNet	VGG-16
Number of Images Tested	100	100
Dense/Sparse	Dense	Dense
Supported Layers	CONV1, CONV2, CONV3, CONV4, CONV5	CONV1-1, CONV1-2, CONV2-1, CONV2-2, CONV3-1, CONV3-2, CONV3-3, CONV4-1, CONV4-2, CONV4-3, CONV5-1. CONV5-2, CONV5-3
Batch Size	4	3
Bits per Weight	16	16
Bits per Input Activation	16	16
Energy per non-zero MAC (pJ)	21.7	52.0
Off-chip accesses per non-zero MAC (Bytes)	0.01	0.016
Run Time (msec)	115.3	4309.4
Power (mW)	278	236

TABLE V
EXAMPLE BENCHMARK METRICS FOR EYERISS [90].

so this article surveys the important components of a DNN workload. In specific, a DNN workload consists of the form of each DNN network including the "shape" of each layer and the interconnections between layers and also the data input to the DNN for inference or training.

This article also surveys a number of avenues that prior work have taken to optimize DNN processing. With respect to energy, since data movement dominates energy consumption, a primary focus of some recent research has been to reduce the data movement while maintaining performance accuracy, throughput and cost. This means selecting architectures with favorable memory hierarchies like a spatial array, and developing dataflows that increases data reuse at the low-cost levels of the memory hierarchy. We have included a taxonomy of dataflows and an analysis of their characteristics. Other work is presented that aims to save space and energy by changing the representation of data values in the DNN. Still other work saves energy and sometimes time by exploiting the sparsity of weights and/or activations.

The DNN domain also affords an excellent opportunity for joint hardware/software co-design. Thus, increasing sparsity (increasing the number of zero values) or changing attributes like data representation by reducing the precision of values or using more complex mapping of the stored value to the actual value for computation, can improve efficiency. However, to avoid losing accuracy it is often useful to modify or fine-tune the weights of the network to accommodate these changes. Thus, this article both reviews a variety of these techniques and discusses the frameworks that are available for describing, running and training networks.

Finally, DNNs afford the opportunity to use mixed-signal circuit design and advanced technologies to improve efficiency. These include using memristors for analog computation and 3-D stacked memory. Advanced technologies can also can facilitate moving computation closer to the source by embedding computation near or within the sensor and the memories. Of course, all of these techniques should also be considered in combination, while being careful to understand their interactions and looking for opportunities for joint hardware/software co-optimization.

In conclusion, although much work has been done, deep neural networks are an important area of research with many promising applications and opportunities for innovation at various levels of hardware design.

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