A Mutual Information Accelerator for Autonomous Robot Exploration
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1. Introduction & Summary of Contribution

Robotic Exploration
Where should the robot move next to learn the most about its environment?

Challenge
Computing the mutual information I(M,Z) is slow (high time complexity) and thus becomes the bottleneck of autonomous exploration system.

Our Contribution
Proposed Multicores MI Accelerator
✓ High-throughput: Computes the MI for the entire map of size 10.05m x 10.05m with 0.05m resolution for the first time at 11 Hz on an ASIC (88x faster than a typical ARM CPU used on robotic racecar) while consuming only 164 mW.

Theoretically Proven Approach
Move to the location that maximizes the mutual information between prospective scan location and sensor angle dependent.

Benefits for Autonomous Exploration
✓ Enables more optimal selection of the next scan location for exploration.

2. Autonomous Exploration Pipeline & MI Formulation

Typical Autonomous Exploration Pipeline

Occupancy Map
Mutual Information

Theoretically Proven Approach
Move to the location that maximizes the mutual information between prospective scan location and sensor angle dependent.

Mutual Information (MI)

I(M,Z) = I(M) – I(M,Z)

Computing the mutual information I(M,Z) is slow (high time complexity) and thus becomes the bottleneck of autonomous exploration system.

3. Hardware Design Challenges

Challenges: Memory Bandwidth (Not Compute) Limits Performance

Each core performs independent read from the map stored in SRAM every cycle to remain active. However, their compute is limited by the memory bandwidth of dual-port SRAMs.

4. Proposed Architecture & Detailed Implementation

4A. Memory Banking Architecture

Memory Access Pattern
Naïve Implementation
Proposed Implementation

4B. Priority Arbiter Architecture

Arbiter Operation
Arbiter Architecture

Each round of arbitration completes in one cycle due to a low critical path of O(log(C)), which is less than O(log(C)+O(log(B))) from round-robin arbiter presented in RSS 2019. Note: C = # of cores, B = # of banks.

5. Results & Real-world Experiments

ASIC Layout using TSMC 65nm LP
Chip size: 2550um x 2550um, Gates: 2,981,291
Clock Core: 116.5MHz, Power: 164mW

System Performance
System throughput (purple) at 91% of theoretical limit (dotted black line)

Real-world Autonomous Exploration Experiment using Xilinx XC7Z045 FPGA