A 24Gb/s Software Programmable Multi-Channel Transmitter

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24Gb/s Transmitter

- A test instrument for verifying different transmission algorithms
- Multiple operation modes
  - 2-channel or 4-channel Analog Multi-Tone (AMT)
  - 2PAM, 4PAM, 8PAM, … baseband
  - Software programmable
High-Speed Electrical Links

Network Routers

CPU/Controller to DRAM

CPU to GPU
State of the Art Links

- Baseband 2PAM or 4PAM
- 4-5 tap discrete linear transmit equalizer
- 5-20 tap decision feedback equalizer (DFE)
Channel Characteristics in Links

- Notches caused by reflections
  - From impedance discontinuities
  - E.g. vias, stubs, package, parasitic capacitance, etc
- Multi-Tone signaling can improve performance
A Practical AMT Architecture

- Small number of sub-channels (N)
  - 2, 3, or 4 in most cases
- N-times over-sampled equalizer per sub-channel at the transmitter
- Multi-Input Multi-Output (MIMO) DFE at the receiver
- AMT is a generalization of a baseband system
Two-Channel Example

Interference zero at the sampling points
Called a Trans-multiplexer
Evolution of a Baseband Tx Equalizer

4-tap BB transmitter

2-way parallelize

Shift “x” to the left
Shift “W” to the right

Represent as over-sampled equalizer
AMT is a Generalization of Baseband

- AMT has more degrees of freedom
  - Better capable of shaping the transmit spectrum
- MIMO DFE is also a generalization of a BB DFE

4-tap Baseband
(2-way parallelized)

2-Channel AMT
4 taps per channel
Software Programmable Transmitter

- Equivalent functionality
  - 16-tap FIR filter at 12GHz
  - 2-bit inputs (4PAM) and 10-bit taps
Measured Eye Diagrams

Baseband Mode

- 2PAM
  - Un-Equalized
  - 12Gb/s

- 2PAM
  - Equalized
  - 12Gb/s

- 4PAM
  - Equalized
  - 24Gb/s

AMT Mode

- Ch1
  - 4-channel AMT (Equalized – Post Processed)
  - 18Gb/s

- Ch2
  - Equalized

- Ch3
  - Equalized

- Ch4
  - Equalized

On an oscilloscope

Rx implemented in Matlab
12GS/s Digital to Analog Converter

- 2-way output multiplexed current-mode DAC
- Termination supply 1.8V
  - Unused current dumped to 1.0V to save power
- 1.8V_{pp} output swing

Digital Equalizer Datapath (One Phase)

- Multiply 16 2-bit numbers by 16 10-bit numbers
  - Multiplication using 4:1 multiplexers
  - W and 3W stored in flops
- Add results using 4:2 compressor units
- 2-way parallelized to operate with a 1.5GHz clock
Equalizer Floorplan

- Phase 1
- Phase 2
- Phase 3
- Phase 4

Input pins to output pins

μm
Complete Equalizer with Routing

Post Route layout in SOC Encounter
Transmitter Clocking

- Phase interpolator (PI) between DAC and equalizer
  - Programmed offline
- Mesh 1.5GHz clock distribution in the equalizer
- Pattern generator clock branches off from equalizer grid
  - Part of the clock distribution latency in the critical path
Performance Summary

Measured Transmitter Performance

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Process</strong></td>
<td>90nm CMOS</td>
</tr>
<tr>
<td><strong>Maximum Rate</strong></td>
<td>29Gb/s</td>
</tr>
<tr>
<td><strong>Digital Power</strong></td>
<td>350mW</td>
</tr>
<tr>
<td><strong>Analog Power</strong></td>
<td>160mW</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>0.8mm²</td>
</tr>
<tr>
<td><strong>Output Swing</strong></td>
<td>1.6V&lt;sub&gt;pp&lt;/sub&gt;</td>
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21mW/Gbps

Chip Micrograph
Multi-Tone Operation

Multi-Drop Configuration

\[ C_i = 1\text{pF} \]

Frequency Response

Measured
3-Channel AMT, 9Gb/s
Multi-PAM Operation

\[
Y_{(4\text{PAM})} = X_1_{(2\text{PAM})} + 2X_2_{(2\text{PAM})}
\]

2PAM/4PAM symbols

Tx configuration in 8PAM/16PAM mode
Fractional Equalization

Measured 8PAM Baseband, 18Gb/s
Cyclically Time-Variant Equalization

4 different paths to output → 4 different responses

Time-Invariant Equalization
SIDR = 26dB
28Gb/s

Time-Variant Equalization
SIDR = 31dB
28Gb/s

Conclusions

• A 4-way parallelized equalizer with each parallel branch programmed independently supports
  • Analog Multi-Tone
  • Multi-level baseband
  • Fractional (over-sampled equalization)
  • Cyclically time-variant equalization
• Power overhead due to digital implementation
  • Instead of pseudo-DAC
• Area overhead for storing more tap coefficients
Digital Implementation Overhead

A 4-tap 2PAM 6Gbps Tx

8-bit 2:1 MUX
+ w
- w
x
4

Add four 8-bit numbers

Compressor

4x8

8-bit Adder

To 7-bit DAC

<table>
<thead>
<tr>
<th>Power</th>
<th>0.5mW</th>
<th>10.3 mW</th>
<th>5.0 mW</th>
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<td></td>
<td>Includes clock power inside flops</td>
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| Area        | 960 um²     | 16,000 um²  | 8,000 um²  |

Total Power Overhead = 16.0 mW (2.6mW/Gbps)
Total Area Overhead = 25,000um²

Compared to a Pseudo-DAC implementation