A Serial Link Transceiver Based on 8 GSa/s A/D and D/A Converters in 0.25μm CMOS

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Goal: More Bits on Long Links

- Wires expensive: use fewer, more complex links
- Links between boards and systems
  - Communications or computing: tens of Gbit/sec
  - Up to 10m cables or 1m backplane traces
- CMOS technology for systems-on-a-chip
  - Smaller, cheaper, cooler products
- More bits/symbol or faster symbol rate
  - Improve and equalize parasitic filters
  - Reduce other interference source
Equalization of Parasitic Filters

Transmit Signal $\rightarrow$ Receive Signal

- Use high bandwidth circuits and RF techniques
  - Linear equalizer using DAC in transmitter
    - Wire and circuit losses are linear, time invariant
    - Attenuates low frequencies to match cable loss
    - Signal amplitudes decrease with frequency
- ADC in receiver for higher performance
  - More bits/symbol: multi-level modulation
  - Decision Feedback Equalization (DFE)
Other Interference Reduction

- Correct linear interference with DAC
  - Reflections from connectors and packaging
  - Signal and clock coupling
  - Correlated supply bounce

- Cancel static errors from mismatches
  - Timing errors
  - DAC nonlinearity
  - ADC offset voltage errors

- Random time-varying noise
  - Thermal noise
  - Random phase noise (high bandwidth timing recovery)
Calibrated Link Based on DAC, ADC

- 2 bits for 4-level signaling
- 4 extra bits for equalization, interference correction
- 2 more bits to explore limits

8 GSample/sec: 1 FO4 gate delay in 0.25μm CMOS
4 GHz Bandwidth

- 2 bits for 4-level signaling
- 2 extra bits for DFE
Organization

- Introduction
  - Transceiver design
    - DAC circuits
    - ADC enhancements
    - Inductors to distribute parasitic capacitances
    - Clock generation
- Experimental results
- Conclusions
Time-Interleaved DACs

- DACs enabled by overlap of two 1 GHz clocks
  - Need precise clocks: $3\%_{pp}$ phase noise $\Rightarrow 24\%_{pp}$ symbol
  - Fast clocks (period of 8 gate delays) limit interleaving
  - Capacitance of all 8 DACs loads output
- Predriver $V_{ddReg}$ controls output current
- Total $RC_{out} = 25\Omega \times 4.3\text{pF} \rightarrow 1.5\text{ GHz bandwidth}$
  - 2.8pF wire cap, 0.6pF pad cap, 0.9pF NMOS drain cap
Interleaved Flash ADC Comparator

- Offsets corrected with DAC in 2nd stage latch
  - Simple, high bandwidth sample/hold amplifier
  - No switches or capacitors: breaks bandwidth vs. offset tradeoff

- Enhancements over GAD chip (VLSI-99)
  - Improved DAC linearity through better matching of clock coupling
  - Clocking error corrected
  - S/H gain reduced 30% to 1.3: 7 GHz bandwidth (0.4 LSB pp noise)

- Total $RC_{in} = 25 \Omega \times 1.9 \text{pF} \rightarrow 3.3$ GHz bandwidth
  - 0.6pF wire cap, 0.6pF pad cap, 0.7pF NMOS gate cap
Goal: reduce effect of large parasitic capacitance
- Old good idea: distributed amplifiers in oscilloscopes

If $\sqrt{L/C}=50\Omega$: lumped transmission line
- Each ADC sees $50\Omega$ to the right, $50\Omega$ to the left

Inputs of pairs of ADCs to separate pads
- Bond wire inductors can optionally be inserted

Bandwidth traded for delay (100ps total on line)
Phase adjusters correct LC delay, static errors

- Adjuster: clock mux, 1/16th-symbol clock interpolator
- 8 ADC phase adjusters + 1 for timing recovery
- 16 DAC phase adjusters (2 clocks for each DAC)
Transceiver Die Photo (3.5x3.5 mm)

- DAC Output
- DAC PLL
- Retime Decode
- ADC PLL
- ADC Retime
- Transmit Logic
- Receive Logic
- Memory
- 1024 x 8 bit DAC Memory
- 1024 x 4 bit ADC Memory
ADC Bond Wire Inductor Photo

- 2-turn inductors ~1.1 nH
  - Not onchip inductors: large R
- Goal: inductors in flip-chips
- HSPICE: +/-30% variation doesn’t affect results
  - nH/mm depends on log(D)
  - 30 gauge wire form: 200 μm
- Verify LC match with TDR
- Inductors increase bandwidth to more than 6 GHz
- Measured TDR matches simulated TDR with $L=1.1\text{nH}$
- Bumps are due to connector and package reflections
ADC Performance

- **SNDR limited by phase noise**
  - Not improved by inductors: distortion proportional to signal
  - Technology file error reduced filter cap: underdamped PLL
  - Input couples into PLL, is downsampled: excites noise peaks

<table>
<thead>
<tr>
<th>Power</th>
<th>1.1 Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Error (INL)</td>
<td>0.6 LSB_{pp} (3 raw)</td>
</tr>
<tr>
<td>Static Phase Error</td>
<td>10 ps_{pp} (47 raw)</td>
</tr>
<tr>
<td>Random Noise</td>
<td>0.5 LSB_{pp}</td>
</tr>
<tr>
<td>Timing Variation</td>
<td>15 ps/V</td>
</tr>
</tbody>
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**SNDR, dB**

- **ENOB**

- **Phase noise peaks**

- **Frequency, MHz**

- **Phase Noise**

- **Power**

- **Static Error (INL)**

- **Static Phase Error**

- **Random Noise**

- **Timing Variation**
### DAC Performance

**Measurements**

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<table>
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<tbody>
<tr>
<td>LSB: 3mV</td>
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<tr>
<td>Power</td>
<td>1.9 Watts</td>
</tr>
<tr>
<td>Static Phase Err.</td>
<td>10 ps&lt;sub&gt;pp&lt;/sub&gt;(47 raw)</td>
</tr>
<tr>
<td>Clock Coupling</td>
<td>6LSB&lt;sub&gt;pp&lt;/sub&gt;(63 raw)</td>
</tr>
<tr>
<td>Voltage Error</td>
<td>1LSB&lt;sub&gt;pp&lt;/sub&gt;(3.7raw)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>3 GHz(1.5 L=0)</td>
</tr>
<tr>
<td>Phase noise</td>
<td>45 ps&lt;sub&gt;pp&lt;/sub&gt;</td>
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- **Wrong inductors bonded, half ideal value: low BW**
- **Phase noise affects asynchronous SNDR**
  - Less effect on synchronous transceiver
Transceiver Equalization, DAC to ADC

- 8 unique pulse responses: need 8 lookup tables
- Short cable used: 2 GHz transceiver bandwidth
- Measured with MSB comparators by adding DC
8 GSymbol/s Transceiver Eyes

- Eye openings less than 750 mV swing by 125 ps
  - Binary: 300 mV_{pp}, 4-level 100 mV_{pp}; 45 ps_{pp} width
  - Random transceiver phase noise: 57 ps_{pp}
  - 2 GHz bandwidth, large voltage errors corrected

- Binary operation also verified at 10^{-10} BER
Conclusion

- High speed CMOS circuit techniques
  - Time-interleave DACs and ADCs for high sample rate
  - Inductors to trade bandwidth for delay
  - Small transistors for high bandwidth, low power

- Calibration to improve accuracy, maintain speed
  - Extra DAC bits to correct interference, nonlinearity
  - ADC offset cancellation with DAC inside comparator
  - Clock interpolators to correct static phase errors
  - Correct layout, circuit asymmetries to lower design risk

- Data converters at binary transceiver speeds
  - Accurate timing is crucial
  - Long links: 4-level signaling, DFE