Silicon-Photonic Clos Networks for Global On-Chip Communication

Ajay Joshi†, Christopher Batten†, Yong-Jin Kwon‡, Scott Beamer‡, Imran Shamim†, Krste Asanović‡, Vladimir Stojanović†

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†Massachusetts Institute of Technology  ‡University of California, Berkeley
Our target manycore system

- 64-tile system
- 1 or more cores per tile
- 5 GHz clock
- ~20 W power budget for network
On-chip network topology spectrum

- Mesh
- CMesh
- Clos
- Crossbar

Increasing diameter

Increasing radix
Landscape of on-chip photonic networks

Mesh
CMesh
Clos
Crossbar

[Shacham’07]
[Petracca’08]

[This work]
[Pan’09]

[Vantrease’08]
[Psota’07]
[Kirman’06]
Outline

- Photonic interconnect technology
- Photonic networks
- Electrical vs Photonic networks
Photonic technology – Silicon photonic link

External Laser Source

Coupler and Taper

Ring Modulator Driver

Photodetector

Receiver

Ring Modulator with $\lambda_1$ Resonance

Waveguide

Ring Filter with $\lambda_1$ Resonance
Silicon photonic link – Coupler

Coupler loss = 1 dB
Silicon photonic link – Ring modulator

Energy spent in E-O conversion = 25 – 90 fJ/bt (independent of link length)

Modulator insertion loss = 0 – 1 dB
Silicon photonic link – Waveguide

Waveguide loss
= 0 – 5 dB/cm
Silicon photonic link – Ring filter, photodetector

Energy spent in O-E conversion = 25 - 60 fJ/bt (independent of link length)

Filter drop loss = 1.5 dB

Photodetector loss = 0.1 dB

Receiver sensitivity = -20 dBm

External Laser Source

Ring Modulator Driver

Waveguide

Photodetector

Filter with \( \lambda_1 \) Resonance

Coupler and Taper

Ring Modulator with \( \lambda_1 \) Resonance

Receiver

Filter with \( \lambda_1 \) Resonance
Silicon photonic link – WDM

Through ring loss = 1e-4 – 1e-2 dB/ring

- Dense WDM (128 λ/wg, 10 Gbps/λ) improves bandwidth density
Silicon photonic link – Energy cost

- E-O-E conversion cost – 50-150 fJ/bt (independent of length)
- Thermal tuning energy (increases with ring count)
- External laser power (dependent on losses in photonic devices)
Design constraints
- 22 nm technology
- 500 nm pitch
- 5 GHz clock

Design parameters
- Wire width
- Repeater size
- Repeater spacing

Repeater inserted pipelined wires

Energy (fJ/bit) vs. Number of pipeline segments

- 1.0 mm
- 2.5 mm
- 5.0 mm
- 7.5 mm
- 10.0 mm
Electrical technology

- **Design constraints**
  - 22 nm technology
  - 500 nm pitch
  - 5 GHz clock

- **Design parameters**
  - Wire width
  - Repeater size
  - Repeater spacing

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` FF | Repeater inserted pipelined wires | FF `

- Repeater inserted pipelined wires

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![Graph showing energy consumption vs. number of pipeline segments with different repeater spacings.](image)
Electrical vs Optical links – Energy cost

- Elec: Electrical
- Opt-A: Optical-Aggressive
- Opt-C: Optical-Conservative

Optical laser power not shown (dependent on the physical layout)

- Thermal tuning energy
- Transmitter-Receiver energy

Energy (fJ/bit)

<table>
<thead>
<tr>
<th></th>
<th>Elec 2.5 mm</th>
<th>Elec 10 mm</th>
<th>Opt-A 2.5/10 mm</th>
<th>Opt-C 2.5/10 mm</th>
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<td>Length (mm)</td>
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<td></td>
<td>2.5</td>
<td>10</td>
<td>2.5/10</td>
<td>2.5/10</td>
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Electrical vs Optical links – Energy cost

- **Electrical**
  - Energy cost: Approx. 6x
  - Thermal tuning energy: Approx. 6x

- **Optical**
  - Energy cost: Approx. 2x
  - Optical laser power (not shown)
  - Transmitter-Receiver energy

Physical layout dependence:
- Energy cost is dependent on the physical layout.
Electrical vs Optical links – Bandwidth density

Repeater inserted pipelined wires – 10 Gbps/μ

Wavelength-division multiplexed photonic link – 320 Gbps/μ

30x bandwidth density advantage using optical links
Outline

- Photonic interconnect technology
- Photonic networks
- Electrical vs Photonic networks
Outline

- Photonic Interconnect technology
- Photonic networks
- Electrical vs Photonic networks
Distributed Multiplexer Crossbar

Electrical design

Photonic design

Waveguide

Ring filter
Distributed Multiplexer Crossbar

Electrical design

Photonic design

Waveguide

I₀  →  O₀

I₁  →  O₁

I₂  →  O₂

I₃  →  O₃

Modulator

Ring filter

I₀

I₁

I₂

I₃
Centralized Multiplexer Crossbar

Electrical design

Photonic design

Modulator

Ring filter
Centralized Multiplexer Crossbar

Electrical design

Photonic design

Modulator

Waveguide

Ring filter
Photonic crossbar for a 64-tile system
Photonic crossbar for a 64-tile system
Photonic crossbar for a 64-tile system

Photonic Receiver Block
Photonic crossbar for a 64-tile system
Photonic crossbar for a 64-tile system

- 64 tiles
- 64 waveguides (for tile throughput = 128 b/cyc)
- 128 modulators per tile
- 63 x 64 = 4032 ring filters per tile
- Total rings > 500K → 10W (thermal tuning)
Photonic device requirements in a crossbar

Optical laser power (W) contour

Percent area of photonic devices contour
Optical laser power (W) contour

Percent area of photonic devices contour

Waveguide loss and Through loss limits for 2 W optical laser power (30% laser efficiency) constraint
Outline

- Interconnect technologies
- Photonic networks
- Electrical vs Photonic networks
Clos network using point-to-point channels

Electrical design

Photonic design
Clos network using point-to-point channels

Electrical design

Photonic design
Photonic Clos for a 64-tile system

Tile

8 tiles per cluster

56 Waveguides (64λ/direction)
Photonic Clos for a 64-tile system
Photonic Clos for a 64-tile system
Photonic Clos for a 64-tile system
Photonic Clos for a 64-tile system

- 64 tiles
- 56 waveguides (for tile throughput = 128 b/cyc)
- 128 modulators per cluster
- 128 ring filters per cluster
- Total rings ≈ 28K → 0.56W (Thermal tuning)
Photonic device requirements in a Clos

Optical laser power (W) contour

Percent area of photonic devices contour

Waveguide loss and Through loss limits for 2 W optical laser power (30% laser efficiency) constraint
Photonic device requirements in a Clos

- Optical laser power (W) contour
- Percent area of photonic devices contour

- Optical loss tolerance for Crossbar
- Optical loss tolerance for Clos
Photonic Crossbar vs Photonic Clos

- 10 W power for thermal tuning circuits (1 μW/ring/K)
- For 2 W optical laser power
  - Waveguide loss < 1 dB/cm
  - Through loss < 0.002 dB/ring

- 0.56 W power for thermal tuning circuits (1 μW/ring/K)
- For 2 W optical laser power
  - Waveguide loss < 2 dB/cm
  - Through loss < 0.05 dB/ring
Outline

- Photonic interconnect technology
- Photonic networks
- Electrical vs Photonic networks
Simulation setup

- Cycle-accurate microarchitectural simulator
- Traffic patterns based on partition application model
  - Global traffic – UR, P2D, P8D
  - Local traffic – P8C
- 64-tile system, 512-bit messages
- Events captured during simulations to calculate power

**CMesh**

**Clos**
Power-Bandwidth tradeoff

CMeshX2
Channel width = 128b

Clos
Channel width = 64b
Power-Bandwidth tradeoff

CMeshX2
Channel width = 128b

Clos
Channel width = 64b

2-3x on-chip power savings for global traffic (off-chip laser)
Power-Bandwidth tradeoff

CMeshX2
Channel width = 128b

Clos
Channel width = 64b

Clos
Channel width = 128b

Comparable on-chip power for local traffic (off-chip laser)
Conclusion

- Accurate baseline electrical design required
- Need to carefully account for the energy components in optical interconnects
  - E-O-E conversion, Thermal tuning power, Optical laser power
- Clos network provides comparable throughput at lower energy for global traffic patterns
- More work required on the photonic device design
Acknowledgement

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  - Intel Corp.
Backup
Clos network using intermediate crossbar crossbar

Electrical design

Photonic design
Clos network using intermediate crossbar crossbar

Electrical design

Photonic design
Clos network using intermediate crossbar

Electrical design

Photonic design