A 9GHz Injection Locked Loop Optical Clock Receiver in 32-nm CMOS

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

The bottleneck of multi-core processors performance will be the I/O, for both on-chip core-to-core I/O, and off-chip core-to-memory. Integrated silicon photonics can potentially provide high-bandwidth low-power signal and clock distribution for multi-core processors, by exploiting wavelength-division multiplexing. This thesis presents the technology environment of the monolithic optical/electrical chip, and then focuses on how an optical method would look like for both source-synchronous link and for on-chip global clock distribution. The injection-locked loop clock receiver that suits this architecture breaks the bandwidth/sensitivity tradeoff, and a self-adjusting mechanism is added to increase robustness. The simulated receiver sensitivity is -14dBm at 9GHz, consuming 77.14µW and generating jitter within 0.15ps when locked onto a mode-locked laser clock source. The chip infrastructure and testing procedures are then presented, and lastly a truly integrated optical-electrical design flow is shown as well.

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Chapter 1

Introduction

The emergence of multi-core processors [29] [30] [31] [32] creates an increasingly complex routing environment for long interconnects. With traditional copper interconnects, area is expensive, as each wire is only able to carry one data signal at maximum bandwidth. Although the I/O circuits are improving in bandwidth as technology scales, the channels are not. Since each core must be able to communicate with a set of other cores and off-chip memory, the total bandwidth required is harder to reach under the overall die power constraint, set by power delivery and cooling requirements. If copper wires are not replaced, we will quickly reach a point where it is simply infeasible to add more cores.

To address this problem, this work investigates the shift to an optical paradigm, where by exploiting wavelength-division multiplexing (WDM), multiple channels of data can be transmitted along a single optical waveguide without interference. This allows a much greater bandwidth density for both on-chip and off-chip channels. Also, with low loss waveguides which are theoretically possible, the total power consumption for interconnects can be greatly reduced. With WDM, we can use architectures that have fewer routers, hence lower latency.

A cartoon of an integrated photonic intra-chip WDM link is shown in Figure 1-1 [1]. The laser light from an external laser source is coupled into chip A, each channel is modulated separately, and then sent to another chip to receive the data. Besides data transmission, it is possible to have an energy efficient and small area clock receiver
with a single wavelength modulated clock signal, or a low power, low skew/jitter clock distribution network by using a mode-locked laser or self-pulsed laser to send short optical pulses into an optical clock distribution network. This alleviates the need for PLLs or DLLs, saving area and power. The focus of this thesis will be on optical clocking, and comparing it to a traditional clocking scheme.

An important feature of this project is that all our photonic structures will be made using standard CMOS processes. Since the photonic devices and their control circuits are only tens of microns apart, this monolithic integration reduces the area and energy costs of interfacing electrical and optical components. Also, monolithic integration is practical in the sense of cost and manufacturability for processor and memory manufactures, but at the same time constrains the materials and dimensions that we are able to use. We believe that this is a tradeoff that must be made for silicon photonics to be implemented in mainstream processor design. A first integrated photonics chip was designed and manufactured in Texas Instrument’s 65nm bulk CMOS [1], and the designs in this thesis were made in a 32nm bulk CMOS process.

In the following sections, we will go over the key points of our photonic technology and describe the characteristics of the photonic devices used in this project. Next we will look at how clocking is done traditionally, then point out the reasons why optical clocking makes sense. The optical clock receiver circuit will be explained in detail, which is the main focus of this thesis. Finally, a quick summary of the infrastructure for on chip testing and automatic layout will be given.
Chapter 2

Photonic Technology

For simplicity of integration, and to be compatible with the majority of CMOS processes, we chose to design our chip with a monolithic CMOS process, without flip-chip bonding a III-V wafer or adding additional layers [1]. Having this constraint narrows the design space, but as mentioned in the introduction, this allows the photonics to be imported into a microprocessor design flow without an overhaul of the existing technology.

2.1 Laser Source, Vertical Couplers and Optical Waveguides

Due to the indirect bandgap of silicon, there are no known high-efficiency lasers in silicon, so all the silicon-photonic technologies proposed here use off-chip laser sources. To couple the light into the waveguides from an optical fiber, we use vertical couplers, which are more feasible from a packaging stand point compared to edge coupling. Vertical couplers have a bragg-grating like structure in a roughly 10µm by 10µm area, which then tapers into a single-mode waveguide with a width of approximately have a micron.

Previously, on-chip photonic waveguides have been made using the silicon body as a core with custom thick buried oxide (BOX) as cladding in a silicon-on-insulator
(SOI) process [6], or by depositing silicon-nitride [7] on top of the interconnect stack. These methods either need significant process changes to a standard CMOS flow, or have poor heat dissipation properties, which may cause problems as high-power density is common in manycore computation. Given that compatibility to mainstream processes is a priority, we have chosen to use bulk CMOS, and the polysilicon layer for the waveguide. Since the shallow-trench oxide beneath the polysilicon is too thin to form an effective cladding and shield the core from optical mode leakage losses into the silicon substrate, we have developed a novel self-aligned post-processing procedure, as shown in Figure 2-1, to etch away the silicon substrate underneath the waveguide forming an air gap [2]. With adequate layout spacing and measured etching, this post-processing should not affect the transistors.

Figure 2-1: Cross-section and SEM image of the waveguides and air gap. Note that the air gap does not reach the transistors. [1, 2]

### 2.2 Optical Modulators

Data is transmitted by modulating the continuous wave laser light, and this is done by changing the resonance frequency of a ring modulator that is near the waveguide. Due to their smaller size, ring modulators have a smaller capacitance, which results in less power consumption compared to Mach-Zehnder modulators. As shown in Figure 2-2, the intrinsic poly-silicon ring is sandwiched by N-type and P-type poly-silicon at each straight section, forming lateral PIN diodes, so we can inject free carriers into the ring. A scanning electron microscope (SEM) photo of the ring modulator is shown in Figure 2-3. By changing the amount of free carriers in the ring, we can change
its effective index of refraction, which in turn change the resonance frequency. The continuous wave laser light that passes by on a waveguide will get coupled into the ring and absorbed if the resonance frequency matches the frequency of the light. Multiple transmitters can modulate light at different frequencies, so we can transmit multiple channels of data simultaneously on the same waveguide. The temperature of the ring also affects the index of refraction, so in-plane polysilicon heaters are placed to control the temperature. Due to the large current range to guarantee wavelength isolation, the heaters are directly connected to pads, and driven by current DACs on the test board. In order to control the temperature, the resistance of the heater is monitored by measuring the voltage drop across it with an off-chip ADC, and in conjunction with the temperature coefficient of polysilicon, we can derive the temperature of the heater.

![Illustration of ring modulator](image)

Figure 2-2: Illustration of ring modulator. Note that diodes were only implemented on the straight sections of the ring due to fabrication constraints. [3]

### 2.3 Photodiodes

At the receiving end, a ring is tuned to the channel it wants to receive, and the light at that frequency is coupled into the photodiode of the receiver. Photodiodes for the receivers are made with SiGe, which are used in modern CMOS processes
to increase mobility in PMOS transistors by introducing strain. The percentage of Ge determines the bandgap of the material, so with more Ge the photodiode will be able to absorb longer wavelengths. In this process we are assuming the mole-fraction of Ge in the SiGe alloy is approximately 30%, which corresponds to a wavelength of about 1200nm. When the light is absorbed, an electron-hole pair are created, which are swept out due to the electric field from the P-N junction, and picked up by receiver circuits. Since these small photodiodes are integrated on chip, the wires in between the diodes and the receiver circuits can be very short, on the order of tens of micrometers. Compared to connecting to a photodiode off chip through a bond pad, this reduces the parasitic capacitance of the connection by two orders of magnitude. Another benefit of integrated photonics is that we are able to have the photodiode itself be a ring resonator coupled to the waveguide, so theoretically we can achieve a reasonable responsivity with a relatively small photodiode, which corresponds to a smaller parasitic capacitance for the diode itself.

2.4 Optical Pulse Source

So far clock transmission or clock recovery has been achieved by several methods based on self-pulsating lasers [17] [18] [19] [25], mode-locked lasers [21] [22], or optoelectronic phase-lock loop (PLL) technologies [23] [24]. The complexity and area overhead of having all-optical phase comparators on a multicore processor is too great, so optoelectronic PLLs are better suited for intra-system links of data rates of 100Gb/s.
This is also the case with using self-pulsating lasers to recover the clock from a data stream. We wish to leave all the complexity at the laser source, and have the photonics on chip be as small as possible. A mode locked laser produces a train of short pulses of light by inducing a fixed phase relationship between the modes of the laser’s resonant cavity. A laser may have a number of modes of equal frequency separation, depending on the gain medium bandwidth, and the cavity length. By fixing the relative phase between each mode, the output amplitudes will periodically all constructively interfere with one another, producing a pulse of light with high intensity. These pulses will be separated in time by the round trip time \( T = 2L/c \), where \( L \) is the length of the laser cavity. Semiconductor mode-locked lasers are attractive candidates for generating picosecond pulses at high repetition rates (10GHz) due to their small size, inherent robustness and possibility of integration with other semiconductor elements [21]. It has been shown that a monolithic semiconductor laser can achieve a 10GHz repetition rate with a 6.6 picosecond pulse width and 50 to 570 femtosecond jitter, depending on the existence of an RF electrical reference. Although many of the lasers discussed are in the 1550nm wavelength range, which is unsuitable for our purposes, there have been more recent efforts toward making high repetition mode-locked lasers with vertical cavity surface emitting lasers (VCSELs) [26], or quantum-dot GaAs/InAs lasers [27] that are more suitable for our wavelength ranges.

### 2.5 Summary

In this chapter, we cover the photonics components needed to make a WDM link, and the benefits or difficulties of designing each component in a monolithic CMOS process. Different devices are suitable for different architectures, so we try to explore all the trade off relations between design parameters for each device. Lastly a few candidates for the optical pulse source are presented and discussed.
Chapter 3

Clocking

All synchronous electrical systems require a clock signal, whether it is for synchronizing communication channels in high speed links or for synchronizing functional blocks in a microprocessor. The important merits of a clock distribution scheme are skew, jitter, rise/fall time, and power consumption. Skew is when the same clock signal arrives at different nodes at different times, although they were designed to arrive simultaneously. Jitter is the random fluctuation of the clock edge. These both limit the maximum operation frequency the chip. We will discuss how clocking is done electrically in both links and synchronous logic, and how using optics will be beneficial.

3.1 Electrical Clocking for Links

High speed links usually transmit a high speed clock synchronously with a parallel data bus, as shown in 3-1. The clock receiver uses a phase locked loop (PLL) or delay locked loop (DLL) to capture the edge information, and generate a sampling clock edge aligned with the eye opening of the input data stream. Having the data receivers sample at the phase where the eye opening is widest provides the largest signal to noise ratio (SNR), resulting in the lowest bit error rate (BER). In the case of using a PLL, a lower frequency clock signal can be used, saving the dynamic power consumed on that wire.
To see how skew and jitter affects this link, a simple example is shown in Figure 3-2. Due to interconnect mismatches and possibly circuit mismatches, the timing for each channel might shift relative to the reference clock, so samples are taken away from widest opening of the eye, lowering the SNR, and resulting in a higher BER. Fortunately, this phase error is static, so there are circuit techniques to compensate for it. One way is to have an adjustable delay chain between the clock receiver output and the clock input of the data receiver, and compensating for the skew after a start-up calibration sequence. The adjustable delay chain may be realized by adjusting the delay for each stage, activating a different number of stages [33] [34], or by using phase interpolation and selecting different combinations of phases [35].

Jitter is a random phase variation in a signal, caused by power supply noise and thermal in the transmitter and receiver, and interference coupled in the channels. This random cycle to cycle variation in clock edges shrinks the eye opening, lowering the SNR, resulting in a higher BER.

The performance of the link depends on the receiver timing recovery, and as mentioned in the introduction, the channels do not improve with technology. Also, the large area and power consumption of low jitter PLLs and DLLs adds to the difficulty
Figure 3-2: Inter-signal skew reduces timing margins at receiver. As inter-signal skew increases, samples are taken farther away from widest opening of eye, lowering the SNR, resulting in a higher BER. [4]

of increasing the number of endpoints in a communication network and hence the number of cores.

### 3.2 Optical Clocking for Links

Figure 3-3: A simple example of a point-to-point optical WDM link. The rings on the transmitter side are modulators driven by the driver circuits, and the rings on the right couple the selected wavelength into photodiodes that are connected to individual receivers.

A simple example of a point-to-point optical WDM source forwarded link is shown in Figure 3-3. The photonic structure is the same as the WDM link shown in Figure 1-1, with driver and receive circuits added. Here we use one of the wavelengths
for clock transmission, and the received clock signal triggers the samplers of the other data receivers. Using optics provides many benefits; Each waveguide can carry multiple wavelengths without crosstalk or power rail injected noise. Secondly, with low loss waveguides, the signals will not require re-buffering, hence reducing the jitter injected. This means that the receiver does not need to have a PLL or DLL to provide a stable clock, greatly reducing the power and area overhead. The design of a simple, low power clock receiver will be the focus of the next chapter.

3.3 Electrical Clocking for Synchronous Logic

![Figure 3-4: Simple example of a synchronous pipeline datapath. [5]](image)

We have already discussed how skew and jitter affect a high speed link, now to see how they affect a synchronous system, a simple example is shown in Figure 3-4. At the initial rising clock edge, the value of Q is copied from D and held at that value after a delay of $t_{C-Q}$ for both data registers. This new value of Q causes the combinational logic to change its output state, and it settles to a final value after a propagation delay of $t_{logic}$. Then after holding the output value of the combinational logic for at least the setup time $t_{setup}$ of data register R2, the value of D will be transferred to Q at the next rising clock edge.

So to ensure that data register R2 stores the result correctly, the duration between the two rising clock edges must be greater than the sum of these three $t$ values, or:

$$\frac{1}{f_{\text{clock}}} = T_{\text{clock}} >= t_{C-Q} + t_{\text{logic}} + t_{\text{setup}}$$

In the case of skew, we see that if the clock edge of R1 arrives earlier than R2, then the logic has more time to settle, so it seems fine. However in general, there are data
paths in both directions between clock grids, so in the other direction the skew eats into the propagation time. Thus the clock frequency must be slowed down enough to accommodate the worst case skew. In the case of jitter, we can see that having a clock edge arriving early immediately after a clock edge arriving late squeezes the propagation time, so the clock frequency must be slowed down enough to accommodate the worst case jitter as well.

Traditionally, electrical clocks are generated by PLLs, synchronized by DLLs, and distributed on the chip with trees and/or grids of metal wires. Skew can be caused by transistor mismatch in the routing, and jitter is mainly caused by power supply noise. A simple illustration is shown in Figure 3-5 The jitter of clock networks in processors has lowered over the years, and in a recent example [8], the 9-sigma jitter is down to 100ps, with a skew of 15ps and 3W power consumption for the entire clock network. Higher speed clocks require more repeaters in order to maintain reasonably sharp rise/fall edges, which cause more skew, jitter and power consumption.

![Diagram of purely electrical clock distribution network.](image-url)
Note that due to the large area and power consumption of the PLLs, they are implemented at a high level. As an example, 8PLLs are used on a 503mm² die in [8].

### 3.4 Optical Clocking for Synchronous Logic

Besides the benefits of optical communication mentioned above, light may also be used for clocking synchronous logic. The idea of optical clocking was first published by J. W. Goodman in 1984 [9], and others [10, 11, 12, 13, 14] demonstrated different optical clock distribution schemes. The most recent of these is receiverless clocking [14], and although the two clock distribution schemes are different, some comparisons are made between them, just to put this work in context.

One main motivation for optical clocking is the mode locked laser, which can have picosecond pulses, 10GHz or higher repetition rates, and sub-picosecond jitter, as demonstrated in [15]. Monolithically integrated mode-locked laser diodes with sub-picosecond jitter have been demonstrated as well, which makes having a computing system with mode locked lasers possible [16].

<table>
<thead>
<tr>
<th>optical receivers</th>
<th>power efficiency</th>
<th>power mismatch</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.00</td>
<td>0%</td>
</tr>
<tr>
<td>2</td>
<td>0.97</td>
<td>±2%</td>
</tr>
<tr>
<td>4</td>
<td>0.94</td>
<td>±4%</td>
</tr>
<tr>
<td>8</td>
<td>0.91</td>
<td>±6%</td>
</tr>
<tr>
<td>16</td>
<td>0.89</td>
<td>±8%</td>
</tr>
<tr>
<td>32</td>
<td>0.86</td>
<td>±10%</td>
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<tr>
<td>64</td>
<td>0.83</td>
<td>±13%</td>
</tr>
<tr>
<td>128</td>
<td>0.81</td>
<td>±15%</td>
</tr>
<tr>
<td>256</td>
<td>0.78</td>
<td>±17%</td>
</tr>
</tbody>
</table>

Table 3.1: Power Efficiency and Mismatch relative to Optical H-Tree Depth

Since the laser source can have a high peak power, on the order of 100mW, we can also easily branch the clock signal. A splitting loss of less than 3% with a ratio of 49:51 has been demonstrated in a process similar to standard CMOS processes [5]. This enables us to have an optical h-tree with a large fanout, and still maintain a good power efficiency and low mismatch at the receiver end. The relationship between
power efficiency and mismatch relative to optical h-tree depth is shown in Table 3.1.

In the case where there is zero area power overhead for clock receivers, since waveguide losses are very small, the optimal condition is to have optical RX at every clock grid, basically directly driving the grid wire cap, and the gate cap of the static and dynamic latches we wish to clock. This configuration is shown in Figure 3-6.

![Diagram of purely optical clock distribution network.](image)

Figure 3-6: Diagram of purely optical clock distribution network.

But of course since there is a finite area and power consumption overhead for the receiver, the optimal point will be somewhere in between, with both optical h-tree and electrical buffering, as shown in Figure 3-7.

With simple receivers that can be small in area and power consumption, we can optically split the clean clock signal further down the distribution tree before we transfer it to an electrical signal. This corresponds to fewer stages of repeaters the clock signal goes through after the receiver, which means less added jitter.

Please note that a clock source using a single modulated wavelength as used in the links may be used for global clock distribution instead of a mode locked laser. This alleviates the need for a separate waveguide, at the cost of more jitter.
3.5 Goals of an Optical Clock Receiver

The simplest possible receiver would be the receiverless clocking scheme [14], in which two photodiodes are connected in series from supply to ground, and by shining light pulses at them alternately, a clock signal can be generated. The only circuitry between the photodiodes and the clocked node are buffers, so a minimal amount of jitter is added. Also, less circuits means less circuit power consumption. Since in our design we use on-chip waveguides, we cannot afford the area to have two waveguides leading into two photodiodes at many places. Lastly, in order to swing the capacitance of two photodiodes rail-to-rail, the quantum efficiency of the photodiode must be sufficiently high or else the optical power required will be large. (Since the average optical power \( P_n = C * V_{DD}/(T_B * R) \), where \( V_{DD} \) is the supply voltage, \( C \) is the node capacitance, \( R \) is detector responsivity and \( T_B \) is the bit period.) For a 5GHz clock and a reasonable photodiode, \( V_{DD} = 1V, C = 20fF, R = 0.5A/W, T_B = 100ps \), then the required average optical power is 0.4mW, or -3.9dBm. Unfortunately, the quantum efficiency of the SiGe photodiodes created in the CMOS flow may not be able to reach 0.5A/W. So the overall power including optical power may not be optimal.
Due to these reasons, a more sensitive but still simple receiver is desired.

3.6 Summary

In this chapter we discuss the methods currently used for clocking in high speed links and microprocessor chips. We discover that optical clocks can have much better skew and jitter performance, due to the superior signal integrity of optics compared to electrical wires. This allows us to use a simpler circuit without PLLs or DLLs, greatly reducing the power and area overhead for a multi-core processor.
Chapter 4

Optical Clock Receiver Circuit Design

Now that the reasons for having a small receiver circuit to amplify the photodiode signal are presented, let us first investigate the commonly used Trans-Impedance Amplifier (TIA). In its simplest form, a single stage TIA can be implemented with two transistors and a resistor, as shown in Figure 4-1.

![Figure 4-1: Schematic of a simple Trans-Impedance Amplifier.](image)

For simpler analysis, let us simplify the circuit further into the one shown in Figure 4-2.
Figure 4-2: Schematic of an amplifier of finite gain $A$ with feedback. $R$ is the feedback resistor, $C$ is the input capacitance, $I$ is the input current.

With an amplifier of finite gain $A$, the output voltage is determined by the differential input. Since the input node is the dominant pole due to the large input capacitance provided by the photodiode, we can determine the sensitivity of the circuit by looking at the slope of the input node voltage $V_{in}$. In this circuit, we can see that initially, when $I_{in} = 0$, then $V_{out} = V_{in} = 0$. If $I_{in}$ is changed to some finite value, all the current goes to charge up the input capacitance $C$, so $V_{in}$ begins to rise with a slope of $I_{in}/C$. Now because of the feedback path, some, and eventually all of the current goes through the resistor, hence the voltage at the input settles at $(R * I_{in})/(1 + A)$, the output settles at $(-R * I_{in} * A)/(1 + A)$, and the voltage across the resistor is $R * I_{in}$ as it should be. This transient voltage plot is shown in Figure 4-3.

In the case where $R = \infty$, it is equivalent to removing the feedback resistor and having an open between input and output, as shown in Figure 4-4? Now all of $I_{in}$ will be directed toward charging up the capacitance, so no current will be "stolen" by the resistor. Since the input current and input capacitance are determined by the photodiode, the maximum slope that can be achieved is $I_{in}/C$.

Now, the reason why the slope is so important is it determines the effect of voltage noise on jitter. Voltage noise shifts the voltage points up and down by a random amount, so the timing when the voltage crosses the switching threshold shifts left
Figure 4-3: Transient plots of input voltage for when R is finite and when R is infinite.

and right in the time domain. With a steep slope, the same amount of voltage noise corresponds to less jitter, as shown on the left of Figure 4-5.

So similar to the circuit in Figure 4-2, in the TIA circuit in Figure 4-1, the gain of a stage is limited by the resistance of the feedback resistor $R$, and that in turn is limited by the bandwidth the TIA is supposed to function at. The dominant pole is the large input capacitance, so a low impedance is required for the receiver to operate at high bandwidth.

### 4.1 Injection Locked Loop

#### 4.1.1 Simple Integrating Receiver

To increase the sensitivity, we could just simply take away the resistor, and let the input current be integrated on the capacitive node, like domino circuits. Since this is a clock receiver, there is no external clock to reset this capacitive node, so there must be some feature that resets the node after a clock edge is detected. As shown in Figure 4-6, we use an NMOS transistor to reset the input node. This essentially breaks the
Figure 4-4: Schematic of an amplifier of finite gain $A$ without feedback. $C$ is the input capacitance, $I$ is the input current.

Figure 4-5: Diagram explaining the effect of voltage noise on jitter. A steep slope has less jitter for the same input noise.

The trade-off between gain and bandwidth for a TIA. By having two states—a high gain state and a reset state—we can achieve high sensitivity when we are expecting edge information, and have a high bandwidth reset state for higher operation frequency.

For simulation, the photodiode is modeled as a current source and a 10fF capacitance in parallel. Although the mode lock laser can provide very short pulses in the sub-picosecond range, there is still a finite transit time of the photodiode itself. In the photodiode design implemented in this chip, we can expect the transit time to be on the order of $W_{\text{intrinsic}}/v_{\text{sat}}$, which is the intrinsic region width divided by the hole saturation velocity, which is about 5ps. For simulations, the current pulse is
modeled as a triangular pulse with a half-max width of 10ps, which is a conservative estimate. The frequency is also slowed down to 5GHz so the waveforms are easily readable. Please note that the same circuit can also be used if the optical input is a single wavelength modulated clock pulse, as we are integrating the input current onto a capacitor. The slope will be worse, so there will be more jitter, but still much better than electrical clock distribution.

The transient operation of the circuit is shown in Figure 4-7. When an optical pulse hits the photodiode, the generated electron hole pairs create a current, charging up node \( i_{\text{in}} \). The voltage change at node \( i_{\text{in}} \) is determined by

\[
\Delta V = \frac{(R \ast \int_{t_{\text{reset}}}^{t_{\text{o}}} P(t)dt)}{C_{\text{in}}}
\]

Where \( R \) is the responsivity of the photodiode (A/W), \( t_{\text{to}} \) to \( t_{\text{reset}} \) is the time period between when the optical pulse arrives to when the reset is triggered. \( P(t) \) is the instantaneous optical power that reaches the photodiode, and \( C_{\text{in}} \) is the total capacitance at node \( i_{\text{in}} \). In this case, we see that \( \Delta V \) is \( V_{DD} \), or 1V, which causes the inverters to change their output voltage. After two inverter delays, the voltage at node \( reset \) goes high, turning on the reset NMOS, pulling node \( i_{\text{in}} \) back down to a low voltage. In this circuit, skew is determined by the process mismatch of the inverter chain, which affects the inverter delays. Jitter is mostly determined by the power supply noise injected through the inverters. So obviously more stages of inverters

Figure 4-6: Schematic of simple clock receiver with reset NMOS.
Figure 4-7: Transient waveforms at node in (top left) and out (top right) with respect to the switching threshold of the first inverter $V_m$ and optical pulses.

correspond to more skew and jitter. Notice that since the pulse width is independent of the pulse frequency, so the duty cycle will have to be controlled by adjusting the length of the inverter chain, or by using a divide by 2 circuit at the output.
4.1.2 Integrating Receiver with Tunable Reset

Since the node \( \text{in} \) from Figure 4-6 swings from 0V to 1V, the power consumption is the same as the receiverless design. To control how far below \( V_m \) node \( \text{in} \) reaches, we stack a DAC of NMOS transistors with the reset NMOS, creating a tunable strength reset NMOS stack, as shown in Figure 4-8.

![Figure 4-8: Schematic of simple clock receiver with a tunable reset NMOS stack.](image)

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![Figure 4-8: Schematic of simple clock receiver with a tunable reset NMOS stack.](image)

Figure 4-9: Transient waveforms at node \( \text{in} \) (top left) and \( \text{out} \) (top right) with respect to the switching threshold of the first inverter \( V_m \) and optical pulses.

The transient operation of the circuit is shown in Figure 4-9. Note that since
we have a smaller voltage swing, the optical pulse power required is greatly reduced. Also note that any voltage noise at node \(in\) will be translated into jitter in time by the slope at which the voltage crosses \(V_m\), which is determined by \(R \cdot P/C_{in}\).

A schematic of the tunable NMOS stack is shown in Figure 4-10. The lower row of NMOS transistors are binary weighted current sources. Due to the small sizes of these transistors, they are vulnerable to mismatch, so the smallest transistor is duplicated to improve the linearity after calibration. Programmable registers control which current sources are connected to the reset NMOS through minimum size transistor switches. During the integration step, the reset NMOS is off, so the input node is isolated from the parasitic capacitance of the current sources. Hence we are able to have a large tuning range without heavily increasing the capacitive load to the input node or the reset node.

Figure 4-10: Schematic of tunable reset NMOS stack.
4.1.3 Integrating Receiver with Precharge – Injection-Locked

To increase the operation frequency, we add a PMOS precharge branch that turns on after the input node discharges past \( V_m \), as shown in Figure 4-11. This allows us to discharge the input node much faster with a stronger NMOS stack, resulting in a net gain of speed, as shown in Figure 4-12.

By looking carefully at the waveform of node \( in \), we see that at the moment before the clock pulse comes in, it is always pre-charged to just below \( V_m \), so the optical charge is always just enough to make node \( in \) go past \( V_m \). The slope at which the voltage at node \( in \) crosses \( V_m \) is now \( (I_{\text{precharge}} + R \cdot P)/C_{in} \). Another way of understanding this circuit is that the first two inverters and the discharge/reset stacks form a three inverter ring oscillator, with a self oscillation frequency set to be slightly lower than the input clock frequency, which is exactly an injection-locked loop. Depending on the settings of the discharge/reset stacks, the ring oscillator will lock onto a certain range of (input current, frequency) values.
Figure 4-11: Schematic of manually tuned clock receiver circuit with PMOS precharge branch.

Figure 4-12: Transient waveforms at node \textit{in} (top left) and \textit{out} (top right) with respect to the switching threshold of the first inverter $V_m$ and optical pulses.
4.2 Auto-locking design

In monte carlo simulations, we are always able to achieve a lock by adjusting the configuration bits. However in an actual chip, it would be much less desirable to calibrate every receiver for every die. Also, the amount of optical power that reaches each receiver may vary after the chip is packaged and optically connected to other chips, so calibration may be required after a system is put together. Finally, and perhaps the biggest issue is that the properties of photodiodes, lasers, modulators and even transistors change with temperature, and the temperature variation on a microprocessor die can be 50 or more degrees [28]. This gives us a motivation to have a circuit that can adapt to a fluctuating environment.

Figure 4-13: Schematic of auto-locking clock receiver circuit. The node 'Vauto' connects the capacitor to the gates of the tuning transistors, adjusting their strength.

The auto-locking version is shown in Figure 4-13. If the NMOS branch is too strong, the receiver takes more time, maybe more than a cycle, to pull the input node back up to Vm, so the duty cycle is less than 50%. Similarly, if the NMOS is too weak, the duty cycle is greater than 50%. Using this relationship, we can integrate this duty cycle difference onto a capacitor, so the strengths of the NMOS and PMOS are gradually tuned until a lock is achieved, as shown in Figure 4-14. When locked, the voltage at Vauto will stay constant if the duty cycles are inversely proportional to the current source current values, so ideally, if the current sources are matched, then
the duty cycle will be 50%. The simulated receiver sensitivity is -14dBm at 9GHz, consuming 77.14μW and generating jitter within 0.15ps. In comparison, to operate at 9GHz, the receiverless design in [14] requires -1.4dBm optical power. A photodiode responsivity of 0.5A/W is assumed in both cases.

![Figure 4-14: Simulated transient waveform of in, output(out4), and Vauto(vm-prime). Before 60ns, the reset NMOS is too weak, so the input node is constantly above Vm, hence out4 is stuck at Vdd. Vauto slowly rises until lock is achieved at around 60ns and stabilizes at about 65 ns.](image)

In the extreme case of process variations and mismatches, the clock receiver may not achieve a lock at the desired frequency and laser power. For instance, if the two current sources are not matched, then the voltage on Vauto will continue to change after a lock is achieved. This in turn changes the strengths of the reset transistors, which changes the duty cycle to compensate for the ratio mismatch, and settles at some non-50% duty cycle. But if the mismatch is too great, the duty cycle may be forced to be skewed even further, which may cause the receiver to fail. This can be avoided by increasing the size of the current mirror transistors, or having a few bits of tuning capability for one of the current sources. Another feature that could be made automatic is the dark current compensation. Since the photodiode will produce some leakage current in the absence of light, a manually tunable current source to compensate for this DC current was added. The final schematic would be something like Figure 4-15.
Figure 4-15: Schematic of auto-locking clock receiver circuit with dark current compensation and independently tunable current sources for duty cycle correction.

For the purposes of testing this injection-locked auto-tuning concept, the receiver circuit implemented in EOS2 was a single ended circuit which is small in area and power consumption, but obviously more vulnerable to power rail noise. A fully differential version would not only provide power supply noise rejection, but also a higher operation frequency can be possible with analog style differential pairs, at the cost of burning more power. An additional benefit is with a differential connection to the photodiode, the DC voltage across the diode is 0V, hence no dark current to worry about.

4.3 Summary

Here we present the limitations of a traditional TIA receiver, and how to break the bandwidth/sensitivity tradeoff by taking advantage of the fact that this is a clock receiver. Starting with a simple self-reset design, we add on the injection-locked feature, then the auto-tuning capability, resulting in a high speed, low power, low jitter receiver that can adapt to a varying environment.
Chapter 5

EOS2 32nm Test Chip

5.1 EOS2 Chip Overview

We completed a test chip in the 32nm process with all the components mentioned in the photonic technology section, shown in Figure 5-1. To characterize waveguide loss, we have sets of waveguides of various lengths with identical bends. Thus by measuring the losses of a set of waveguides, we can decouple the insertion losses of the vertical couplers and bending losses, leaving us an accurate loss per centimeter figure. There are also loss rings to measure the loss more accurately if it is very small. Individual modulators and photodetectors are connected to high speed probe pads (GSG pads), for a thorough optical-electrical characterization. Modulator rings are accompanied with heaters, so the relation between frequency shift and temperature can be measured. Due to the fact that this chip is manufactured in a 32nm pilot run, for many of the photonic devices, different designs and sizings are implemented, such that the variation of unknown design parameters such as doping concentration are covered by a design. The hope is that if a design of one set of parameters is tested to be functional, the next iteration of the chip can narrow down the types of variations implemented. In the center of the chip are WDM photonic links connected to transmitter and receiver circuits. We have waveguides that connect modulators and receivers, with heaters for each ring, so multiple channels can operate simultaneously.
Figure 5-1: Layout view of EOS2 test chip. Sandwiched between loss measurement structures and individually testable optical devices are the circuit/photonic WDM rows. The chip dimensions are 2mm by 2mm.
5.2 EOS2 Cell

Figure 5-2: Layout view of circuit cell of EOS2 with photonic devices. Note the relative size of the vertical couplers, rings and spacing between photonics and circuits. Also note the row of etch vias below the photonics. The circuit cell dimensions are 220μm by 40μm.

Since we plan to run the links at 5Gb/s, we have all our test structures on chip, including a programmable PRBS to generate the data sequence for the modulator, a data snapshot and counter for error checking, and many registers to store configuration bits for the modulator and both data and clock receivers. With most of the digital infrastructure on the chip, no high speed outputs are required, and we are area limited in how many devices we are able to implement and test, instead of being pad limited. This digital infrastructure with analog blocks is denoted as a "cell", a block diagram is shown in Figure 5-3, and a layout view with the adjacent photonics is shown in Figure 5-2. For ease of layout and verification, one unique cell is created, and then repeated in rows. The photonics, whether WDM links or individual test structures, are then connected to the regularly spaced pin locations of the clock receivers, data receivers and modulators, making the hookup process simple and easy to verify.
All scan signals and high speed clocks were buffered in each cell, and then passed on to the next cell in each row. This is fine for low speed scan signals as long as we avoid hold time violations, but unfortunately for high speed clocks, the jitter and duty cycle will deteriorate further down the chain. This problem has been fixed in the latest chip.
5.3 EOS2 Testing

5.3.1 Clock Receiver Testing

The testing infrastructure is set up to measure the output clock frequency of the receiver circuit relative to an off chip high speed clock source. The implementation is shown in Figure 5-4. The two asynchronous counters are initially set to all zeros, then the high speed inputs are enabled from the configuration registers. The counter count the number of cycles, until the MSB of the reference counter changes to 1. This is the shutoff signal that quickly stops the input signals from coming in. By reading out and comparing the two counter values, we can measure the frequency ratio between the reference clock and the received clock. For instance, if both clocks are matched, then they should both read out the same value. There will be some offset in the counter value, since the overflow propagates through every counter bit and then shuts off the clock input, so a few extra cycles will be counted. This offset is a fixed delay in time, and can be easily calibrated out.

Also, as a backup in case the photodetectors do not work as well as planned, and for
debugging purposes, an electrical pulsed current source can be enabled as the input to the clock receiver circuit. This self test circuit is driven by a high speed clock, and the pulse strength and width can be configured to mimic different photodiode current profiles.

Measuring the relative frequencies allows us to know whether or not the receiver is properly locked, but to do jitter measurements, a more sophisticated test circuit is required. In a later chip, the receiver circuit output is also sampled with a reference clock, so by adjusting the relative phases, we can derive a cumulative histogram of received clock edge phases with respect to the reference clock.

5.3.2 Chip Testing

All scan chain control signals are connected to an FPGA board, with a state machine that can interface with a python command set. The functions include resetting the chip, reading out the cell values of a target cell, writing a user defined configuration to a target cell. Although the scan chain is about 20000 registers long, the FPGA can operate at a MHz frequency, so each operation only takes a fraction of a second. When reading and writing a target cell, the values of the other cells are preserved, this allows us to configure multiple cells easily. An example of a write operation is shown in Figure 5-5.

To perform a purely electrical clock receiver test, we configure a target cell to have the self test circuit enabled, clock receiver enabled, and high speed clocks enabled. After the experiment is done, we read out the counter values of that target cell and adjust the clock receiver configuration if necessary. Once we have confidence the circuits work with the electrical self test, we can move the chip to our optical table to perform full optical/electrical tests. For the clock receiver, this includes using a mode-locked laser as the clock source, and a modulated single wavelength laser source.
<table>
<thead>
<tr>
<th>Time</th>
<th>Cell 0</th>
<th>Cell 1</th>
<th>Cell 2</th>
<th>Cell 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>D</td>
<td>A</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>2</td>
<td>New</td>
<td>D</td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>3</td>
<td>B</td>
<td>New</td>
<td>D</td>
<td>A</td>
</tr>
<tr>
<td>4</td>
<td>A</td>
<td>B</td>
<td>New</td>
<td>D</td>
</tr>
</tbody>
</table>

Figure 5-5: Here we write the value "New" to Cell 2, while preserving the values of the other cells. This is done by feeding back the last bit of the scanchain into the input, and only feeding in new data at the right time.

## 5.4 Summary

In this chapter we give an overview of the features in the EOS2 chip, the electrical cell architecture, and the procedures to test the chip. The key is to have most of the digital infrastructure on the chip, so no high speed outputs are required, and we can test as many devices as we can fit. When designing a chip with both photonics and digital backend of this complexity, we see the need to fully integrate the photonics into our CMOS design flow. This includes parametrized layout generation for photonic components, photonic cell preparation for automatic place and route, and post route design rule checking and connectivity checking. The issues will be addressed in the next chapter.
Chapter 6

Integrated CMOS/Photonic Chip Design

For an electronic/photonic chip to be designed in a truly integrated fashion, there must be a photonic equivalent to every step of the CMOS design flow. These include parametrized layout generation or p-cells, macro preparation for automated place and route, design rule checking (DRC) and layout vs. schematic checking (LVS).

6.1 Parametrized photonic layout generation and optimization

In this project, we have used p-cells to draw the photonic devices [14]. A p-cell lets the designer to input the design parameters of a device, and reflects the changes in the layout immediately. For instance, for a waveguide bend, the user and specify the waveguide width, bend radius, bend angle, etc. More parameters can be added later on if more degrees of freedom are needed. In stream-out, Cadence merges rectangles into many-vertex polygons (max 4000 vertices). So this means we can draw polygons with many vertices. One major benefit is redundant vertices are minimized, saving disk space. Also, Cadence displays simplified polygons when zoomed out, so the screen refreshes faster in a complex design. This effect is shown in Figure 6-1.
6.2 Design Automation of Electric and Photonic Integrated Circuits

For most commercial digital chips, the physical layout is done automatically with CAD (Computer Assisted Design) tools. The user starts with a behavioral description of the chip in Verilog that describes the functionality of the chip, then proceeds to synthesize the chip into a gate level design, where we have a netlist of logic gates. The next procedure is floorplaning, where the designer places the power wires, pads, and higher level module blocks of the chip. Finally a detailed place and route is performed, where the standard cell layout corresponding to each logic gate are placed and wired up. Modern CAD tools let the user adjust the optimization parameters, such as area, clock frequency, signal integrity etc, and warn the designer of bottlenecks and violations, so that many iterations can be quickly made, saving the designer a significant amount of time.

For photonics to be integrated in a complex chip, it also needs to be compatible with this CAD tool flow. A straightforward solution is to treat photonic blocks the same way as we treat logic gate standard cells. This integrated electric and photonic circuit design flow is shown in Figure 6-2. So the only additional step is to create a
Chip-level verilog (instantiation of .LEF macros and connectivity)
Figure 6-3: Layout view of example ring modulator

Figure 6-4: Abstract view of example ring modulator. Note that lower level metal features such as metal fill have been blocked out, since port connections are made at higher levels.
Figure 6-5: Abbreviated macro description in LEF format of example ring modulator.
6.3 Simple design check using LVS and DRC

As we try to build truly integrated photonic-electrical circuits, LVS capability is crucial, since humans can only be error-free up to a certain complexity level. To indicate optical connectivity, we can use a layer that is unused by the electrical process, so the optical and electrical nets are independent of each other. We also add additional layers to help us extract optical devices and their parameters. Thus the extraction tool will be able to recognize photonic devices and compare the layout (Figure 6-6) with the designed schematic (Figure 6-7).

In addition to checking connectivity, by making the optical connectivity layer wider than the actual waveguide, LVS will detect a short if two waveguides are too close to each other. Additional DRC checks may be made by adding rules to the DRC rules file. For example, we can check if the waveguides have the proper silicide, metal fill and dopant blocking layers overlapping them.
6.4 Summary

This chapter focuses on the integration of photonics with circuits from a design perspective. Using existing tools, we develop methods to draw photonic devices, verify the circuit and include the photonic devices within a standard CMOS place and route flow.
Chapter 7

Conclusion and Future Work

7.1 Conclusion

The bottleneck of multi-core processors performance will be the I/O, for both on-chip core-to-core I/O, and off-chip core-to-memory. Integrated silicon photonics can potentially provide high-bandwidth low-power signal and clock distribution for multi-core processors, by exploiting wavelength-division multiplexing. This thesis presents the technology environment of the monolithic optical/electrical chip, and then focuses on how an optical method would look like for both source-synchronous link and for on-chip global clock distribution. The injection-locked loop clock receiver that suits this architecture breaks the bandwidth/sensitivity tradeoff, and a self adjusting mechanism is added to increase robustness. The simulated receiver sensitivity is -14dBm at 9GHz, consuming 77.14μW and generating jitter within 0.15ps when locked onto a mode-locked laser clock source. We then present the chip infrastructure and testing procedures, also methods to make the photonic device design more compatible with a CMOS circuit design flow, putting us closer to true integration.

7.2 Future Work

As already mentioned in chapter 4, a fully differential receiver circuit would be less vulnerable to power supply noise, and can potentially operate at a higher frequency.
Another technique to explore is to have a frequency dividing mechanism for the reset, so the electrical clock frequency can be an integer multiple of the input optical clock source. Although the jitter will increase since the phase noise is not cleaned up every cycle, this will allow us to use mode-locked lasers of a lower repetition rate, which are more easily accessible.

Another improvement that is orthogonal to the two mentioned above, is to explore the possibility of using a phase comparator as the reset/precharge strength tuning mechanism. This will help us decouple the two features that we wish to tune, frequency and duty cycle, and provide a larger range of operation. For instance, in the current design, if the optical input frequency is much lower than the designed range, the duty cycle will be much less than 50% if locked, so the auto tune will push itself out of lock. However if we use a phase comparison mechanism, it will stay locked once a lock is achieved, and can proceed to fix the duty cycle. The receiver would still rely on the injected clock source to clean up the phase noise, so the jitter would still be much better than a PLL.
Bibliography


