A Fractionally Spaced Linear Receive Equalizer with Voltage-to-time Conversion

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BW limited channels challenge CDR and EQ

- Trace routing
- Manufacturing
- Temperature & humidity

Equalization and synchronization dominate link performance and power efficiency
Interaction between data and synchronization paths in conventional designs

- Problem:
  - Equalize on $d_n$; synchronize on $e_n$
  - EQ and CDR do NOT work to optimize the same performance metric
Overcoming the limitations

• Performance improvement by joint equalization and phase recovery

• Fractionally spaced equalization (FSE) can do both for mesochronous system
  – Architecture
  – Implementation
  – Measurements
FSE concept

- Phase critical for symbol spaced RX
- FSE compensates phase offset by interpolating samples
FSE robustness to phase offset

- Example
  - 4-tap 2X oversampled FSE @ 6Gbps rate

17 dB attenuation at Nyquist rate
FSE implementation challenges and options

• Challenges
  – 4~5 bit linearity for large DR
  – Two samples per symbol period: efficiency

• Options
  – CML technique
  – Voltage-time conversion technique*
    
    \[ V2T: \text{voltage-to-time converter} \]
    
    \[ T2V: \text{time-to-voltage converter} \]

Voltage conversion technique comparisons (1)

- **CML with source degeneration**
  - Good linearity with small input signals
  - Bad linearity given large input dynamic range

- **V2T**
  - Convert by current integration
  - Current sources determine the linearity
Voltage conversion technique comparisons (2)

- **CML with source degeneration**
  - Bad linearity when $I_1 << I_2$ & large input DR

- **V2T**
  - Timing inputs $ed_{x\pm}$ are digital
    - More headroom at $V_{O+}/V_{O-}$
  - >25% power saving than CML
    - 1.0V VDD & >5bit linearity
Proposed fractionally spaced equalizer structure

- 2 way interleaving
- 2X oversampling
- 2 feed forward taps
Voltage-to-time converter

\[ \Delta t = a\Delta V_{in} \]
**V2T — track & preset phase**

![ Circuit Diagram ]

- **$E_{1r+}$**, **$E_{1f+}$**: Switches
- **$Sign Mux$**: Switch for sign inversion
- **$V_{in+}$**, **$V_{in-}$**: Input voltages
- **$V_{1x+}$**, **$V_{1x-}$**: Intermediate voltages
- **$V_{1s+}$**, **$V_{1s-}$**: Final voltages
- **$C_S$**: Capacitors
- **$N_+$**, **$N_-$**: Nodes
- **$P_+$**, **$P_-$**: Transistors

**Data Diagram**

- **$D_0$**: Data waveform
- **$V_{1x+}/V_{1x-}$**, **$V_{1s+}/V_{1s-}$**: Voltage waveforms
- **$V_{th}$**: Threshold voltage
- **$V_{th} \approx 300mV$**

**Additional Details**

- **$Φ_2$**: Timing phases
- **Tx-Rx delay**: Transmission delay

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**Equations**

- $V_{th} \approx 300mV$
**V2T — evaluation phase: sample & level shift**

Data

- $\Phi$
- $\Phi_2$
- $V_{1x+}/V_{1x-}$
- $V_{1s+}/V_{1s-}$
- $E_{1r+}/E_{1f+}$
- $E_{1r-}/E_{1f-}$

$V_{th} \approx 300 \text{mV}$

$Tx-Rx$ delay

$D_0$
$\Delta t = a \Delta V_{\text{in}}$
\[ \Delta V_O = \mu \Delta t I_1 = \mu \alpha \Delta V_{in} I_1 \]
T2V for one tap — preset

T2V for CH+  T2V for CH-

M_{PRE+}  M_{PRE-}

V_{o+}  V_{o-}

E_{r+}  E_{r-}

E_{f+}  E_{f-}

M_{+}  M_{-}

\Phi

I_1

C_{o+}  C_{o-}

Vo+/Vo-
T2V for one tap — evaluation: common pull-down

\[ V_{o+} \]
\[ V_{o-} \]

\[ M_{PRE+} \]
\[ M_{PRE-} \]

\[ C_{o+} \]
\[ C_{o-} \]

\[ I_1 \]

\[ \Phi \]

\[ E_{r+} \]
\[ E_{f+} \]
\[ E_{r-} \]
\[ E_{f-} \]

\[ V_{o+/Vo-} \]
T2V for one tap — evaluation: differentiate

\[ T2V \text{ for CH}^+ \quad T2V \text{ for CH}^- \]

\[ E_r^+ \quad E_r^- \quad \Delta t \quad \Phi \]

\[ M_{PRE+} \quad M_{PRE-} \quad \Phi \quad I_1 \quad M_+ \quad M_- \]

\[ V_{o+} \quad V_{o-} \quad C_{o+} \quad C_{o-} \quad I_1 \quad I_1 \quad \Phi \quad I_1 \]

\[ E_{f+} \quad E_{f-} \quad V_{o+/o-} \quad E_{r+} \quad E_{r-} \]

\[ \text{T2V for CH}^+ \quad \text{T2V for CH}^- \quad \text{CO}^+ \quad \text{CO}^- \quad I_1 \quad I_1 \]

\[ \Phi \quad \Delta t \]

\[ E_{f+} \quad E_{f-} \quad V_{o+/o-} \]
$\Delta V_o = \mu \Delta t I_1$

$= \mu a \Delta V_{in} I_1$
• **Discharge currents are shared between even & odd ways**
• Scan-chain/snapshot for in-situ link margin characterization
Tap weight linearity measured @ 4Gbps rate

- 4.3 effective bits linearity in tap weights
  - Monotonic gain
- 8 mW power consumption w/ 1.2 V supply
  - @ 4Gbps
Phase robustness is shown @ 4Gbps rate

- ±5% eye open variation
  - Gain mismatch of factor 2 between $I_1$ and $I_2$
  - Tap weights are tuned
Conclusions

- FSE integrates EQ and phase interpolation
  - Leverage process speed vs. channel BW

- A two-tap FSE receiver is shown
  - Robust against phase offset
  - Voltage-to-time technique scales well compared to CML
    - 4.3 effective bit linearity @ ±400 mv input DR
    - 2 pJ/bit power efficiency @ 4 Gbps
Acknowledgement

• National Semiconductor Corporation
• Center for Integrated Circuits and Systems (CICS) at MIT
• Trusted Foundry for chip fabrication
• Fred Chen