Design of High-Speed Links: 
A look at Modern VLSI Design

Vladimir Stojanović

Integrated Systems Group
Massachusetts Institute of Technology
Chip design is changing

- Becoming constrained by power
  - Not so much by area/density

Pentium
- 3M transistors
- 30mW/mm²
- 0.6um tech
- 4W
- 0.1GHz

Pentium 4
- 125M transistors
- 850mW/mm²
- 90nm tech
- 103W
- 3.4GHz

- Best systems trade-off circuits, architecture and system issues
Power-performance system optimization

- Complex, many levels of hierarchy and variables
Power-performance system optimization

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Individual components
Flops & latches
(power and timing critical)

Power-performance system optimization

- Complex, many levels of hierarchy and variables

Individual components
Flops & latches
(power and timing critical)

System level,
VLSI blocks and circuits
- Physical (Vdd, Vth, Sizing)
- Logic
- uArchitecture
(parallelism, pipelining)

V. Stojanovic, D. Markovic, B. Nikolic, M. A. Horowitz and R. W. Brodersen
Seems pretty simple:

- Challenging multi-disciplinary area
  - Circuits
  - Communications
  - Optimization
What makes it challenging

- Now, the bandwidth limit is in wires
- High speed link chip
- > 2 GHz signals
New link design

Dealing with bandwidth limited channels

- This is an old research area
  - Textbooks on digital communications
  - Think modems, DSL
- But can’t directly apply their solutions
  - Standard approach requires high-speed A/Ds and digital signal processing
  - 20Gs/s A/Ds are expensive
- (Un)fortunately need to rethink issues
Outline

- Show system level optimization for links
  - Create a framework to evaluate trade-offs

- Background on high-speed links
- High-speed link modeling
- System level optimization
- Practical implementation issues
- Current / future work
Backplane environment

- Line attenuation
- Reflections from stubs (vias)
Backplane channel

- Loss is variable
  - Same backplane
  - Different lengths
  - Different stubs
    - Top vs. Bot

- Attenuation is large
  - >30dB @ 3GHz
  - But is that bad?

- Required signal amplitude set by noise
Inter-symbol interference (ISI)

- Channel is low pass
  - Our nice short pulse gets spread out

- Dispersion – short latency
  (skin-effect, dielectric loss)

- Reflections – long latency
  (impedance mismatches – connectors, via stubs, device parasitics, package)
Middle sample is corrupted by 0.2 trailing ISI (from the previous symbol), and 0.1 leading ISI (from the next symbol) resulting in 0.3 total ISI.

As a result middle symbol is detected in error.
Prior state of high-speed links

- Links components well developed
  - Fast multiplexed transmitters and receivers
  - Precise timing generation and data recovery
- Starting to use equalization (1 – 2 taps)
  - Few taps set manually at the transmitter
Barriers to improving link performance

- No good link system and noise models
  - Cannot predict the “right” architecture for a given set of channels
  - Need to make performance/power tradeoff

- Maximum achievable data rates – unknown
  - Limited link communication system design

- Peak power constraint in the transmitter
  - No solution for optimal transmit equalization
  - No solution for automatic equalization
Previous system models

- Mostly non-existent
- Borrowed from computer systems
  - Worst case analysis
    - Can be too pessimistic in links
- Borrowed from data communications
  - Gaussian distributions
    - Works well near mean
    - Often way off at tails
      - ISI distribution is bounded
- Need accurate models
  - To relate the power/complexity to performance
How bad is Gaussian model?

- Gaussian model only good down to $10^{-3}$ probability
- Way pessimistic for much lower probabilities
A new model

- Use direct noise and interference statistics

- Main system impairments
  - Interference
  - Voltage noise (thermal, supply, offsets, quantization)
  - Timing noise – always looked at separately
    - Key to integrate with voltage noise sources
    - Need to map from time to voltage
Effect of timing noise

- The effect depends on the size of the jitter, the input sequence, and the channel
- Need effective voltage noise distribution
Example: Effect of transmitter jitter

- Decompose output into ideal and noise
- Noise are pulses at front and end of symbol
  - Width of pulse is equal to jitter
- Approximate with deltas on bandlimited channels

Jitter effect on voltage noise

- **Transmitter jitter**
  - High frequency (cycle-cycle) jitter is bad
    - Changes the energy (area) of the symbol
    - No correlation of noise sources that sum
  - Low frequency jitter is less bad
    - Effectively shifts waveform
    - Correlated noise give partial cancellation

- **Receive jitter**
  - Modeled by shift of transmit sequence
  - Same as low frequency transmitter jitter

- **Bandwidth of the jitter is critical**
  - It sets the magnitude of the noise created
Jitter source from PLL clocks

- Noise sources
  - Reference clock phase noise
  - VCO supply noise
  - Clock buffer supply noise


2x Oversampled bang-bang CDR

- Generate early/late from \(d_n, d_{n-1}, e_n\)
  - Simple 1\(^{st}\) order loop, cancels receiver setup time
- Now need jitter on data Clk, not PLL output
  - Base linear PLL jitter
  - Add non-linear phase selector noise from CDR
Bang-bang CDR model

- Model CDR loop as a state machine – Markov chain

- Gives the probability distribution of phase
  - Which is the CDR jitter distribution

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- System level optimization
  - Limits – What is the capacity of these links?
  - Improving today’s baseband signaling

- Practical implementation issues

- Current / future work
Baseline channels

- Legacy (FR4) - lots of reflections
- Microwave engineered (NELCO)
Capacity with link-specific noise

- Effective noise from phase noise
  - Proportional to signal energy
  - Decreases expected gains
- Still, capacity much higher than data rates in today’s links
Removing ISI

Transmit and Receive Equalization

- Changes signal to correct for ISI
- Often easier to work at transmitter
  - DACs easier than ADCs

Transmit equalization – headroom constraint

- Transmit DAC has limited voltage headroom
- Unknown target signal levels
  - Hard to formulate error or objective function
- Need to tune the equalizer and receive comparator levels

Amplitude of equalized signal depends on the channel
Optimization example: Power constrained linear precoding

Add variable gain to amplify to known target level
- Formulate the objective function from error
- $SINR$ is not concave in $\mathbf{w}$ in general
- Change objective to quasiconcave $\sqrt{SINR_{\text{unbiased}}}$

V. Stojanović, A. Amirkhany, M. Horowitz, “Optimal Linear Precoding with Theoretical and Practical Data Rates in High-Speed Serial-Link Backplane Communication,” IEEE International Conference on Communications, June 2004
Optimal linear precoding

Still, does this objective really relate to link performance?

Need to look at noise and interference distributions

\[
\begin{align*}
\text{maximize } & \gamma = \\
& \frac{0.5d_{\min} \mathbf{w}^T \mathbf{P} \mathbf{1}_\Delta ^{-1} - V_{\text{peak}} \| \mathbf{w} \mathbf{P} \mathbf{I}_{PD} \|_1 - \text{offset}}{\left( E_a \mathbf{w}^T \mathbf{P} (\mathbf{I} - \mathbf{1}_\Delta ^{-T} \mathbf{I}_{PD}) (\mathbf{I} - \mathbf{1}_\Delta ^{-T} \mathbf{I}_{PD})^T \mathbf{P}^T \mathbf{w} + \sigma^2 \right)^{1/2}} \\
\text{s.t. } & \| \mathbf{w} \|_1 \leq 1
\end{align*}
\]

Minimize BER

- Residual dispersion into peak distortion
- Reflections into mean distortion

Includes all link-specific noise sources
Including feedback equalization

- Feedback equalization (DFE)
  - Subtracts error from input
  - No attenuation

- Problem with DFE
  - Need to know interfering bits
  - ISI must be causal
    - Problem - latency in the decision circuit
    - Receive latency + DAC settling < bit time
  - Can increase allowable time by loop unrolling
    - Receive next bit before the previous is resolved
One-tap DFE with loop unrolling

Pulse response

+1

0

-1
One-tap DFE with loop unrolling

\[
\begin{align*}
1 & \quad +1 + \alpha \\
\alpha & \\
0 & \quad +\alpha \\
-1 & \quad -1 + \alpha
\end{align*}
\]
One-tap DFE with loop unrolling
Instead of subtracting the error

- Move the slicer level to include the noise
- Slice for each possible level, since previous value unknown

Ber contours

- Voltage margin
  - Min. distance between the receiver threshold and contours with same BER
Pulse amplitude modulation

- **Binary (NRZ)**
  - 1 bit / symbol
  - Symbol rate = bit rate

- **PAM4**
  - 2 bits / symbol
  - Symbol rate = bit rate/2
Multi-level: Offset and jitter are crucial

- To make better use of available bandwidth, need better circuits
- PAM2/PAM4 robust candidate for next generation links
Full ISI compensation too costly

- Today’s links cannot afford to compensate all ISI
  - Limits today’s maximum achievable data rates
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  - Low-cost adaptation
  - Dual-mode link (hardware re-use)
- Current / future work
Fully adaptive dual-mode link

- PAM2/PAM4
- 2-10Gb/s
- 0.13µm
- 40mW/Gb/s

Reconfigurable dual-mode PAM2/PAM4 link

- Adaptive equalization
- Transmit and receive equalization
- DFE with loop unrolling

Adaptation with minimum overhead

- Adaptive sampler
  - Generates the error signal at reference level
- Monitors the link
  - Adjustable voltage and time reference
  - On-chip sampling scope
- Can replace any other sampler - calibration
Dual-loop adaptive algorithm

- **Data level reference loop**
  \[ d\text{Lev}_{n+1} = d\text{Lev}_n - step_{\text{dataLev}} \text{sign}(e_n), \quad \hat{x}_n > 0 \]

- **Equalizer loop**
  \[ \underline{w}_{n+1} = \underline{w}_n + step_w \text{sign}(e_n) \text{sign}(\hat{x}_n) \]

- **Scale the equalizer - output Tx constraint**
Dual loop convergence – 4 tap example

- Hard to estimate analytically
- Experimental results show
  - Both loops are stable within wide range 0.1 – 10x of relative speeds

PAM2, 5Gb/s, 4taps Tx Equalization
Hardware re-use: Dual-mode receiver

- PAM4
Hardware re-use: Dual-mode receiver

- PAM4

- Pre-amp with offset

- Comparator

- PrDFE enable

- Lsb(+)

- Msb

- InP

- OutP

- InN

- OutN

- Threshold (+)

- Threshold (-)

- In

- Dclk

- Clk

- Pre-amp with offset
Hardware re-use: Dual-mode receiver

- PAM2
Hardware re-use: Dual-mode receiver

- PAM2 with loop-unrolled DFE tap
Hardware re-use: Dual-mode receiver

- PAM2 with loop-unrolled DFE tap
  - Leverage multi-level properties of signals in loop-unrolling
  - Re-use PAM4 receiver hardware (slicers and CDR)
Improvements with loop-unrolling

Signal as seen by the receiver (on-chip scope)
Model and measurements

- PAM4, 3 taps of transmit equalization, 5Gb/s, 26” FR4 channel
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  - Bridging the gap to link capacity
  - Other similar system optimizations
Bridging the gap: Multi-tone link

Bridging the gap: Multi-tone link

- Challenge – balancing the inter-symbol and inter-channel interference
  - Microwave filter techniques
  - Custom signal processing
The Problem with Multi-Mode Fiber

Multi-modal dispersion limits the data rates to ~ 3Gb/s/km
Example Fiber Modes

- Two 3D plots showing different fiber mode patterns.
- Axes range from $-5 \times 10^{-5}$ to $5 \times 10^{-5}$.
- The plots illustrate the intensity distribution of different fiber modes.
SLM’s for Equalization

- Shape the E-field projected on the fiber
- Lens performs Fourier Transform
  - SLM’s adjust the spatial frequency of the light
- Optimize to reduce modal dispersion
  - Objective is intensity – makes optimization challenging

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E. Alon, V. Stojanovic, J. M. Kahn, S. Boyd, M. Horowitz

“Equalization of Modal Dispersion in Multimode Fiber using Spatial Light Modulators,”
Conclusions

- Interfaces are challenging system designs
  - Good space to explore system level optimization

- Optimization leads to novel approaches
  - Baseband links
    - PAM4 and simple DFE reduce effect of ISI
    - Low cost adaptive, self-calibrating link
  - Still, far from the capacity of these links
    - Looking into multi-tone to bridge the gap
  - Multimode fiber optics
    - Leverage multiple propagation modes rather than being limited