Integrated Systems

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Introduction

Integrated Systems Group is focused on several key design aspects of modern integrated systems. The group is focused on building cutting edge, energy-efficient integrated systems through vertical optimization encompassing communications and signal processing algorithms and architectures, and digital and mixed-signal circuits, as well as early interaction with research on novel devices. This early circuit design with novel devices, such as nano electro mechanical relays or silicon photonic devices, provides both a general framework for the evaluation of device impact on future VLSI systems as well as drives the roadmap and feedback to the device researchers.

Most integrated systems today are limited by tight power and/or throughput constraints. In this environment, the usual system hierarchy becomes inefficient and novel vertical system design approaches are needed to create overall most efficient integrated systems. We believe that this can be achieved by blurring of the strict hierarchy boundaries and modification of standard communication techniques and circuits to perform the operations in a most energy-efficient way.
On one hand, this system-to-circuit approach helps further the efficiency improvement in CMOS-based integrated systems that has otherwise slowed due to technology scaling. On the other, the circuit-to-novel device approach helps investigate the potential performance benfits of the emerging device technology as well as impacts their further development. Some examples of these tightly constrained systems that we are interested in are high-speed electrical and optical interfaces, on-chip signaling and networks, memory systems, as well as implantable sensor systems.

1. A 6.25-Gb/s Adaptive Fractionally Spaced Receive Equalizer with Voltage-time Conversion

Project Staff
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Center for Integrated Circuits and Systems (CICS) at MIT

This work describes an architecture and circuit implementation of a fractionally spaced equalizer (FSE) receiver [1], built to unify equalization and phase synchronization in high-speed links, as shown in Figure 1. To achieve the desired linearity for adaptation with good energy efficiency, large input dynamic range, and high operation rate, the FSE is designed using a voltage-time conversion technique [2]. The proposed auto-zero inverter-based threshold detectors are able to

compensate for the detection threshold mismatch while converting voltage signals to timing signals, a trait missing in [1]. A two-tap quad-rate FSE receiver with one-tap DFE is fabricated in 90-nm bulk CMOS technology, occupying a 0.03 mm^2 active area. With a 1.2-V supply, it achieves a 6.25-Gbps rate, 3.6-pJ/bit efficiency and 5 effective bits of linearity.

A modified sign-sign LMS adaptive algorithm is used to tune the FSE tap weights to mitigate the inter-symbol interference (ISI) for the arbitrary receiver phase. Based on data conditioning, it reduces the quantization noise and overcomes divergence issues of the traditional FSE sign-sign LMS algorithm.

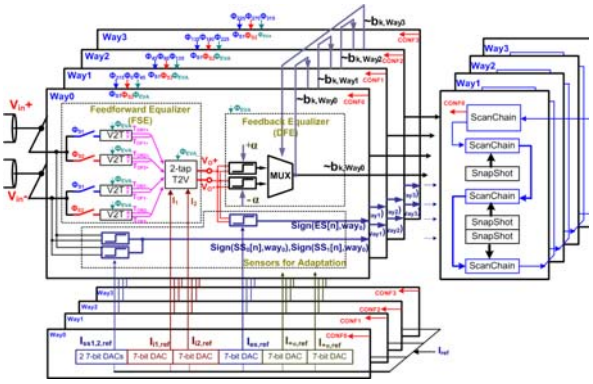

Figure 1: Architecture of the 4-way interleaved 2-tap FSE and 1-tap DFE receiver with on-chip adaptation sensors. Scan-chain and snapshot are applied for in-situ link characterization and the off-chip adaption experiment.

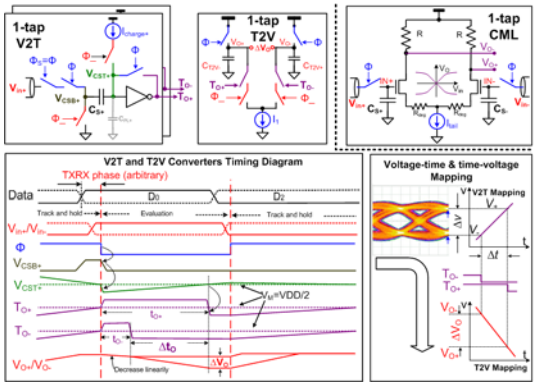

Figure 2: FIR tap implementation concept with CML and V2T technique. For CML implementation, the transconductance of the input devices determines the linearity, while for the V2T implementation, the charge current $I_{charge+/-}$ determines the linearity.

References

[1] S. Song, B. Kim, and V. Stojanović, "A Fractionally Spaced Linear Received Equalizer with Voltage-to-Time Conversion," IEEE Symposium on VLSI Circuits Dig. Tech. Papers, June 2009.

[2] L. Brooks and H.-S. Lee, " A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC," IEEE Journal of Solid State Circuits, Dec. 2007.

2. A Compressed Sensing Acquisition System for Wireless and Implantable Sensors

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In this work, we present the design and implementation of a new sensor-system architecture (Fig. 1) based on the theory of compressed sensing (CS) [1] that addresses both the energy and telemetry bandwidth constraints of wireless and implantable sensors. This approach reduces the average radio power by exploiting signal sparseness to encode the data at a high compression factor (~40x) while enabling a faithful reconstruction of the entire original signal. The reconstruction process also enables power reduction in the frontend circuitry by relaxing the noise and resolution requirements of the AFE and ADC by nearly an order of magnitude. An efficient implementation of the CS sampling is realized in a 90-nm CMOS process and consumes 1.9μW

at 0.6V and 20kS/s [2].

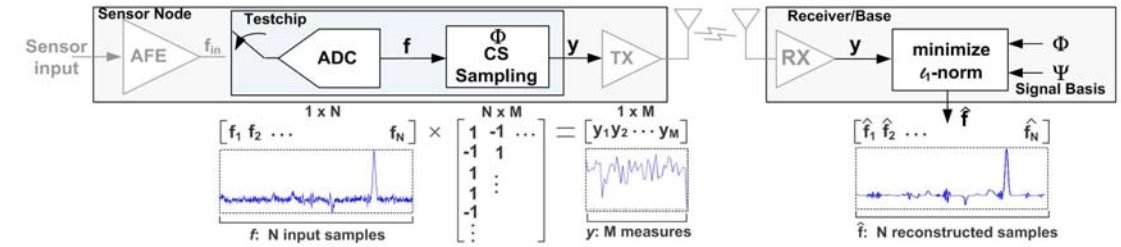

Figure 1: Link Architecture.

References

[1] D. Donoho, "Compressed sensing," *IEEE Transactions on Information Theory*, vol. 52, 2006, pp. 1289–1306.

[2] F. Chen, A. P. Chandrakasan, V. Stojanović, "A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors", to appear in *IEEE Custom Integrated Circuits Conference*, 4 pages, September 2010.

3. Design of Integrated Micro-Electro-Mechanical (MEM) Relay Circuits for VLSI Applications

Sponsors

Defense Advanced Research Projects Agency (DARPA), MIT Center for Integrated Circuits and Systems (CICS), Center for Circuit and System Solutions (C2S2)

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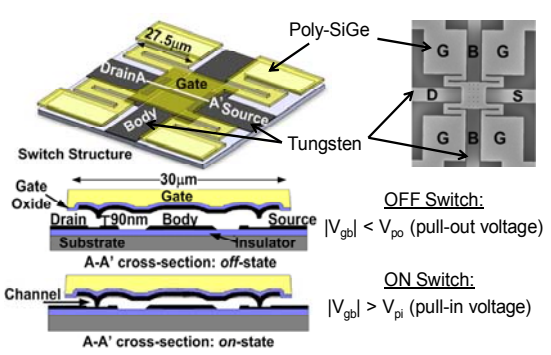
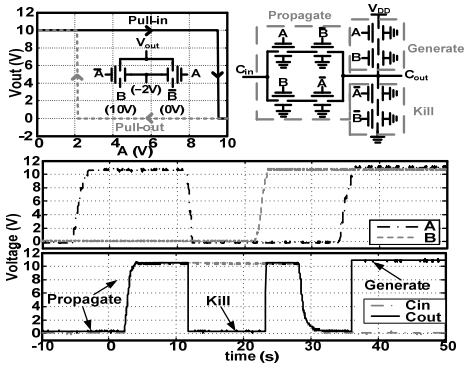
Silicon CMOS circuits have a well-defined lower limit on their achievable energy efficiency due to subthreshold leakage. Once this limit is reached, power constrained applications will face a cap on their maximum throughput independent of their level of parallelism. Avoiding this roadblock requires an alternate device with steeper sub-threshold slope – i.e., lower VDD/Ion for the same Ion/Ioff [1]. One promising class of such devices is electro-statically actuated micro-electro-mechanical (MEM) relays with nearly ideal Ion/Ioff characteristics. Although mechanical movement makes MEM relays significantly slower than CMOS, they can be useful for a wide range of VLSI applications by reexamining traditional system- and circuit-level design techniques to take advantage of the electrical properties of the device. Unlike in CMOS circuit design, logic functions in MEMS circuit design should be implemented as a single complex gate with minimum-sized relays, resulting in significantly reduced logic complexity.

We have recently shown that with optimized circuit topologies MEM relays may potentially enable ~10x lower energy over CMOS at up to ~0.1GHz frequencies [2]. This work takes initial steps towards experimental validation of these principles by leveraging recently developed relay technology and reliability enhancements [3] to demonstrate several monolithically integrated MEM relay-based building blocks. Specifically, our chip includes logic, memory, I/O, clocking and power optimization structures, and we demonstrate successful basic functionality and circuit composition [4,5]. These relay circuits illustrate a range of important functions necessary for the implementation of integrated VLSI systems, and give insight into circuit design techniques that leverage the physical properties of these devices.

This project is a collaboration with research labs of Profs. Tsu-Jae King Liu, Elad Alon (UC Berkeley) and Dejan Markovic (UCLA).





References

[1] H. Kam, et al., "Circuit Level Requirements for MOSFET Replacement Devices," in IEDM Tech. Dig., 2008, pp. 427.

[2] F. Chen, et al., "Integrated Circuit Design with NEM Relays," in IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 750-757, 2008.

[3] R. Nathanael, et al., "4-Terminal Relay Technology for Complementary Logic," in IEDM Tech. Dig., 2009, pp. 223-226.

[4] F. Chen, et al., "Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications," in International Solid-State Circuits Conference (ISSCC Tech. Dig.), pp.150-151, 7-11 Feb. 2010.

[5] H. Fariborzi, et al., "Analysis and Demonstration of MEM-Relay Power Gating", to appear in IEEE Custom Integrated Circuits Conference, Sep. 2010.

Publications

[1] Bond, B., Z. Mahmood, R. Sredojević, Y. Li, A. Megretski, V. Stojanović, Y. Avniel, and L. Daniel, "Compact Modeling of Nonlinear Analog Circuits using System Identification via Semi-Definite Programming and Robustness Certification," *IEEE Transactions on Computer-Aided Design,* August 2010.

[2] Kim, B., V. Stojanović, "An Energy-Efficient Equalized Transceiver for RC-Dominant Channels," *IEEE Journal of Solid-State Circuits*, vol.45, no.6, pp.1186-1197, June 2010.

[3] Orcutt, J. S., A. Khilo, M. A. Popović, C. W. Holzwarth, H. Li, J. Sun, B. Moss, M. S. Dahlem, E. P. Ippen, J. L. Hoyt, V. Stojanović, F. X. Kartner, H. I. Smith, R. J. Ram, "Photonic integration in a commercial scaled bulk-CMOS process," *IEEE International Conference on Photonics in Switching*, Pisa, Italy, pp. 1-2, September 2009.

[4] Chen, F., M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T-J. K. Liu, D. Marković, V. Stojanović, and E. Alon, "Demonstration of Integrated Micro-Electro-Mechanical (MEM) Switch Circuits for VLSI Applications," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, pp. 150-151, February 2010.

[5] Beamer, S., C. Sun, Y-J. Kwon, A. Joshi, C. Batten, V. Stojanović, K. Asanović, ”Re-architecting DRAM with Monolithically Integrated Silicon Photonics,” *in Proceedings of the 37th International Symposium on Computer Architecture* (ISCA-37), Saint-Malo, France, pp. 129-140, June 2010.

[6] H. Fariborzi, M. Spencer, V. Karkare, J. Jeon, R. Nathanael, C. Wang, F. Chen, H. Kam. V. Pott, T-J. K. Liu, E. Alon, V. Stojanović, D. Marković, “Analysis and Demonstration of MEM-Relay Power Gating”, to appear in IEEE Custom Integrated Circuits Conference, 4 pages, September 2010.

[7] F. Chen, A. P. Chandrakasan, V. Stojanović, “A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors”, to appear in *IEEE Custom Integrated Circuits Conference*, 4 pages, September 2010.

[8] F. Chen, A. P. Chandrakasan, V. Stojanović, “A Low-power Area-efficient Switching Scheme for Charge-sharing DACs in SAR ADCs”, to appear in *IEEE Custom Integrated Circuits Conference*, 4 pages, September 2010.

[9] R. Sredojević, V. Stojanović, “Digital Link Pre-emphasis with Dynamic Driver Impedance Modulation”, to appear in *IEEE Custom Integrated Circuits Conference*, 4 pages, September 2010.