Compact Virtual-Source Current–Voltage Model for Top- and Back-Gated Graphene Field-Effect Transistors

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***Abstract*—This paper presents a compact model for the current–voltage characteristics of graphene field-effect transistors (GFETs), which is based on an extension of the "virtual-source" model previously proposed for Si MOSFETs and is valid for both saturation and nonsaturation regions of device operation. This GFET virtual-source model provides a simple and intuitive understanding of carrier transport in GFETs, allowing extraction of the virtual-source injection velocity $v_{\rm VS}$, which is a physical parameter with great technological significance for short-channel graphene transistors. The derived I–V characteristics account for the combined effects of the drain–source voltage V_{DS}, the top-gate voltage V_{TGS}, and the back-gate voltage V_{BGS}. With only a small set of fitting parameters, the model shows excellent agreement with experimental data. It is also shown that the extracted virtual-source carrier injection velocity for graphene devices is much higher than in Si MOSFETs and state-of-the-art III–V heterostructure FETs with similar gate length, demonstrating the great potential of GFETs for high-frequency applications. Comparison with experimental data for chemical-vapor-deposited GFETs from our group and epitaxial GFETs in the literature confirms the validity and flexibility of the model for a wide range of existing GFET devices.**

***Index Terms*—Ambipolar transport, device model, graphene field-effect transistors (GFETs), virtual-source carrier injection velocity.**

I. Introduction

GRAPHENE is a 2-D material that has attracted great interest for electronic devices since the demonstration of field-effect carrier modulation in 2004 [1]. Its high mobility, high saturation velocity, and high thermal conductivity make graphene a promising material for the next generation of high-frequency devices [2], [3]. Recently, researchers at IBM have shown the operation of transistors fabricated on epitaxial graphene with the current-gain cutoff frequency f_T of 100 GHz [4]. In addition, ambipolar transport in graphene creates new opportunities for novel device applications [5]–[7]. The 2-D geometry of graphene also makes it highly compatible with existing fabrication technology in the semiconductor industry. Furthermore, the possibility of a large-scale synthesis of graphene by chemical vapor deposition (CVD) and epitaxial growth [8]–[10] makes graphene integrated circuits a feasible reality in the near future. Hence, it is desirable to develop a compact physical model that can provide insight into the carrier transport in graphene devices and enable the use of computer-aided design software to simulate future complex circuits.

Many physical models for electrical charge and conduction in graphene exist [11]–[14]. Most of these, however, focus on the first-principle calculation of band structures, tunneling effects, and carrier transport. These models are generally insufficient or too complex and resource intensive for device- and circuit-level modeling. Over the past few years, a few device-level models have also been proposed for graphene field-effect transistors (GFETs) [15]–[18]. Reference [15] and [16] present two different device-level models for bilayer GFETs with band gaps tunable by a vertical electric field. Reference [17] proposes a low-complexity current–voltage model for Schottky-barrier graphene nanoribbon transistors, and [18] derives a device model for GFETs based on epitaxial graphene on SiC. However, the results of all these models [15]–[18], although giving great insight into the device physics, have not been compared with any experimental data.

A quasi-analytical modeling approach for GFETs with gapless large-area graphene channels is presented in [19]. The model allows the calculation of I–V characteristics, small-signal behaviors, and cutoff frequency of GFETs. Another compact physical model for GFETs was presented in [20] and [21]. This model was derived directly from conventional metal–oxide–semiconductor (MOS) FET models [22]–[24] and gave a qualitative explanation of graphene transistor operation in an ambipolar region. However, the empirical square-root charge-voltage relation used in [20] and [21] does not distinguish between electron and hole charges, preventing quantitative physical insight into device operation in an ambipolar region. In addition, both models (in [19] and in [20] and [21]) are only validated with experimental data from long-channel GFETs ($L_G > 1\ \mu$m). Hence, their applicability to submicrometer short-channel GFETs, which should dominate potential high-frequency electronic applications, still awaits verification.

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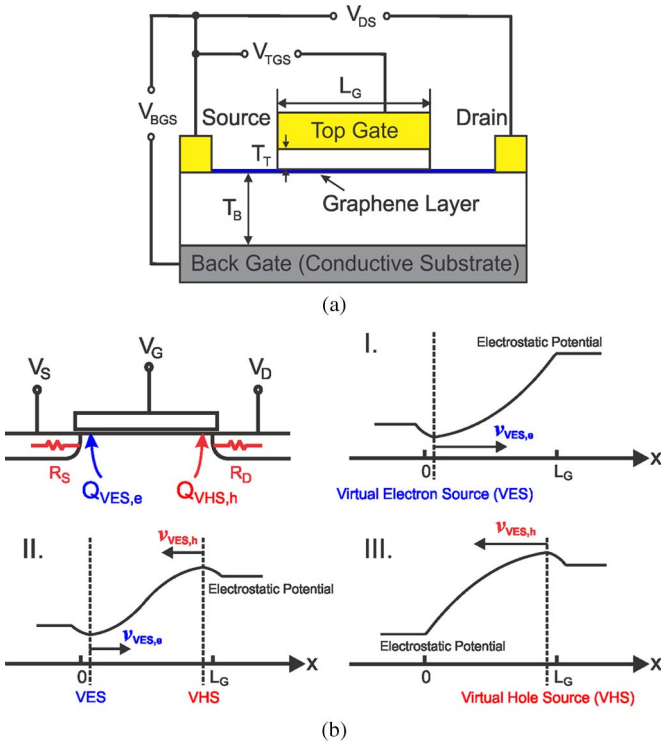

Fig. 1. (a) Diagram of the graphene device analyzed in this paper and the definition of key voltage variables. (b) Schematic of the cross section of the GFET device. The VES and VHS points in the channel are defined for the GFET. The electrostatic potential along the channel and the position of the VES and the VHS are shown for a GFET operating in each of the three operating regions as defined in Fig. 2. Unless it is explicitly stated otherwise, all sheet charge density and carrier velocity for n-type and p-type channels used in this paper are defined at the VES and the VHS, respectively.

Recently, a new class of semiempirical physics-based compact models strictly based on carrier charge and transport has been proposed for short-channel Si MOSFETs [25]–[28]. In this paper, we extend this virtual-source model to GFETs, with the goal of providing a simple and intuitive understanding of the underlying carrier transport in graphene transistors as well as providing the basis for a numerically efficient compact model. The model shows very good agreement with experimental data with only a small set of fitting parameters and is valid for predicting the I–V characteristics of GFETs, accounting for the combined effects of the drain–source voltage V_{DS}, the top-gate voltage V_{TGS}, and the back-gate voltage V_{BGS}.

This paper is organized as follows. Section II presents the formulation of the virtual-source carrier injection model for GFETs. Section III discusses the effects of back gating on the series resistance of GFETs and how to incorporate this into the model. Section IV compares the modeling results to experimental data for dual-gate GFETs fabricated by our group as well as for short-channel GFETs [4] found in the literature. Section V provides the conclusion.

II. Source Injection Velocity Model for the Dual-Gate GFETs

Fig. 1(a) shows the general structure of GFETs and defines the main variables used in this paper. The operation of ambipolar graphene transistors differ significantly from unipolar Si MOSFETs. The channel charges contributing to current are

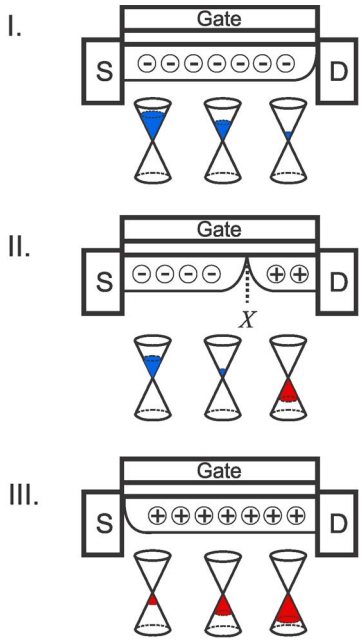

Fig. 2. Conical-shaped band structure and distribution of charge carriers in the channel at different operation regions of GFETs. Assuming that $V_{DS} > 0$, in region I, the device has n-type carriers everywhere in the channel. In region II, the device has n-type carriers at the source side of the channel and p-type carriers at the drain side of the channel. This is the ambipolar region. Point X is the recombination point. In region III, the device has p-type carriers everywhere in the channel.

always electrons in n-channel Si MOSFETs and always holes in p-channel Si MOSFETs in all regions of operation of the devices. In GFETs, however, conduction in this zero-band-gap material is by electrons at a high gate bias when the quasi-Fermi level (for electrons) is above the charge neutrality point at every point in the channel (see region I in Fig. 2) and by holes at low gate biases when the quasi-Fermi level (for holes) is below the charge neutrality point anywhere in the channel (see region III in Fig. 2). However, in the region where the device channel transits from n-type to p-type, conduction is by both electrons and holes. This is called the ambipolar region (see region II in Fig. 2) and is first explained in [20]. Assuming that $V_{DS} > 0$, channel conduction in this region is by electrons injected from the source and holes injected from the drain, which meet and recombine in pairs at a point in the channel. Hence, the channel conduction in GFETs exhibits characteristics of an n-type FET, a p-type FET, and also a transitional ambipolar behavior with both n-type and p-type sections in the channel, depending on bias conditions. The model proposed in this section divides the characteristics of GFETs into these three operation regions. The boundaries between the three operation regions are determined by the position of the recombination point (also called "the minimum charge point" in some literature) along the channel for given bias conditions. Specifically, the device is in the ambipolar region (i.e., region II) if the recombination point exists between the source and the drain in the channel. Otherwise, the device is in region I or III. We will start by deriving the current–voltage relation in each operation region of the device. Then, the position of the recombination point and, hence, the operation region boundaries, will be explicitly derived in Sections II-C

and II-D. It is important to note that while the device is symmetrical, we define here as "source" the terminal that is sourcing electrons (sinking holes) and "drain" the terminal that is sinking electrons (sourcing holes).

A. Device Operation in Region I

When GFETs are operating in region I, only an electron charge is present in the entire channel, and device operation is similar to that in an n-type Si MOSFET. The virtual-source model in [25] can be applied directly to GFETs to describe the conduction in this operation region. At the virtual electron source (VES) defined as shown in Fig. 1(b), we have the following general relation between current $I_{DS,I}$, the channel sheet charge density $Q_{\mathrm{VES},e}$, and the carrier velocity $(v_{\mathrm{VES},e})$ [25], [29], [30] that is valid for both saturation and nonsaturation regions:

$$I_{DS,I}/W = Q_{\mathrm{VES},e} v_{\mathrm{VES},e} F_s \tag{1}$$

where W is the device width, and $v_{\mathrm{VES},e}$ is the local electron carrier velocity at the VES, which is a very important parameter for modern FETs. Its relation to ballistic transport velocity v_θ and its importance in limiting the drive current for devices operating in the quasi-ballistic regime have been discussed in detail in [29]–[32]. In GFETs, injection velocity carries even greater significance due to graphene's long ballistic transport length (≈ 0.3 μm at room temperature [33], [34]).

The virtual-source electron charge density induced by the top gate of GFETs can be approximated by the empirical function in (2) [25]. Equation (2) is adopted from the charge-voltage relation previously used in Si MOSFET models [23]–[25], which, as shown in this paper, also serves well to empirically reproduce the dependence of the charge on the bias voltages in graphene devices as follows:

$$Q_{\mathrm{VES},e} = C_{TG} n \phi_t \ln\left(1 + \exp\frac{V'_{TGS} - V_{t,e}}{n\phi_t}\right) \tag{2}$$

where C_{TG} is the top-gate capacitance per unit area. n is analogous to the subthreshold coefficient in a Si MOSFET, and its value is related to the band gap of the channel material. In GFETs, n typically has much larger values than in Si MOSFETs due to the graphene's zero band gap. This band-gap-dependent term, which is considered as a fitting parameter in this paper, gives additional flexibility to the model, making it also applicable to bilayer GFETs or graphene nanoribbon FETs in which significant band gaps can exist. ϕ_t is the thermal voltage given as $k_B T/q$. V'_{TGS} is the top-gate-to-source voltage of the intrinsic part of the device. $V_{t,e}$ is the effective threshold voltage for a gate-induced electron charge in the channel, which is given as

$$V_{t,e} = V_{TG,\min} + \Delta V \tag{3}$$

where $V_{TG,\min}$ is the top-gate voltage at the point of minimum conductance and is given as (see [20])

$$V_{TG,\min} = V_{TG,\min 0} + \frac{C_{BG}}{C_{TG}}\left(V_{BG,\min 0} - V'_{BGS}\right). \tag{4}$$

The effect of the back-gate voltage V'_{BGS} on channel charges is explicitly modeled as a shift to the overall top-gate minimum conduction point $V_{TG,\min}$. C_{BG} is the back-gate capacitance per unit area. $V_{BG,\min 0}$ is the back-gate minimum conduction point voltage. V'_{BGS} is the intrinsic back-gate-to-source voltage. $V_{TG,\min 0}$ is the top-gate voltage at the minimum conduction point without the back-gate effect. ΔV accounts for the difference between $V_{TG,\min}$ and the effective threshold voltage for the electron charge $V_{t,e}$. In principle, ΔV can be experimentally estimated from the drain-current–gate-voltage characteristics of GFETs, but it is considered as a fitting parameter here. In this paper, V'_{TGS}, V'_{BGS}, and V'_{DS} will be referred to as the intrinsic voltages, i.e., the voltages that are applied to the intrinsic transistor region, which is given by the externally applied voltage corrected for potential drops across the access regions $V'_{TGS} = V_{TGS} - I_{DS}R_S$, $V'_{DS} = V_{DS} - I_{DS}(R_S + R_D)$, and $V'_{BGS} = V_{BGS} - I_{DS}R_S$. V_{TGS}, V_{BGS}, and V_{DS} will be referred to as the external voltages.

In (1), F_s is introduced as a saturation factor to empirically describe the transition of device operation from nonsaturation to saturation region when the drain-to-source voltage increases. Similar to the saturation function proposed for Si devices in [25, adopted from 35, 36], F_s takes the following form:

$$F_s = \frac{V'_{DS}/V_{\mathrm{DSAT}}}{\left(1 + \left(V'_{DS}/V_{\mathrm{DSAT}}\right)^{\beta}\right)^{1/\beta}} \tag{5}$$

where V'_{DS} is the intrinsic drain-to-source voltage, V_{DSAT} is the saturation voltage, and β is a fitting parameter relevant for the transition from low-field nonsaturation region to high-field saturation region. It is found in this paper that $\beta = 1.8$ gives a good fitting for both electron and hole conduction in graphene transistors. Typical values of β for Si MOSFETs were found between 1.8 for electrons and 1.6 for holes in [25]. It is clear from (1) that the saturation factor in (5) is defined to satisfy $I_{DS,I} = 0$ for $V'_{DS} = 0$ and $\lim_{V'_{DS}\to\infty} I_{DS,I} = Q_{\mathrm{VES},e} v_{\mathrm{VES},e} W = I_{\mathrm{DSAT}}$, which gives the saturation current.

The derivation of the saturation voltage V_{DSAT} for Si MOSFETs in [25], which is by relating the definition of low-field channel conductivity in the vicinity of $V_{DS} = 0$ to its physical dependence on sheet charges and mobility, is also valid for graphene transistors. Here, we quote the result as

$$V_{\mathrm{DSAT}} = \frac{v_{\mathrm{VES},e} L_G}{\mu} \tag{6}$$

where V_{DSAT}, as expressed in this form, is only dependent on the carrier transport properties $v_{\mathrm{VES},e}$, μ, and the device geometry L_G and is independent of the fitting parameter β. L_G is the gate length of the device. μ is the channel carrier effective mobility, which is, in general, a function of the top-gate, back-gate, and drain-to-source voltages [37], [38]. μ is assumed here to be a constant for simplicity.

Finally, graphene transistors always have a minimum current that cannot be fully pinched off by the gate. This is accounted

for by adding the minimum current $I_{\min}$ to the drain current $I_{DS,I}$, where

$$I_{\min} = \frac{V'_{DS}}{R_p} = \frac{V'_{DS}}{L_G/\mu \cdot W \cdot Q_{\min}} \tag{7}$$

where μ is the channel carrier effective mobility, and $Q_{\min}$ is the minimum charge in the channel, which cannot be modulated by the gate, thus giving rise to $I_{\min}$. $Q_{\min}$ is mainly due to disorder and thermal excitation, as discussed in [12], [39], and [40]. $1/R_p = (\mu \cdot W \cdot Q_{\min}/L_G)$ is the equivalent additional conductance contributed by the minimum charge $Q_{\min}$ to the channel. In this paper, $Q_{\min}$ is considered as a fitting parameter.

B. Device Operation in Region III

When GFETs are operating in region III, only hole charge is present in the channel, and the device operation is similar to that of p-channel Si MOSFETs. The formulation of the model in Section II-A for region I is also valid for the hole channel in region III. However, it is important to note that the drain side of the device acts as an "injection source" for holes when the device is operating in region III. The holes are injected from the drain side of the device and collected by the source of the device, which is opposite to that for electrons. Hence, the virtual source for hole injection is effectively at the drain side of the device, which is defined as the "virtual hole source (VHS)" in Fig. 1(b). Both the charge and injection velocity for the hole channel should be evaluated at this point. Applying (1) to the hole charge at the VHS, we have the following:

$$I_{DS,\mathrm{III}}/W = Q_{\mathrm{VHS},h} v_{\mathrm{VHS},h} F_s \tag{8}$$

where $v_{\mathrm{VHS},h}$ is the local hole carrier velocity at the VHS. $v_{\mathrm{VHS},h}$ is assumed to be equal to $v_{\mathrm{VES},e}$ in this paper. $Q_{\mathrm{VHS},h}$ is the hole charge at the VHS and is given as

$$Q_{\mathrm{VHS},h} = C_{TG} n \phi_t \ln\left(1 + \exp\frac{-V'_{TGD} + V_{t,h}}{n\phi_t}\right) \tag{9}$$

where $V_{t,h}$ is the effective threshold voltage for the gate-induced hole charge in the channel, which is given as

$$V_{t,h} = V_{TG,\min} - \Delta V. \tag{10}$$

The expressions for F_s in Section II-A are also valid for hole conduction. Similar to that in Section II-A, the minimum current $I_{\min}$, given by (7), needs to be added to $I_{DS,\mathrm{III}}$.

C. Device Operation in Region II

In this region of device operation, both electrons and holes are present in the channel. Assuming that $V_{DS} > 0$, the channel charge distribution can be schematically described as shown in Fig. 3. Point X in Fig. 3 marks the recombination point. As shown in Fig. 3, the part of the channel to the left of the recombination point has electron conduction and the part of the channel to the right of the recombination point has hole conduction. L_n is the length of the electron section of the channel, which is the distance from the VES to the recombination point. L_p is the length of the hole section of the channel, which is the distance from the recombination point to the VHS. V_n and V_p are the potential drops across the electron and hole sections of the channel, respectively. Hence, we have the following:

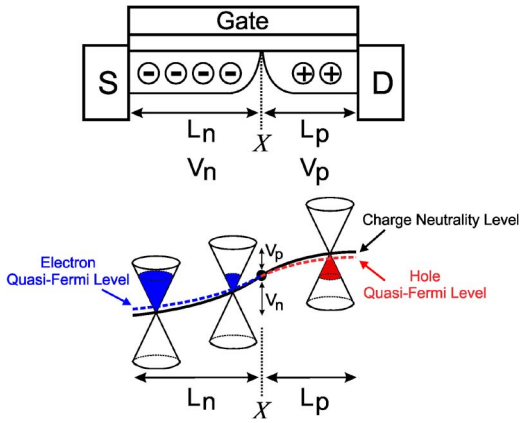

Fig. 3. Schematics of the cross section of a GFET operating in the ambipolar region (i.e., region II) and the charge distribution in the channel. The charge neutrality level is also shown, which connects the charge neutrality points for all positions along the channel. The dotted line shows the variation of quasi-Fermi levels along the channel (not drawn to scale). Point X is the recombination point. L_n and L_p are the length of the n-type and p-type sections of the channel, respectively. V_n and V_p are the potential drop across the respective n-type and p-type sections.

$$L_n + L_p = L_G \tag{11}$$

$$V_n + V_p = V'_{DS} \tag{12}$$

where I_n and I_p are the currents in the electron and hole sections of the channel, respectively. By current continuity, we have the following:

$$I_n = I_p \tag{13}$$

where

$$\frac{I_n}{W} = Q_{\mathrm{VES},e} v_{\mathrm{VES},e} F_{s,e} \tag{14}$$

$$\frac{I_p}{W} = Q_{\mathrm{VHS},h} v_{\mathrm{VHS},h} F_{s,h} \tag{15}$$

where $F_{s,e}$ and $F_{s,h}$ are the saturation factor for the electron and hole sections of the channel, respectively, and are given as

$$F_{s,e} = \frac{V_n/V_{\mathrm{DSAT},e}}{(1 + (V_n/V_{\mathrm{DSAT},e})^{\beta})^{1/\beta}}$$
$$V_{\mathrm{DSAT},e} = \frac{v_{\mathrm{VES},e} L_n}{\mu} \tag{16}$$

$$F_{s,h} = \frac{V_p/V_{\mathrm{DSAT},h}}{(1 + (V_p/V_{\mathrm{DSAT},h})^{\beta})^{1/\beta}}$$
$$V_{\mathrm{DSAT},h} = \frac{v_{\mathrm{VHS},h} L_p}{\mu}. \tag{17}$$

In addition, since electrons and holes recombine at the recombination point X, this point must be a point of minimum charge, i.e., a charge neutrality point where the channel carrier density is minimum. In other words, the recombination point X should be defined as the point along the channel where the channel potential is equal to the minimum conduction point of the GFET, i.e., the point where quasi-Fermi levels are equal

to the charge neutrality level in Fig. 3. Hence, we have the following:

$$V'_{TGX} \stackrel{\text{def}}{=} V_{TG,\min} \Rightarrow V'_{TGX} = V_{TG,\min} = \frac{V_{t,h}+V_{t,e}}{2}$$
$$\Rightarrow -(V'_{GD}+V_p)+V_{t,h} = (V'_{TGS}-V_n)-V_{t,e} \quad (18)$$

where V'_{TGX} is the voltage between the top gate and the recombination point. Hence, we can solve the set of six equations (11)–(15), and (18), for the six unknowns L_n, L_p, V_n, V_p, I_n, and I_p. It is clear from the expressions of the saturation factors $F_{s,e}$ and $F_{s,h}$ that this set of equations can only be solved numerically. In addition, since internal voltages are required to evaluate the charge and the current, iterations are needed to obtain self-consistent solutions of voltage and current, increasing the computational load in evaluating the model. However, the computation can be significantly reduced with little loss of accuracy by simply assuming a linear potential drop across the channel when the device is operating in the ambipolar region, which gives the following:

$$\frac{V_n}{L_n} = \frac{V_p}{L_p}. \quad (19)$$

By solving for the four unknowns L_n, L_p, V_n, and V_p from the four equations (11), (12), (18) and (19), we have the following:

$$L_n = \frac{L_G}{1+\frac{V'_{TGS}-(V_{t,e}+V_{t,h})/2}{(V_{t,e}+V_{t,h})/2-V'_{TGD}}}. \quad (20)$$

The current is evaluated by (14) or (15) depending on the relative saturation levels of the electron and hole sections, i.e., if $F_{s,h} > F_{s,e}$, we have $I_{DS,\mathrm{II}} = I_{DS,\mathrm{II},e} = Q_{\mathrm{VES},e} v_{\mathrm{VES},e} F_{s,e}$, and if $F_{s,h} < F_{s,e}$, we have $I_{DS,\mathrm{II}} = I_{DS,\mathrm{II},h} = Q_{\mathrm{VHS},h} v_{\mathrm{VHS},h} F_{s,h}$. Although the current continuity approach has a stronger physical basis, the linear approximation requires much less computation with very little loss of accuracy in calculating the current. Hence, we use the linear approximation method to evaluate L_n, L_p, V_n, and V_p for all results presented in Section IV. Finally, as in Sections II-A and II-B, the minimum current $I_{\min}$ needs to be added to $I_{DS,\mathrm{II}}$.

D. Determination of the Operation Region

A very important step in the model evaluation is to determine which operation region the device is in for a given gate and drain bias. This can be determined by the location of the recombination point X, i.e., by the value of L_n and L_p. Assuming that $V_{DS} > 0$, we have:

1) If $L_p < 0$, i.e., $L_n > L_G$, the hole section of the channel does not exist, and the entire channel has electron as the carrier. Hence, the GFET is operating in region I. The current is evaluated as in Section II-A.
2) If $L_p > L_G$, i.e., $L_n < 0$, the electron section of the channel does not exist, and the entire channel has hole as the carrier. Hence, the GFET is operating in region III. The current is evaluated as in Section II-B.
3) If $0 < L_p, L_n < L_G$, the channel has an electron section to the left of the recombination point and a hole section to the right of the recombination point (see Fig. 2). The device is in region II, and we use the derivations in Section II-C to evaluate the current.

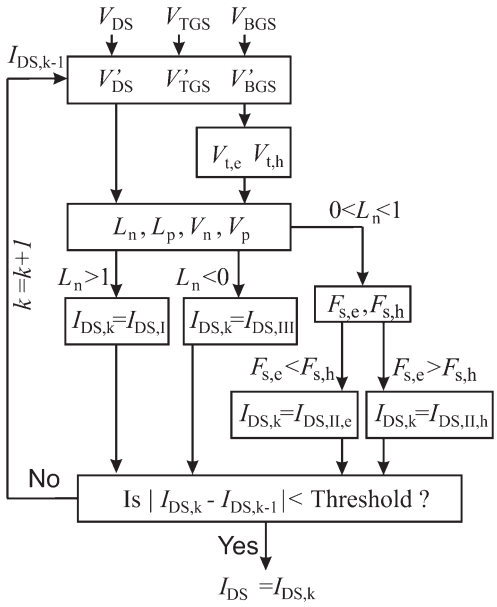

Fig. 4. Main steps in evaluating the model and the iteration loop needed to achieve self-consistent solutions of current and voltage. k is the iteration step index. Hence, $I_{DS,k}$ denotes the drain current evaluated in the kth step of the iteration process. The choice for the iteration threshold is arbitrary. Generally, a smaller threshold value gives more accurate results but requires more computation. An iteration threshold value of 10^{-6} mA/mm is used for the results presented in Section IV.

Note that, for $L_p = 0$ and $L_n = L_G$, we have $I_{DS,I} = I_{DS,\mathrm{II}}$, and for $L_p = L_G$ and $L_n = 0$, we have $I_{DS,\mathrm{II}} = I_{DS,\mathrm{III}}$, which ensures the continuity of the model between the three operation regions.

Fig. 4 summarizes the main steps in evaluating the model and the iteration loop needed to achieve self-consistent values of current and voltage since internal voltages are required to evaluate the charge and current.

III. Modulation of Access Resistance by the Back Gate

Several papers have reported that the parasitic series resistance of GFETs, which includes both the contact resistance and the resistance of the access region, is a function of the applied vertical electric field [39], [41], [42]. This dependence is due to the modulation of charge density in the contact and access regions. Since the access region and the region underneath the contacts, i.e., excluding the region under the top gate, are only modulated by the back gate, this series resistance is only a function of the back-gate voltage and is independent of the top-gate voltage. Assuming that the resistance of these regions is inversely proportional to the carrier density present, we have the following equation describing this dependence:

$$R_S = R_0 + \frac{r_1}{Q_{BGS,\,\mathrm{access}}} \quad (21)$$

$$R_D = R_0 + \frac{r_1}{Q_{BGD,\,\mathrm{access}}} \quad (22)$$

where R_0 and r_1 are fitting parameters. The source access region charge $Q_{BGS,\,\mathrm{access}}$ and the drain access region charge $Q_{BGD,\,\mathrm{access}}$ can be approximated as the sum of the charge induced by the back gate in the respective regions and the minimum charge $Q_{\min}$ as follows:

$$Q_{BGS,\,\mathrm{access}} = C^*_{BG} n_{BG} \phi_t \ln \times \left(1+\exp \frac{|V'_{BGS} - V_{BG,\,\min 0}|}{n_{BG}\phi_t}\right) + Q_{\min} \quad (23)$$

$$Q_{BGD,\,\mathrm{access}} = C^*_{BG} n_{BG} \phi_t \ln \times \left(1+\exp \frac{|V'_{BGD} - V_{BG,\,\min 0}|}{n_{BG}\phi_t}\right) + Q_{\min} \quad (24)$$

n_{BG} is the back-gate equivalence of n, which is analogous to the subthreshold coefficient in Si MOSFETs, and is considered as a fitting parameter. C^*_{BG} is the back-gate capacitance in the source and drain access regions without the screening effect from the top gate. C^*_{BG} is, in general, different from the back-gate capacitance C_{BG} in the channel region, which has the screening effect from the top gate since the graphene channel is not a perfect conductor. Since it would involve fairly complicated electrostatics to fully capture the screening effect of the top gate on C_{BG}, in this paper, we assume $C_{BG} = C^*_{BG}$ for simplicity. V'_{BGD}, which is given by $V'_{BGD} = V_{BGD} + I_{DS}R_D$, is the intrinsic back-gate-to-drain voltage, where V_{BGD} is the external back-gate-to-drain voltage.

IV. Results and Discussions

In this section, the results from the aforementioned model are compared with experimental data taken from a typical GFET fabricated in our laboratory. For the fabrication of the GFET, single-layer graphene films were grown by CVD on copper substrates [9]. Copper foils annealed at 1000 °C in H_2 (350 mtorr for 30 min) are exposed to CH_4 under a low-pressure condition (1.6 torr) to initiate graphene growth. After the growth, polymethyl methacrylate (PMMA) is coated on the graphene films, and the copper substrates are etched away in a copper etchant and diluted HCl. Films are then transferred onto polished Si wafers with 300-nm thermally grown SiO_2 on top. Monolayer graphene with uniformity greater than 95% is obtained (see Fig. 5). The ohmic contacts of the GFET are formed by depositing a 2.5-nm Ti/ 45-nm Pd/ 15-nm Au metal stack by electron beam (e-beam) evaporation. Device isolation is achieved by O_2 plasma etching. The gate dielectric of 15-nm Al_2O_3 is formed in two steps. A 3-nm Al layer is first deposited on the graphene surface by e-beam evaporation, which is then naturally oxidized in air. This first Al_2O_3 film serves as the initial nucleation layer to promote adhesion of the subsequent 12 nm of Al_2O_3 deposited by atomic layer deposition, using H_2O as the precursor and trimethyl aluminum as the Al source [39]. The top gate is formed with a 30-nm Ni/ 200-nm Au/ 50-nm Ni metal stack. Direct-current (dc) characterization of the devices was performed using an Agilent 4155C parameter analyzer. The devices were measured at room temperature under vacuum (1.1×10^{-4} torr) to reduce hysteresis. The device dimensions are shown in Table I(a), which also includes the parameters used in the compact device model.

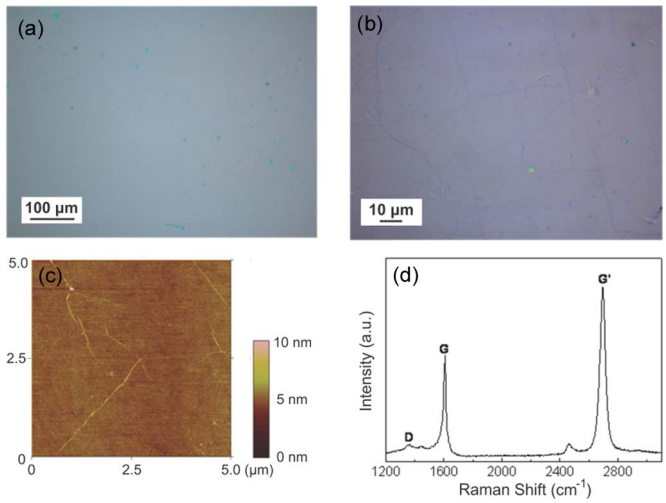

Fig. 5. (a) and (b) are the optical micrographs of the CVD-grown graphene. Using Cu as the catalyst, high-quality wafer-scale graphene sheets (greater than 95% area with mono-layer graphene) are obtained. (c) Atomic force microscopy image of the graphene obtained with a Veeco Dimension 3100 system showing excellent uniformity. (d) Raman spectrum confirms the presence of monolayer graphene.

A. I_{DS} versus V_{TGS} and V_{BGS}

Fig. 6(a) shows the top view of the 3-D plot generated from the model for I_{DS} as a function of both V_{TGS} and V_{BGS} for $V_{DS} = 1.1$ V. There are two distinct ridges of minimum conduction for the GFET due to modulation of the channel and series resistance, respectively. The deeper vertical ridge is due to the modulation of the channel region by both the top and back gates. The shallower horizontal ridge is due to the back-gate modulation of the source-and-drain series resistance, which includes both the contact resistance and access region resistance.

Fig. 6(b)–(d) compares the model with the measured data. In Fig. 6(b), V_{BGS} is kept constant at 0 V, and V_{TGS} is swept from -1 to 3 V. A family of curves is shown for V_{DS} increasing from 0.35 to 1.1 V in steps of 0.25 V. There is a clear dependence of the top-gate minimum conduction point on V_{DS}, which is due to both the increased potential drop across the source series resistance and the increased potential variation along the channel region as V_{DS} increases. In Fig. 6(d), V_{TGS} is kept constant at 1.41 V, and V_{BGS} is swept from -30 to 40 V. Again, a family of curves is shown for V_{DS} increasing from 0.35 to 1.1 V in steps of 0.25 V. In both the top-gate and back-gate sweeps, the ambipolar V-shaped characteristics for GFETs are observed. The model gives very good agreement with the experimental data in all bias combinations. In Fig. 6(c), V_{TGS} is kept constant at 0 V, and V_{BGS} is swept from -50 to 100 V. This is a sweep similar to the one in Fig. 6(d) only at a slightly different top-gate bias. The I_{DS}–V_{BGS} characteristic, however, shows a kink, which can be decomposed into two separate minimum conduction points that correspond to the back-gate modulation of the channel and of the series resistance, respectively.

In the devices analyzed in this section, the gate length is approximately equal to the distance between the source and drain electrodes (i.e., $L_{DS} \approx L_G$). The series resistance values are therefore dominated by the contact resistance values. The

TABLE I

GFET DEVICE PARAMETERS. (a) DEVICE PHYSICAL DIMENSIONS FOR THE GFET MODELED IN FIGS. 6 AND 7. THE PARAMETERS USED IN THE MODEL ARE GIVEN. (b) DEVICE PHYSICAL DIMENSIONS FROM [4] FOR THE GFET MODELED IN FIG. 8. THE PARAMETERS USED IN THE MODEL ARE GIVEN

DEVICE PHYSICAL DIMENSION	GFET
T_T (Al_2O_3)[nm]	15
T_B (SiO_2) [nm]	300
L_G [μm]	5
L_{DS} [μm]	5
W [μm]	25
C_{TG} [μF/cm^2]	0.39
C_{BG} [μF/cm^2]	0.0085
β	1.8
$V_{\mathrm{TG,\,min0}}$ [V]	1.24
$V_{\mathrm{BG,\,min0}}$ [V]	11
ΔV [V]	0
n	11.2
n_{BG}	49
$v_{VES,e}$, $v_{VHS,h}$ [10^7 cm/s]	1.2
μ [cm^2/V.s]	1500
WR_0 [kΩ.μm]	1.0
r_1 [10^{-4} V.s/cm^2]	3.6
Q_{min} [10^{-7} C/cm^2]	1.1

(a)

DEVICE PHYSICAL DIMENSION	GFET
T_T [nm]	10 nm poly-hydroxystyrene and 10 nm HfO_2
T_B (SiC) [nm]	Insulating Substrate
L_G [μm]	0.24
L_{DS} [μm]	Not Specified in Ref. [4]
W [μm]	30
C_{TG} [μF/cm^2]	0.195 (Given in Ref. [4])
C_{BG} [μF/cm^2]	Zero (No Back Gate)
β	1.8
$V_{\mathrm{TG,\,min0}}$ [V]	-3.1
$V_{\mathrm{BG,\,min0}}$ [V]	N.A.
ΔV [V]	1.8
n	14.6
n_{BG}	N.A.
$v_{VES,e}$, $v_{VHS,h}$ [10^7 cm/s]	2.5
μ [cm^2/V.s]	1600
WR_0 [kΩ.μm]	0.578
r_1 [10^{-4} V.s/cm^2]	N.A.
Q_{min} [10^{-7} C/cm^2]	0.92

(b)

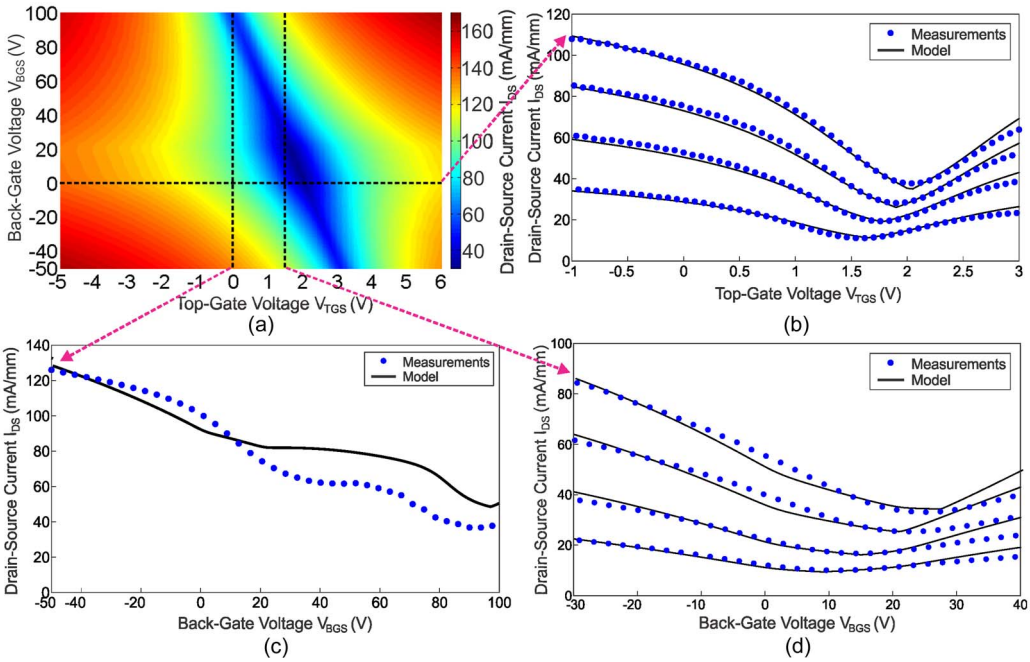

Fig. 6. (a) Top view of the 3-D plot of I_{DS} versus V_{TGS} and V_{BGS} at $V_{DS} = 1.1$ V. The two distinct ridges of minimum conduction in the GFET are clearly visible. (b), (c), and (d) are the cross sections in (a) at the corresponding dotted lines. The model results are shown as solid lines, and the experimental data are shown as dots. In (b), V_{BGS} is kept constant at 0 V, and V_{TGS} is swept from -1 to 3 V. A family of curves is shown for V_{DS} increasing from 0.35 to 1.1 V in step of 0.25 V. In (c), V_{TGS} is kept constant at 0 V, and V_{BGS} is swept from -50 to 100 V. The I_{DS}–V_{BGS} characteristics show a kink, which is due to two separate minimum conduction points from the back-gate modulation of the channel and the series resistance, respectively. (d) V_{TGS} is kept constant at 1.41 V, and V_{BGS} is swept from -30 to 40 V. A family of curves is shown for V_{DS} increasing from 0.35 to 1.1 V in a step of 0.25 V.

fitted contact resistance varies between 2.5 and 4.2 kΩ · μm, and it agrees well with the contact resistance measured by transmission line measurements [41], which gives values between 3 and 5 kΩ · μm, depending on back-gate bias. The fitted mobility is 1500 cm^2/V · s. This is very close to the mobility obtained from Hall measurements after the top-gate dielectric is deposited, which varies between 1400 and 1700 cm^2/V · s, depending on gate bias. The model extracts a virtual-source injection velocity of $v_{\mathrm{VES},\,e} = v_{\mathrm{VHS},\,h} = 1.2 \times 10^7$ cm/s in this long-channel device ($L_G = 5$ μm).

B. I_{DS} versus V_{TGS} and V_{DS}

Fig. 7(a) shows the 3-D plot generated from the model for I_{DS} as a function of both V_{TGS} and V_{DS}, for $V_{BGS} = 0$ V. In Fig. 7(b), curves A–D are the cuts in Fig. 7(a) at the

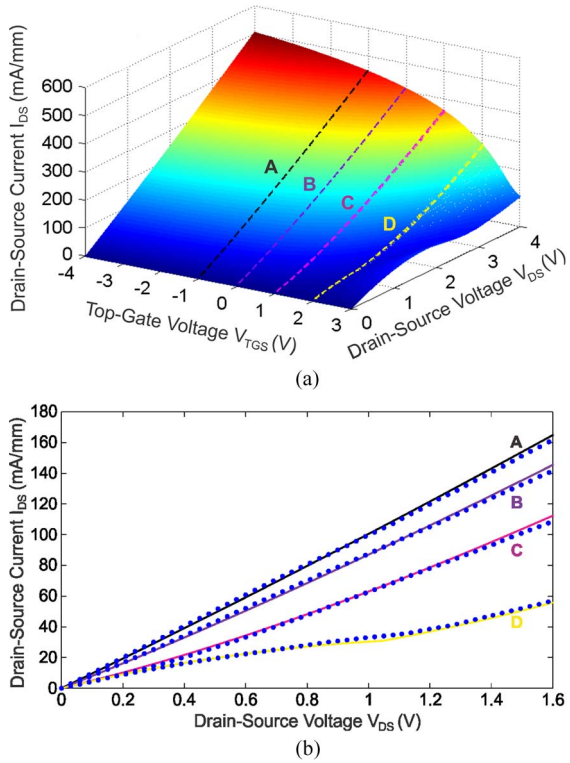

Fig. 7. (a) Three-dimensional plot of I_{DS} versus V_{TGS} and V_{DS} at $V_{BGS} = 0$ V. For curve D, the device starts with an n-type channel at low V_{DS} due to a high top-gate bias voltage. As V_{DS} increases, the device channel transits from an n-type to a p-type. The I_{DS}–V_{DS} cross section shows a characteristic kink due to the transitional ambipolar region (region II). The current continues to increase when the channel becomes entirely p-type. For curves A and B, the device starts with a p-type channel at low V_{DS} due to a low (or negative) top-gate bias, and the device never operates in the ambipolar region for all positive V_{DS}. (b) Curves A–D are the cross sections in (a) at the corresponding dotted lines. The model results are shown as solid lines, and the experimental data are shown as dots. $V_{BGS} = 0$ V in all plots.

corresponding dotted lines. The modeled results are shown as solid lines, and the experimental data are shown as dots. In all the plots, V_{BGS} is set to 0 V. Again, the model gives excellent agreement with the experimental data. In addition, the model can fully capture the kink in the I_{DS}–V_{DS} characteristics due to GFETs operating in the ambipolar region with an n-type channel section on the source side and a p-type channel section near the drain side. For example, in curve D in Fig. 7, with $V_{BGS} = 0$ V and $V_{TGS} = 2$ V, the channel is n-type everywhere in the channel (region I) at low V_{DS}, i.e., the L_n/L_G ratio is greater than 1. As V_{DS} increases to about $V_{DS} = 0.8$ V, the device operation starts to transit from region I to the ambipolar region (region II), and the recombination point appears near the drain, i.e., $0 < (L_n/L_G) < 1$. From approximately $V_{DS} = 0.8$ V to $V_{DS} = 1.2$ V, the device is in the ambipolar region (region II), and with increasing V_{DS}, the recombination point migrates from the drain side to the source side as the electron section of the channel shrinks and the hole section extends. In this operation region, the potential drop across the electron section V_n stays relatively constant, whereas the potential drop across the hole section V_p increases proportionally as V'_{DS} increases. Hence, in the early stage of region II when V_{DS} is still relatively low, the recombination point is closer to the drain side as the electron section still dominates the channel; the channel current stays relatively constant due to a relatively constant V_n, leading to the kink in the I_{DS}–V_{DS} characteristics. In the later stage of region II, when V_{DS} is much higher, the recombination point is closer to the source side as the hole section starts to dominate the channel. V_p increases proportionally with V'_{DS}, causing the current to start rising again with increasing V_{DS}. For $V_{DS} > 1.2$ V, the recombination point reaches the source side, and the channel becomes p-type everywhere (region III), i.e., $L_p/L_G > 1$ and $L_n/L_G < 0$. The current in the channel continues to rise in this operation region until it can saturate at a much higher drain bias.

The device, however, will not pass through the ambipolar region as V_{DS} increases from 0 V to more positive biases if the GFET starts with a p-type channel everywhere. In terms of the energy level diagram in Fig. 3, it means that, at $V_{DS} = 0$ V, the Fermi level is above the charge neutrality level (p-type) everywhere in the channel. As V_{DS} increases, which can cause the charge neutrality level on the drain side to rise but have a minimum effect on the source-side charge neutrality level, the quasi Fermi level (for holes) will always stay below the charge neutrality level everywhere in the channel, resulting in a p-type channel and no ambipolar operation in the GFET for all positive drain bias, i.e., for all $V_{DS} > 0$ V. For example, in curves A and B in Fig. 7(a), the top-gate biases are at $V_{TGS} = -1$ V and 0 V, respectively, making the channel p-type everywhere at a low drain bias. Fig. 7(a) shows that the device is never in the ambipolar region as V_{DS} increases, which is evidenced by the absence of the kink in the I_{DS}–V_{DS} characteristics.

C. Modeling Short-Channel Devices

Fig. 8 plots the modeled and experimental data for a short-channel (which is reported as $L_G = 240$ nm) top-gated GFET in [4]. To the best of our knowledge, this is the GFET whose gate length is among the shortest in the literature. The physical dimensions of the device reported in [4] and the parameters used in the model are listed in Table I(b). Since the GFET in [4] only has a top gate, it allows a few simplifications to the model. First, the back-gate effect is removed by setting $C_{BG} = 0$ in (4). In addition, (21) and (22) can be reduced to a single constant by setting $r_1 = 0$ since there is no back gate to modulate the series resistance. Fig. 8(a) compares the model results (solid line) for I_D–V_{DS} output characteristics with data from [4, Fig. 1C] (dashed line), showing very good agreement. Fig. 8(b) compares the model results (solid line) for I_D–V_{TGS} (transfer characteristics) with data from [4, Fig. 1B] (dashed line). Although there is a discrepancy between the model and those measured data, nevertheless, the model results agree very well with I_{DS}–V_{GS} data point mapped from [4, Fig. 1C] under the same bias conditions (blue dots). Hence, we attribute the discrepancy to the variation in the experimental data in [4, Fig. 1B and 1C], possibly due to measurements being taken under slightly different conditions. The model extracts a virtual-source velocity of $v_{\mathrm{VES},e} = v_{\mathrm{VHS},h} = 2.5 \times 10^7$ cm/s in this device. The injection velocity for this device is significantly higher than the injection velocity in the device in Section IV-A, probably due to its much shorter gate length (240 nm compared with 5 μm). The fitted source resistance is $WR_s = 578\ \Omega \cdot \mu$m,

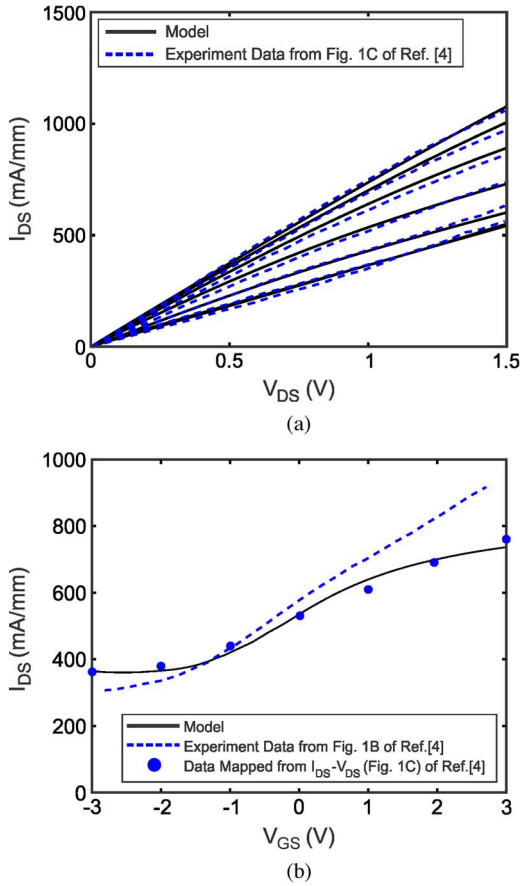

Fig. 8. (a) Model (solid line) versus experimental data (dotted line) for the I_{DS}–V_{DS} characteristics of a short-channel GFET with $L_G = 240$ nm. The experimental data is from , Fig. 1C[4]. The gate voltage increases from -3 to 3 V in a step of 1 V. (b) Model (solid line) versus experimental data (dotted line) for I_{DS}–V_{GS} characteristics for the same GFET. The experimental data (dashed line) is from , Fig. 1B[4]. The blue dots show the experimental data for I_{DS}–V_{GS} mapped directly from the I_{DS}–V_{DS} characteristics in , Fig. 1C[4]. The model has a discrepancy with the experimental data (dashed line) but shows good agreement with the mapped data (blue dots). The discrepancy is hence attributed to variations in measurement condition when data in [4] is obtained.

and the fitted mobility $\mu = 1600$ cm^2/V $\cdot$ s agrees very well with the measured values given in [4] and its supplementary information.

D. Virtual-Source Velocity

The model presented in Section II allows the extraction of a key parameter in FET operations for graphene transistors, which is the virtual-source carrier injection velocity. Fig. 9 compares the virtual-source carrier velocity extracted for GFETs using the model reported in this paper with that in modern Si MOSFETs and the state-of-the-art III–V heterostructure FETs (HFETs). For similar gate length, Fig. 9 shows that the source carrier velocity in graphene is much higher than the source carrier velocity in modern Si MOSFETs [26], [27] and also higher than the source carrier velocity in the state-of-the-art III–V HFETs [43], showing the great potential of graphene devices for high-frequency applications. In GFETs, the carrier velocity also increases as gate length is reduced, following the same trend as in Si MOSFETs and III–V HFETs, which is explained by increased carrier ballisticity with reduced channel length.

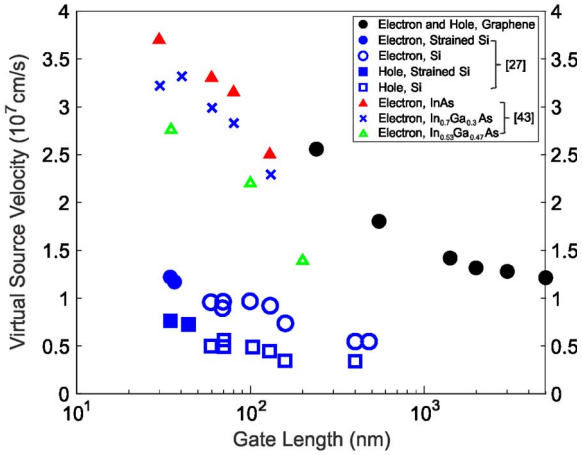

Fig. 9. Virtual-source injection velocity versus gate length for graphene transistors, modern Si MOSFETs, and state-of-the-art III–V HFETs. The virtual-source velocity in graphene devices is much higher than in Si MOSFETs and also higher than in the state-of-the-art III–V HFETs for similar gate lengths in the range of 200–250 nm, demonstrating the great potential of graphene for high-frequency applications. Source carrier injection velocity for all the GFETs are extracted using the model reported in this paper. The dc I–V characteristics for GFETs with gate lengths of 550 and 240 nm are taken from [4]. The Si MOSFETs source carrier injection velocity data are from [27]. The InGaAs and InAs source carrier injection velocity data are from [43].

V. Conclusion

This paper has presented a compact virtual-source model for the current–voltage characteristics of GFETs. The model provides a simple and intuitive understanding of the underlying carrier transport in GFETs and gives a quantitative explanation to the device behavior in the ambipolar region of GFET operation. The derived I–V characteristics account for the combined effects of the drain–source voltage V_{DS}, the top-gate voltage V_{TGS}, and the back-gate voltage V_{BGS} and is valid for both saturation and nonsaturation regions. With only a small set of mostly physical fitting parameters, the model agrees well with the experimental data for GFETs fabricated in our laboratory using CVD graphene and, also, the experimental data reported in the literature using epitaxial graphene. The simplicity and flexibility of the model promise attractive potential applications for circuit-level modeling of GFETs.

References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[2] A. H. Castro Neto, F. Guinea, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan.–Mar. 2009.

[3] T. Palacios, A. Hsu, and H. Wang, "Applications of graphene devices in RF communications," *IEEE Commun. Mag.*, vol. 48, no. 6, pp. 122–128, Jun. 2010.

[4] Y. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. H. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, Feb. 2010.

[5] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 547–549, May 2009.

[6] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, Sep. 2010.
[7] H. Wang, A. Hsu, K. K. Kim, J. Kong, and T. Palacios, "Gigahertz ambipolar frequency multiplier based on CVD graphene," in *IEDM Tech. Dig.*, 2010, pp. 23.6.1–23.6.4.
[8] A. Reina, A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large area few-layer graphene films on arbitrary substrates by chemical vapor deposition," *Nano Lett.*, vol. 9, no. 1, pp. 30–35, Jan. 2009.
[9] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.
[10] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," *Science*, vol. 312, no. 5777, pp. 1191–1196, May 2006.
[11] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197–200, Nov. 2005.
[12] S. Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma, "A self-consistent theory for graphene transport," in *Proc. Natl. Acad. Sci. U.S.A.*, Nov. 2007, vol. 104, no. 47, pp. 18 392–18 397.
[13] T. Ohta, A. Bostwick, T. Seyller, K. Horn, and E. Rotenberg, "Controlling the electronic structure of bilayer graphene," *Science*, vol. 313, no. 5789, pp. 951–954, Aug. 2006.
[14] V. Ryzhii, M. Ryzhii, and T. Otsuji, "Tunneling current–voltage characteristics of graphene field-effect transistor," *Appl. Phys. Exp.*, vol. 1, no. 1, p. 013001, Jan. 2008.
[15] V. Ryzhii, M. Ryzhii, A. Satou, T. Otsuji, and N. Kirova, "Device model for graphene bilayer field-effect transistor," *J. Appl. Phys.*, vol. 105, no. 10, pp. 104510-1–104510-9, May 2009.
[16] M. Cheli, G. Fiori, and G. Iannaccone, "A semianalytical model of bilayer graphene field effect transistor," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2979–2986, Dec. 2009.
[17] D. Jimenez, "A current–voltage model for Schottky-barrier graphene-based transistors," *Nanotechnology*, vol. 19, no. 34, p. 345204, Aug. 2008.
[18] M. Cheli, P. Michetti, and G. Iannaccone, "Model and performance evaluation of field-effect transistors based on epitaxial graphene on SiC," *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1936–1941, Aug. 2010.
[19] S. A. Thiele, J. A. Schaefer, and F. Schwierz, "Modeling of graphene metal–oxide–semiconductor field-effect transistors with gapless large-area graphene channels," *J. Appl. Phys.*, vol. 107, no. 9, pp. 094505-1–094505-8, May 2010.
[20] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nat. Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.
[21] K. L. Shepard, I. Meric, and P. Kim, "Characterization and modeling of graphene field-effect devices," in *Proc. IEEE/ACM ICCAD*, 2008, pp. 406–411.
[22] J. Brews, "A charge-sheet model of the MOSFET," *Solid State Electron.*, vol. 21, no. 2, pp. 345–355, Feb. 1978.
[23] A. B. Bhattacharyya, *Compact MOSFET Models for VLSI Design*. Piscataway, NJ: Wiley-IEEE Press, 2009.
[24] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ: Wiley, 2009, ch. 6.
[25] A. Khakifirooz, O. M. Nayfeh, and D. Antoniadis, "A simple semi-empirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009.
[26] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," in *IEDM Tech. Dig.*, 2006, pp. 667–670.
[27] D. A. Antoniadis, I. Åberg, C. N. Chleirigh, O. M. Nayfeh, A. Khakifirooz, and J. L. Hoyt, "Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovation," *IBM J. Res. Develop.*, vol. 50, no. 4/5, pp. 363–376, Jul. 2006.
[28] A. Khakifirooz and D. A. Antoniadis, "The future of high-performance CMOS: Trends and requirements," in *Proc. Eur. Solid State Device Res. Conf.*, 2008, pp. 30–37.
[29] M. S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.
[30] M. S. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 133–141, Jan. 2002.
[31] K. Natori, "Ballistic metal–oxide–semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879–4890, Oct. 1994.
[32] M. Lundstrom, "Device physics at the scaling limit: What matters?," in *IEDM Tech. Dig.*, 2003, pp. 33.1.1–33.1.4.
[33] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nat. Mater.*, vol. 6, no. 3, pp. 183–191, Mar. 2007.
[34] F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. I. Katsnelson, and K. S. Novoselov, "Detection of individual gas molecules adsorbed on graphene," *Nat. Mater.*, vol. 6, no. 9, pp. 652–655, Sep. 2007.
[35] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.
[36] J. A. Cooper and D. F. Nelson, "High-field drift velocity of electrons at the Si-SiO_2 interface as determined by a time-of-flight technique," *J. Appl. Phys.*, vol. 54, no. 3, pp. 1445–1456, Mar. 1983.
[37] R. S. Shishir and D. K. Ferry, "Intrinsic mobility in graphene," *J. Phys., Condens. Matter*, vol. 21, no. 23, p. 232204, Jun. 2009.
[38] M. C. Lemme, T. J. Echtermeyer, M. Baus, B. N. Szafranek, J. Bolten, M. Schmidt, T. Wahlbrink, and H. Kurz, "Mobility in graphene double gate field effect transistors," *Solid State Electron.*, vol. 52, no. 4, pp. 514–518, Apr. 2008.
[39] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, pp. 062107-1–062107-3, Feb. 2009.
[40] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby, "Observation of electron–hole puddles in graphene using a scanning single-electron transistor," *Nat. Phys.*, vol. 4, pp. 144–148, Feb. 2008.
[41] A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "Impact of Graphene Interface Quality on Contact Resistances and RF Device Performance," *IEEE Electron Device Lett.*, 2011, submitted for publication.
[42] B. Huard, N. Stander, J. A. Sulpizio, and D. Goldhaber-Gordon, "Evidence of the role of contacts on the observed electron–hole asymmetry in graphene," *Phys. Rev. B*, vol. 78, no. 12, pp. 121402-1–121402-4, Sep. 2008.
[43] D. H. Kim, J. A. del Alamo, D. A. Antoniadis, and B. Brar, "Extraction of virtual-source injection velocity in sub-100 nm III–V HFETs," in *IEDM Tech. Dig.*, 2009, pp. 35.4.1–35.4.4.

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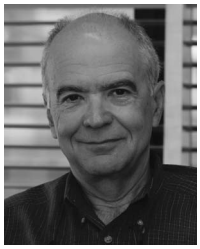

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