Engineering Density of Semiconductor-Dielectric Interface States to Modulate Threshold Voltage in OFETs

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***Abstract*—Threshold-voltage control is critical to the further development of pentacene organic field-effect transistors (OFETs). In this paper, we demonstrate that the threshold voltage can be tuned through chemical treatment of the gate dielectric layer. We show that oxygen plasma treatment of an organic polymer gate dielectric, parylene, introduces traps at the semiconductor-dielectric interface that strongly affect the OFET performance. Atomic force microscopy, optical microscopy using crossed-polarizers, and current–voltage and capacitance–voltage characterization were performed on treated and untreated devices. A model is presented to account for the effects of trap-introduced charges, both 1) fixed charges (2.0×10^{-6} C/cm^2) that shift the threshold voltage from -17 to $+116$ V and 2) mobile charges (1.1×10^{-6} C/cm^2) that increase the parasitic bulk conductivity. This technique offers a potential method of tuning threshold voltage at the process level.**

***Index Terms*—Organic compounds, thin-film transistors (TFTs).**

I. Introduction

ORGANIC field-effect transistors (OFETs) are a potential building block for many flexible, large-area applications such as printed circuits, electronic textiles, and robotic skin [1]–[5]. The performance of organic semiconductors, typically benchmarked by mobility, has been significantly improved by considerable research into materials and processes over the past decade [6]. Pentacene in particular has already been demonstrated with field effect mobilities comparable to that of amorphous silicon [7]. A next step in the development of OFETs is to address the issue of threshold voltage control, which ultimately determines circuit functionality and yield.

A range of threshold voltages, V_Ts, have been obtained for hole-conducting pentacene FETs. Positive V_Ts have been reported for FETs using solution-processed polymer dielectrics such as PVP [2] and sputtered materials such as SiO_2 [1], while negative V_Ts were reported for FETs using chemical vapor deposition (CVD) polymer dielectrics such as parylene [8] and thermally grown materials such as Si/SiO_2 [7], [9]. This suggests that the difference in threshold voltages is not necessarily intrinsic to the gate dielectric material but is related to the occurrence of process-dependent fixed charged states at the semiconductor-dielectric interface.

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For solution-processed dielectrics it is common to deposit a precursor and then perform a cross-linking step. Incomplete cross-linking results in unsatisfied chemical bonds or leftover reactive reagents that, if present at the semiconductor-dielectric interface, can generate interface states. In contrast, the CVD polymer parylene fully cross-links during deposition, obviating a separate cross-linking step. Hence, we expect OFETs fabricated with a parylene gate dielectric to have fewer interface states, providing a suitable platform to study the effects of process-induced traps.

In this paper, pentacene OFETs with a parylene gate dielectric were fabricated and for some devices the parylene dielectric was treated with an O_2 plasma prior to pentacene deposition. We hypothesize that the O_2 treatment breaks bonds at the parylene surface, introducing parylene-pentacene interface states. These states dope the semiconductor, introducing mobile charges that increase parasitic bulk conductivity in the device. Fixed charges that shift the threshold voltage are also introduced. This paper presents characterization results of O_2 plasma-treated OFETs and confirms that charges introduced by interface states influence threshold voltage and parasitic conductivity.

II. Experimental Technique

Pentacene OFETs were fabricated on glass substrates using parylene-C as the gate dielectric. A schematic cross section of the bottom-gate, top-contact device is shown in Fig. 1(a). Patterning of the aluminum gates, pentacene layer, and gold source/drain contacts was performed using shadow masks. A 275 ± 5 nm blanket layer of parylene was deposited by CVD over the patterned gates. Thermal evaporation of 10 nm of pentacene (at a rate of 0.02 nm/s) onto the parylene was followed by electron beam deposition of source/drain contacts. The top-contact devices have a channel length of 42 μm and a channel width of 1250 μm [Fig. 1(b)].

Two sets of devices were fabricated together using this process. The "control" device set was processed as described above, while for the second device set the parylene surface was treated with O_2 plasma in a Plasmod barrel plasma asher for 15 s prior to pentacene deposition. Metal–insulator–semiconductor (MIS) aluminum–parylene–pentacene–gold capacitors were also fabricated in the same evaporation, CVD, and O_2 treatment runs.

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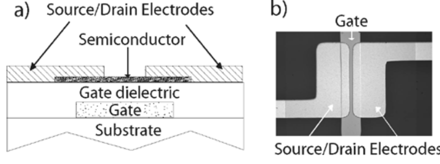

Fig. 1. OFET device structure. (a) Schematic cross-section of bottom-gate, top-contact OFET device. (b) Photograph of FET. The channel dimensions are 1250/42 μm W/L.

III. Threshold Voltage and Conductivity

Electrical characterization of the transistors was performed using an Agilent 4156C semiconductor parameter analyzer. Fig. 2(a) shows the I–V characteristic of a typical control transistor; Fig. 2(b) shows the same for an OFET with O_2 plasma-treated parylene. We observe a dramatic difference in the shape and magnitude of the drain current I_D. In the O_2-treated device I_D is more than an order of magnitude larger and does not saturate. This increase could be due to: 1) a change in pentacene morphology; 2) an enhancement of the field effect mobility; 3) a shift in threshold voltage; or 4) an increase in parasitic bulk conductance.

We explore these four possibilities: 1) Pentacene morphology has been linked to performance in OFETs; for example, field effect mobility has been shown to be sensitive to pentacene grain size [10]. For our samples, atomic force microscopy and optical microscopy with cross-polarizers show that both the control and O_2-treated devices have similar pentacene grain sizes of approximately 150 nm. This data suggests that pentacene morphology is not responsible for the observed differences. 2) The field effect mobility extracted from the OFET linear regions at $V_{\rm DS} = -10$ V, changed from 0.26 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ in the control device to 0.39 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ in the O_2-treated device. This increase is also not sufficient to account for the I_D increase. 3) and 4) Both the threshold voltage and parasitic bulk conductance, however, change significantly. In the context of the following model, these two factors can explain the I_D increase in the linear region of OFET operation.

OFETs are often modeled using conventional semiconductor device equations [11]. More refined models have been developed to include the contributions of trap states at the semiconductor/dielectric interface by modeling them as a gate voltage dependent mobility [12] or as localized bandgap states [13]. As in [14], we assume a constant mobility and model the interface states as acceptors. For an OFET in the linear region, the contribution of interface states is modeled as both fixed and mobile charges. The model assumes a parallel conduction mechanism consisting of: 1) a surface channel in which the carrier density in the surface accumulation layer is modulated by gate voltage and 2) a "bulk" layer away from the surface channel whose mobile carrier density is not modulated by the gate voltage. Fixed charges shift threshold voltage and mobile charges add parasitic bulk conductivity

$$-I_D = \frac{W}{L}\mu V_{\rm DS}\left[C_{\rm ins}\left(V_{\rm GS} - V_T - \frac{Q_{\rm fixed}}{C_{\rm ins}}\right)\right] + \frac{W}{L}\mu V_{\rm DS} Q_{\rm mobile} \quad (1)$$

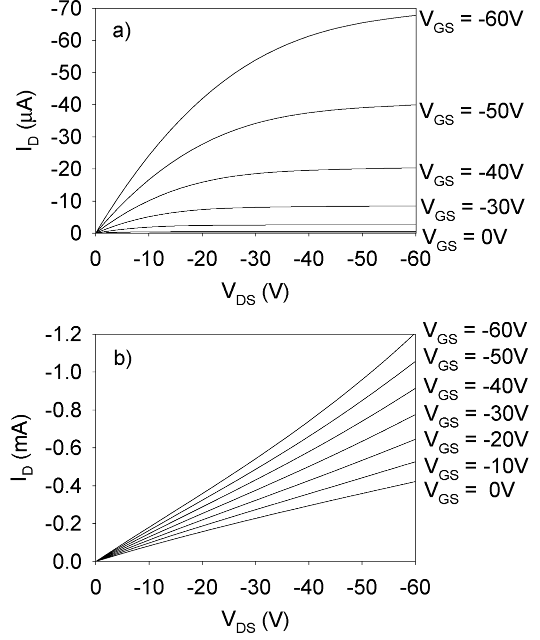

Fig. 2. I–V characteristics for (a) control and (b) O_2-treated pentacene FETs. The O_2-treated device shows much higher drain current and appears to have a significant parasitic bulk conductivity.

where W = width of the OFET, L = length, μ = field effect mobility, $C_{\rm ins}$ = dielectric insulator capacitance, $V_{\rm GS}$ = gate to source voltage, $V_{\rm DS}$ = rain to source voltage, V_T = threshold voltage, $Q_{\rm fixed}$ = fixed interface trap charge, and $Q_{\rm mobile}$ = parasitic mobile charge. This equation can then be rearranged to the form

$$-I_D = \frac{W}{L}\mu V_{\rm DS}\left[(V_{\rm GS} - V_T)\,C_{\rm ins} - Q_{\rm fixed} + Q_{\rm mobile}\right] \quad (2)$$

and $Q_{\rm fixed}$ and $Q_{\rm mobile}$ can be determined from the I–V characteristics.

Fig. 3(a) and (b) shows the extrapolated threshold values for the control and O_2 treated devices, respectively. Multiple runs of the control demonstrated that V_T variation across a substrate is generally within 1–2 V for control devices. After O_2 plasma treatment, the V_T variation across FETs on the same substrate increases, possibly due to nonuniformity in the O_2 plasma. The curves in Figs. 2(b) and 3(b) are representative of a group of six devices tested on the O_2-treated substrate, which all showed V_T shifts > 100 V.

As expected from the larger current modulation in the O_2-treated device I–V characteristics [Fig. 2(a), (b)], threshold voltage V_T has shifted positive. V_T changes from -17 V in the control to $+116$ V in the O_2-treated device. Lee and Song noted a similar, much smaller, positive shift in V_T (-1.8 ± 0.84 V to 0.34 ± 2.1 V) in pentacene FETs with an SiO_2 gate dielectric when the dielectric was treated for 5 min with O_2 plasma prior to pentacene deposition [9]. The threshold shift, $\Delta V_T = +133$ V, can be used to determine the relative difference in fixed charge between the control and O_2-treated devices

$$\Delta Q_{\rm fixed} = \Delta V_T * C_{\rm ins}. \quad (3)$$

Using the measured value $C_{\rm ins} = 1.5 \times 10^{-8}$ F/cm^2, $\Delta Q_{\rm fixed} = -2.0 \times 10^{-6}$ C/cm^2 $= -10^{13}$ charges/cm^2.

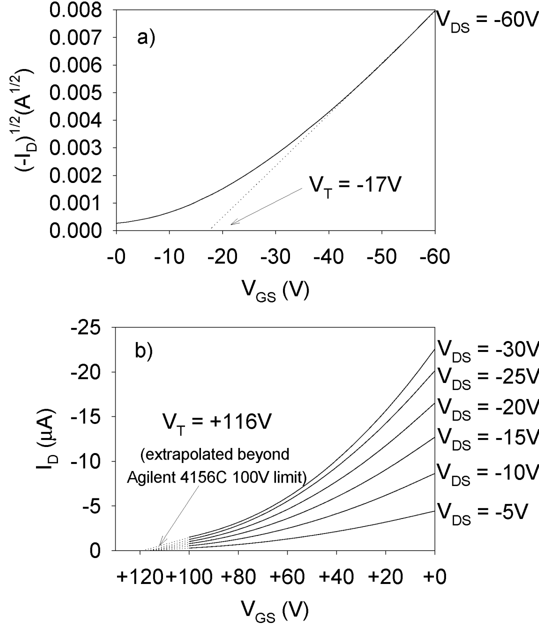

Fig. 3. Extrapolated threshold voltage for (a) control and (b) O_2-treated pentacene FETs. For the control device, V_T was extracted from saturation region measurements. Because the O_2-treated device does not saturate and I_D is high, V_T was extrapolated from V_{GS} close to V_T to minimize contact resistance effects. The threshold voltage has been shifted $+133$ V by the O_2 treatment.

TABLE I
CALCULATED VALUES FOR Q_{mobile} AT $0 \geq V_{\mathrm{DS}} \geq -10$ V. THESE VALUES WERE CALCULATED USING THE I-V CURVES AND (4). $\Delta Q_{\mathrm{fixed}}$ WAS 2.0×10^{-6} C/cm^2 $= 10^{13}$ electrons/cm^2

V_{GS} [V]	Q_{mobile} (control) [C/cm^2]	Q_{mobile} (O_2-treated) [C/cm^2]
-30V	5.8x10^{-8}	1.1x10^{-6}
-40V	9.2x10^{-8}	1.1x10^{-6}
-50V	1.1x10^{-7}	1.0x10^{-6}
-60V	1.1x10^{-7}	1.1x10^{-6}

The presence of a mobile charge in the bulk produces a parasitic conductivity that is not modulated by the gate bias. The resulting increase in I_D can be modeled as $\Delta I_D = W/L * \mu V_{\mathrm{DS}} * Q_{\mathrm{mobile}}$, as given in the model above. Although only the relative difference in Q_{fixed} can be calculated, values for Q_{mobile} can be determined for both the control and O_2-treated devices. Since the measured values of V_T include the contribution of Q_{fixed}, (2) can be written as

$$-I_D = \frac{W}{L}\mu V_{\mathrm{DS}}\left[\left(V_{GS} - V_{T_{\mathrm{measured}}}\right)C_{\mathrm{ins}} + Q_{\mathrm{mobile}}\right].$$

Differentiating this equation with respect to V_{DS} and solving for Q_{mobile}, we obtain

$$-Q_{\mathrm{mobile}} = \left(V_{\mathrm{GS}} - V_{T_{\mathrm{measured}}}\right)C_{\mathrm{ins}} + \frac{\frac{d(I_D)}{dV_{\mathrm{DS}}}}{\frac{\mu W}{L}}. \quad (4)$$

Table I gives the extracted values for Q_{mobile} in the linear region, where dI_D/dV_{DS} is calculated for $0 \geq V_{\mathrm{DS}} \geq -10$ V. The Q_{mobile} values for each device agree across several V_{GS} gate biases, indicating that the parasitic bulk conductivity is independent of gate voltage. Q_{mobile} in the O_2-treated device is an order of magnitude higher than in the control device and on the same order of magnitude as $\Delta Q_{\mathrm{fixed}}$.

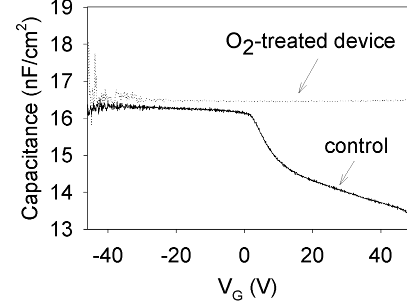

Fig. 4. Quasi-static C–V curve for control and O_2-treated MIS capacitors. The control device is in accumulation for negative gate voltages and enters depletion for positive V_{GS}. The O_2–treated device remains in accumulation throughout the measurement range and does not reach flatband.

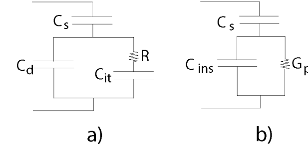

Fig. 5. (a) Gate capacitance model. C_d is the parylene dielectric capacitance; C_s is the semiconductor depletion capacitance; and C_{it} is the trap capacitance. Traps are modeled as a parasitic *RC* leg in parallel with the dielectric. (b) Equivalent capacitance model. Note that C_{ins} is the parallel combination of C_d and C_{it}.

IV. CAPACITANCE

The presence of traps introduced by O_2 plasma treatment is also observable in capacitance measurements of MIS test structures. Quasi-static C–V measurements were performed using an Agilent 4156C semiconductor parameter analyzer. An HP 4192A LF impedance analyzer was used to take C–V measurements at 1 kHz. Since O_2 plasma treatment etches parylene, the dielectric capacitance of the O_2-treated device is a few percent higher than that of the control. Parylene thickness in the O_2-treated device was reduced from 275 ± 5 nm to 255 ± 5 nm, as measured using a Dektak surface profiler.

As shown in the quasi-static C–V curve (Fig. 4), the control MIS capacitor goes through accumulation, flatband, and depletion over the -45 V $\leq V_{\mathrm{GS}} \leq +45$ V measurement range. In contrast, the O_2-treated MIS capacitor stays in accumulation throughout. This shift in flatband voltage is consistent with the V_T shift seen in the I–V characteristics and supports the existence of traps at the parylene/pentacene interface.

Traps can be modeled as capacitances with an *RC* time constant related to the trapping and release of carriers [15], [16]. We modeled the parylene-pentacene interface as a combination of three capacitances: the pentacene (semiconductor) depletion capacitance, C_s; capacitance of traps on the dielectric-semiconductor interface, C_{it}; and the parylene dielectric capacitance, C_d [Fig. 5(a)]. The total capacitance is then

$$C_{\mathrm{total}} = \left(\frac{1}{C_s} + \frac{1}{C_d + C_{\mathrm{it}}}\right)^{-1}. \quad (5)$$

In accumulation, the depletion capacitance C_s drops out and the model simplifies to the parallel combination of C_d and C_{it} [Fig. 5(b)].

High-frequency C–V measurements of the MIS structures showed that the gate capacitance in accumulation varies with

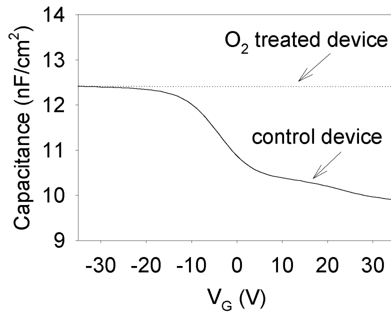

Fig. 6. High-frequency (1 kHz) C–V measurements of control and O_2-treated MIS capacitors as a function of gate bias.

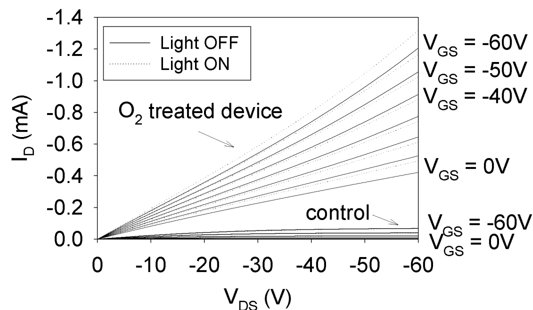

Fig. 7. I–V characteristics for control device and O_2-treated device in the dark and under 3400 $\mathrm{cd/m^2}$ incandescent white light illumination. The O_2–treated device exhibits enhanced photosensitivity.

frequency. Measurements of plain metal–parylene–metal capacitors confirmed that the parylene dielectric capacitance, $C_d = 9.4 \times 10^{-9}$ F/cm^2, is constant over the frequency range measured [17]. The frequency dependence of the accumulation gate capacitance can be attributed to 1) high resistivity and slow charge carrier movement in the pentacene material and/or 2) a distribution of carrier trapping/detrapping rates from localized states in the bulk and at the interface [18]. As frequency increases, slower traps can no longer follow the ac voltage [15], and Fig. 6 shows decreased capacitance at 1 kHz for both devices. Impedance spectroscopy is a possible method of determining the (possibly faster) carrier trapping and release time constants of the interface states introduced by O_2 plasma treatment, but this method is complicated by significant resistance in the pentacene material and was not performed.

V. Photosensitivity

In the accumulation-mode pentacene FETs, charges induced by the applied gate voltage first must fill trap states in the OFET channel before becoming available for conduction. The shift in V_T described previously is a measure of the increase in interface trap density in the O_2-treated FETs. Photo-induced detrapping of the carriers filling interface traps releases additional carriers that can contribute to conduction [19], [20], so that the traps introduced by the O_2 treatment are also observable in photocurrent measurements of OFETs.

We characterized the O_2-treated and control devices in the dark and under 3.4×10^3 cd/ m^2 white light luminance generated by an incandescent light bulb. At $V_{\mathrm{DS}} = V_{\mathrm{GS}} = -60$ V, I_D changed by $0.5\% \pm 0.02\%$ in the control device, while in the O_2-treated device I_D increased by $8.3 \pm 0.7\%$ (Fig. 7). This photosensitivity suggests that the traps introduced by the O_2 treatment can be probed optically.

VI. Conclusion

O_2 plasma treatment of the gate dielectric introduces trap states that can be observed with several techniques. In pentacene FETs traps induce both fixed charges that influence threshold voltage and mobile charges that increase parasitic bulk conductivity. A model was presented that attempts to explain the influence of the fixed and mobile charges on the transistor behavior.

O_2 plasma treatment shifts pentacene FETs from enhancement mode to depletion mode transistors, enabling the development of enhancement-depletion OFET logic circuits in an integrated process. Unlike enhancement-only or depletion-only FET logic, enhancement-depletion logic avoids the need for complex level-shifting schemes or additional biasing power supplies. By simply masking off appropriate sections of the substrate during treatment, transistors with different V_Ts can be produced on the same substrate.

Because the described O_2 treatment results in a very large shift in OFET characteristics within 15 s, a similar, but more controllable surface treatment technique (such as UV-ozone treatment [21]) is desirable. The specific O_2 plasma treatment presented in this paper is ultimately less important than the demonstration that surface modification of the gate dielectric at the process level, both intentional and unintentional, strongly affects OFET performance in a quantifiable way.

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