

# An Organic Active-Matrix Imager

Ivan Nausieda, *Student Member, IEEE*, Kyungbum Ryu, *Student Member, IEEE*, Ioannis Kymissis, *Member, IEEE*, Akintunde Ibitayo (Tayo) Akinwande, *Senior Member, IEEE*, Vladimir Bulović, and Charles G. Sodini, *Fellow, IEEE*

**Abstract**—In this paper, a proof of concept  $4 \times 4$  active-matrix imager fabricated at near room temperature ( $<95^\circ\text{C}$ ) is presented. Conventional photolithography and inkjet printing were used to pattern integrated organic FETs and photoconductors. The design and characterization of a pixel circuit is described. A simple first-order calibration technique is used to partially compensate for fixed pattern noise. Following the calibration, the imager is shown to correctly image a “T” pattern.

**Index Terms**—Integrated optoelectronics, organic compounds, thin-film transistors (TFTs).

## I. INTRODUCTION

ORGANIC semiconducting thin films could enable the development of large area, mechanically flexible integrated optoelectronics consisting of light emitters, photodetectors, electronic transistors, and sensors [1]–[4]. The low processing temperatures of organic semiconductors assure their compatibility with a broad range of substrates, including inexpensive plastic films such as polyethylene terephthalate (PET). Organic materials can simply be deposited through thermal evaporation of organic powders or inkjet printing of solutions of organic semiconducting inks, leaving the substrate near room temperature and enabling coarse ( $\sim 30\ \mu\text{m}$ ) patterning of deposited films.

Functionally useful organic devices need to achieve both adequate electrical performance, and the ability to be integrated into multicomponent circuits. Both requirements are paramount in the development of an active-matrix imager. To reduce crosstalk between transistors and increase device integration density, the organic FETs (OFETs) need isolated active regions. This requires them to be patterned by scalable fabrication techniques such as photolithography or inkjet printing, both of which are utilized in this paper.

Presently, the most often demonstrated OFETs use thermally evaporated thin films of the organic semiconductor pentacene. Charge transport in pentacene thin films favors hole over electron transport, with reported hole mobilities exceeding  $1\ \text{cm}^2/\text{V}\cdot\text{s}$  in saturation for shadow-mask-patterned OFETs [5]. In addition, photolithographic patterning of pentacene has

been demonstrated using standard photoresist and dry etching, achieving comparable hole mobilities to shadow-masked versions [6]. The compatibility with photolithography, together with near-room-temperature deposition conditions and charge carrier mobility comparable with amorphous silicon, identify pentacene as a candidate semiconductor for the development of large-area integrated organic circuits.

In this paper, we describe and demonstrate a process flow to produce integrated pentacene OFETs and organic photoconductors (OPDs) on a single substrate [7]. Both OFETs and lateral photoconductor electrodes are patterned by conventional photolithography. The photoconductor material is deposited by inkjet printing. Isolated individual fabricated devices are electrically and optically characterized.

By integrating an OFET switch with a photoconductor, we design and demonstrate an imaging pixel. An active-matrix imager consisting of 16 pixels is then fabricated and tested. The fixed pattern noise in the imager, likely dominated by variation in inkjetted photosensitive area, was partially overcome by a first-order calibration. Upon calibration, the imager correctly images a “T” pattern.

## II. PROCESS FLOW FOR INTEGRATED ORGANIC OPTOELECTRONICS

OFETs can be fabricated in a number of different device architectures. Top contact transistors have the source and drain deposited after the semiconductor, and exhibit lower contact resistance than bottom contact OFETs in which the semiconductor is deposited on top of prepatterned source/drain contacts [8]. To minimize semiconductor exposure to the solvents present in the photolithography process, we utilize a bottom gate, bottom contact geometry.

Pentacene OFETs are fabricated on glass substrates, following the near-room-temperature processing method described in previous work [6]. Devices are fabricated in a class 100 clean room, and are exposed to clean room air ambient after each processing step. The process flow is depicted in Fig. 1. A gate layer of 10-nm thick Cr (for adhesion to glass) and 60-nm thick Au is electron-beam evaporated, and patterned by photolithography and wet chemical etching. A 150-nm thick layer of parylene-C deposited by hot-filament CVD is used as the gate dielectric. Via holes are patterned in parylene by photolithography and reactive ion etching (RIE) in oxygen. A 60-nm thick layer of Au, which serves as the source/drain layer, is then deposited by e-beam evaporation. Photolithography and wet chemical etching are used to pattern the layer. A 20-nm thick pentacene film is blanket deposited by thermal evaporation at a rate of 0.6 nm/min. The pentacene is encapsulated by 200-nm thick film of parylene, allowing the pentacene/parylene stack to be

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I. Nausieda, K. Ryu, A. I. Akinwande, V. Bulović, and C. G. Sodini are with the Microsystems Technology Laboratory, Massachusetts Institute of Technology (MIT), Cambridge, MA 02139 USA (e-mail: nausieda@mit.edu; ryu@mit.edu; akinwand@mtl.mit.edu; bulovic@mit.edu; sodini@mtl.mit.edu).

I. Kymissis is with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA (e-mail: johnkym@ee.columbia.edu).

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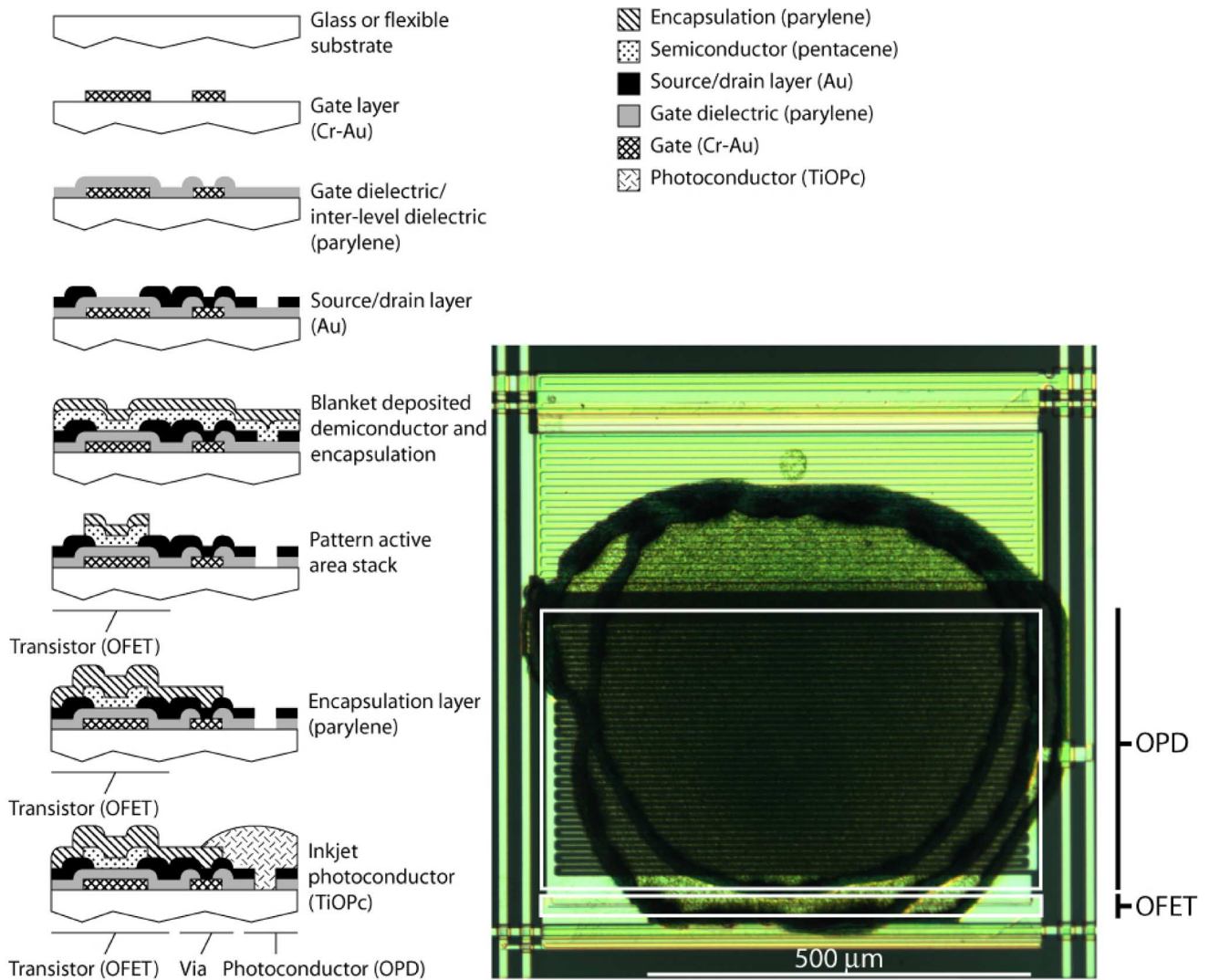


Fig. 1. Process flow for photolithographic fabrication of the active-matrix imager, with inkjet printed photoconductors (left). Micrograph of OPD, OFET, and interconnects (right).

photolithographically processed without exposing the pentacene to photoresist or developer. A subsequent RIE process defines islands of parylene and pentacene, isolating the active area of each OFET.

A third layer of parylene is then deposited over the entire substrate, passivating the exposed pentacene sidewalls, and further, electrically isolating each transistor. Photolithography and RIE were employed to pattern this parylene layer and expose the lateral photoconductor fingers defined in the source/drain Au layer. The last parylene layer also provides a “well” around the photoconductor fingers, to help confine the inkjetted photosensitive material of each pixel.

A colloidal dispersion of photosensitive titanyl phthalocyanine (TiOPc) in ethyl acetate and butyl acetate is inkjetted onto the interdigitated Au fingers. Approximately 100 drops with a nominal drop size of 220 pL were deposited on each pixel. A 1 s drying time between drops allows the solvent to evaporate before the subsequent drop. Fig. 1 shows a schematic cross section

of the completed substrate, and a top view micrograph of the OPD and OFET.

### III. DEVICE CHARACTERIZATION AND PERFORMANCE

Electrical characterization of the OFETs was performed using an Agilent 4156 C semiconductor parameter analyzer.

Fig. 2(a) shows the transfer curve for a transistor of width 1000  $\mu\text{m}$  and length 25  $\mu\text{m}$  taken immediately after active area patterning (Step 6 in Fig. 1). The transfer curve of Fig. 2(b) was measured after photoconductor processing, which involved photolithography, a solvent resist strip, and dry etching in oxygen plasma. It was observed that the threshold voltage shifts positively after this processing.

Quasi-static capacitance-voltage (QSCV) measurements and contact resistance measurements were obtained in order to extract the transistor mobility following the method of Ryu *et al.* [9]. Fig. 3 plots the hole mobilities versus applied gate bias for

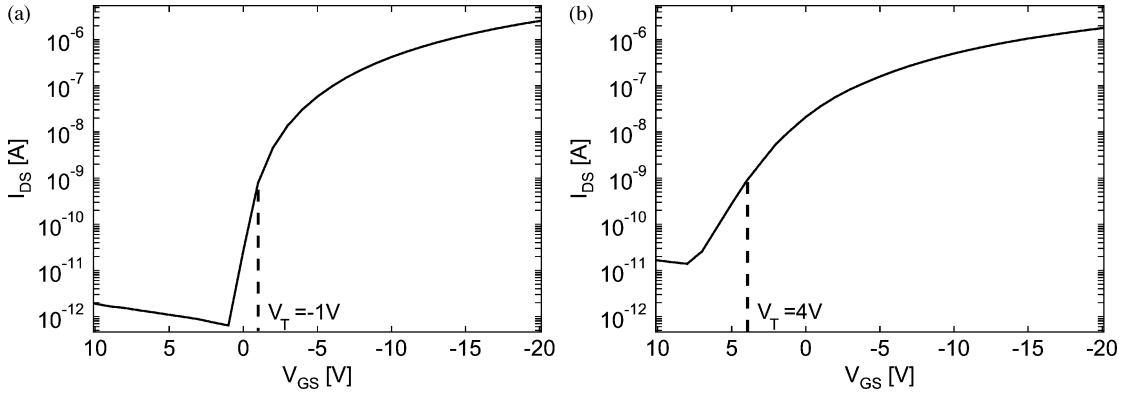


Fig. 2. (a) Transfer curve in the saturation regime for 1000  $\mu\text{m}/25 \mu\text{m}$  OFET at  $V_{\text{DS}} = -20 \text{ V}$  prior to photoconductor processing. (b) Transfer curve in the saturation regime for 1000  $\mu\text{m}/25 \mu\text{m}$  OFET at  $V_{\text{DS}} = -20 \text{ V}$  after photoconductor processing.

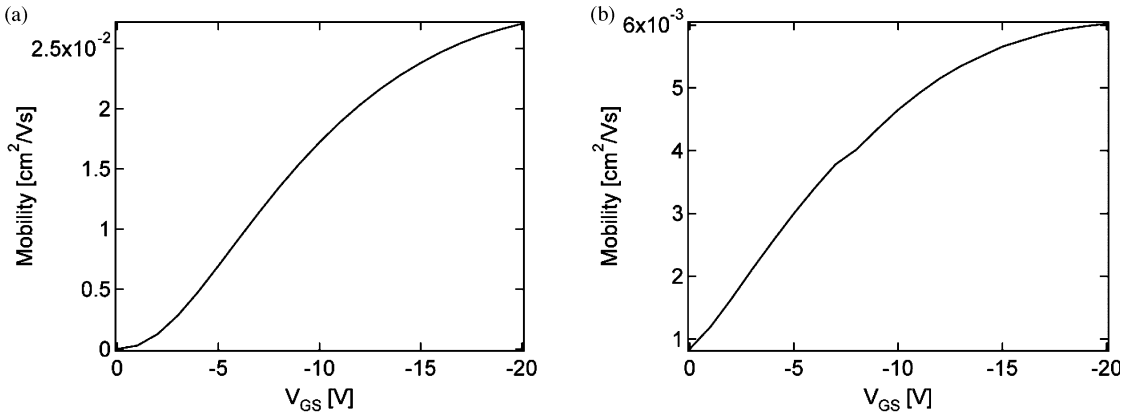


Fig. 3. (a) Hole mobility versus gate bias, measured prior to photoconductor processing. Same device as Fig. 2(a). (b) Hole mobility versus gate bias, after photoconductor processing. Same device as Fig. 2(b). Mobilities extracted accounting for source/drain contact resistance following method of Ryu *et al.* [9].

the devices characterized in Fig. 2. We note that mobility is about an order of magnitude lower for the transistor that has undergone photoconductor processing [10]. We suspect the degradation in mobility, positive threshold voltage shift, and shallower sub-threshold slope could be due to poor parylene encapsulation of the OFETs, leading to pentacene exposure to solvents from a wet photoresist strip performed before inkjetting of the photosensitive dispersion. Also, it has been reported that parylene exposure to oxygen plasma results in positive threshold shifts in pentacene OFETs [11].

The external quantum efficiency of the TiOPc photoconductor is plotted in Fig. 4 as a function of illumination light wavelength. For this measurement, the photoconductor is illuminated by a Xe lamp filtered by a monochromator, chopped at 95 Hz and referenced to a Newport 818 UV calibrated photodetector. A SR 830 lock-in amplifier sensed the current through the photoconductor as the illumination wavelength is varied.

#### IV. PIXEL DESIGN

An OFET connected in series with an OPD acts as a switch, creating an active-matrix pixel. In this circuit, the OFET behaves

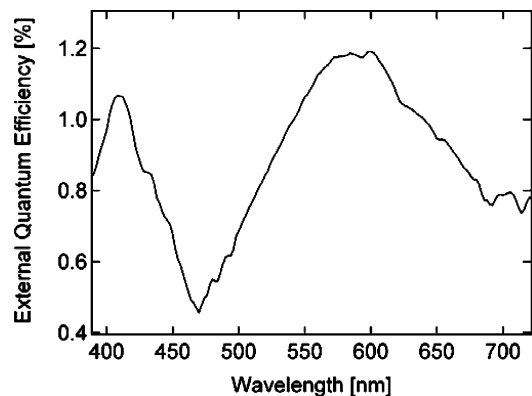


Fig. 4. External quantum efficiency of the TiOPc lateral photoconductor.

as a low-resistance switch when turned ON, and the pixel current is dictated by the photoconductor, which responds to the incident light intensity. When the OFET is turned OFF, the total pixel resistance is dominated by the OFET, and the pixel current does not change regardless of the illumination intensity. This behavior and the corresponding bias conditions are shown in Fig. 5.

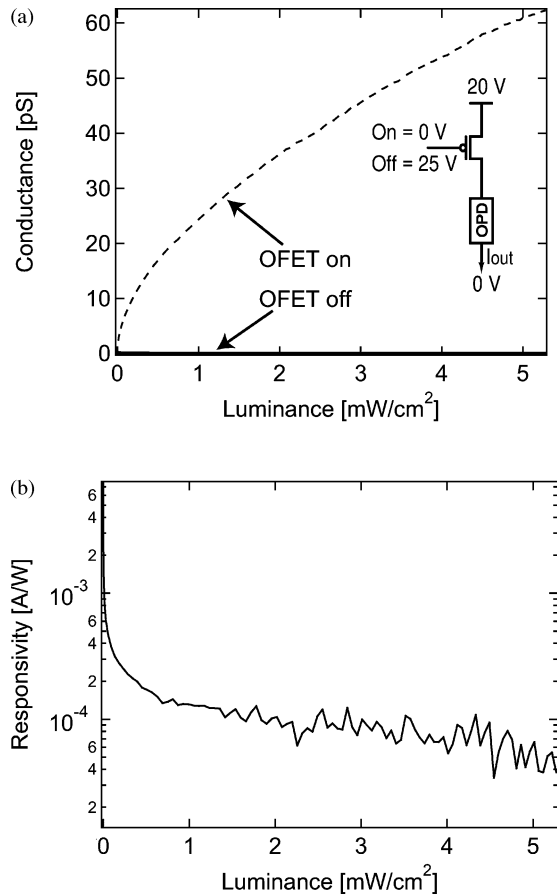


Fig. 5. (a) Conductance of an active-matrix pixel versus incident luminance of the 530 nm wavelength green light source. (Inset) Pixel circuit and bias conditions for ON and OFF states. (b) Responsivity of active-matrix pixel versus luminance.

The OFET and OPD must be properly sized to achieve conductances enabling the desired circuit behavior. The conductance of an OFET in ON state should be, at least, two orders of magnitude greater than that of the photoconductor, so that the photoconductor conductance can control the pixel current. This ratio of conductances also assures that the circuit will behave as designed even if the mobility of the OFET degrades over time. We use an OFET with a channel width of  $1000 \mu\text{m}$  and length of  $5 \mu\text{m}$ . A gate-to-source voltage of  $-20 \text{ V}$  exhibits an ON conductance of  $20 \text{ nS}$ , and a gate-to-source voltage of  $5 \text{ V}$  exhibits an OFF conductance of  $69 \text{ fS}$ .

The TiOPc photoconductor is highly resistive, and requires an effective width of  $25 \text{ mm}$  and length of  $5 \mu\text{m}$  to achieve a conductance appropriate to that of the OFET. An interdigitated structure is used to achieve the large effective width while maintaining an appropriate aspect ratio. A micrograph of the finished pixel is shown in Fig. 1.

The pixel was characterized by uniformly illuminating it with a 530 nm wavelength light generated by a Lumileds LED. The pixel current was measured by an Agilent 4156 C while the LED brightness was increased. The LED luminance was measured using a calibrated 818 UV Newport photodiode.

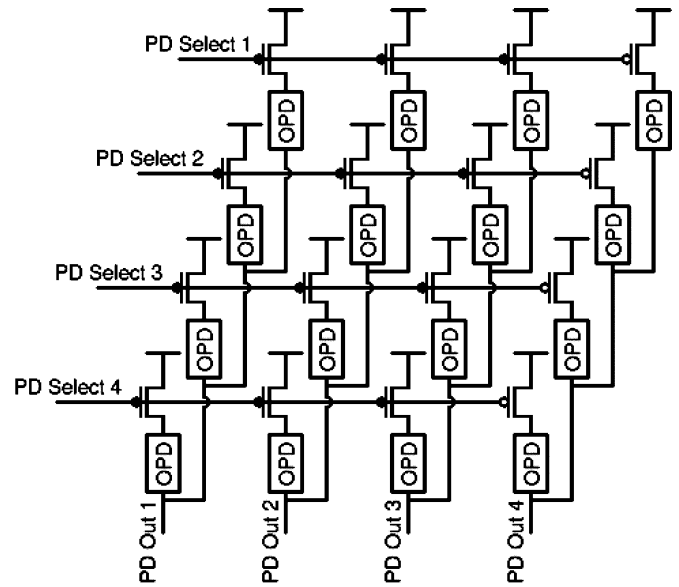


Fig. 6. Circuit schematic of the  $4 \times 4$  active-matrix imager.

The pixel conductance and responsivity versus LED luminance are plotted in Fig. 5(a) and (b), respectively. At a luminance of  $5 \text{ mW/cm}^2$ , the pixel on/off conductance ratio is 880 and responsivity is  $6 \times 10^{-5} \text{ A/W}$ . We note that this number was obtained by using the entire pixel area, even though photosensitive material covers only a portion of it. Consequently, the stated responsivity is an underestimate.

## V. ACTIVE-MATRIX IMAGER

The circuit schematic for the  $4 \times 4$  imager is shown in Fig. 6. The fabricated imager occupies an area of  $10.24 \text{ mm}^2$  and uses a  $25 \text{ V}$  power supply. A micrograph of the finished imager under test is also pictured in Fig. 7(a).

It is apparent from Fig. 7(a) that the inkjetted area varies from pixel to pixel. The variation in photosensitive area contributes to fixed pattern noise. This can be seen in Fig. 7(b), which plots the response of each pixel to a uniform luminance. The pixel currents were recorded for subsequent calibration, which reduces the effect of fixed pattern noise.

To perform the first-order calibration, the conductances recorded from the patterned test are divided by the conductances under uniform illumination. This ratio is multiplied by the luminance of the uniform illumination. This method approximates the conductance versus luminance behavior of the pixel as linear.

A clear transparency mask with a semitransparent print in the shape of a "T" was placed in the field of the LED, producing a patterned shadow on the imager in the shape of a "T." The system under test is shown in Fig. 7(a). Column 2 is completely covered by the shadow and Column 3 only partially.

Fig. 7(c) plots the brightness sensed by the imager after the first-order calibration. The imager correctly produces a higher brightness for Column 3 than Column 2, since the first is only partially shadowed.

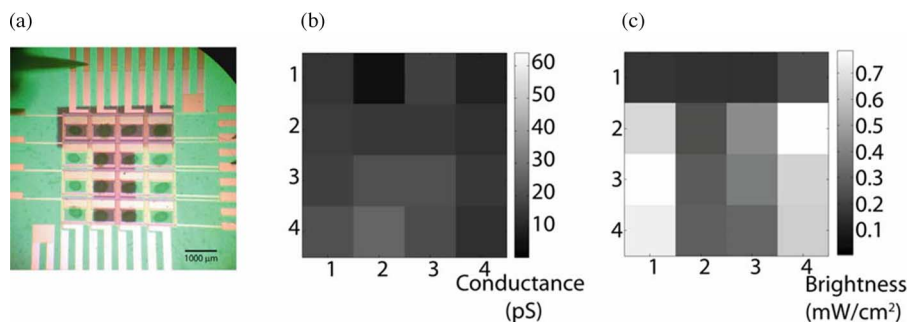


Fig. 7. (a) The  $4 \times 4$  active-matrix imager under test. (b) Pixel conductances recorded under uniform illumination (without T). (c) Sensed brightness after first-order calibration (with T).

## VI. CONCLUSION

A low-temperature process flow for integrated OFETs and OPDs was introduced. Photolithographically processed OFETs were electrically characterized and exhibited a hole mobility of  $6 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$  at a  $V_{\text{GS}}$  of  $-20 \text{ V}$ . The OPD responsivity was measured to be  $6 \times 10^{-5} \text{ A/W}$  at a luminance of  $5 \text{ mW/cm}^2$ .

A proof of concept  $4 \times 4$  active-matrix imager was fabricated and tested. Variation in inkjetted photosensitive area contributed to fixed pattern noise. A first-order calibration was performed and enabled the imager to correctly image a “T” pattern.

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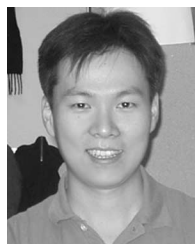
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**Ivan Nausieda** (S’00) received the first B.S. degree in electrical and computer engineering and the second B.S. degree in materials science and engineering from Carnegie Mellon University, Pittsburgh, PA, in 2004, and the M.S. degree in applied physics from Harvard University, Cambridge, MA, in 2005. He is currently working toward the Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge.

His current research interests include organic thin-film transistors for integrated circuits.



**Kyungbum Ryu** (S’00) received the B.S. degree in electrical engineering from the Cooper Union for the Advancement of Science and Art, New York, NY, in 2003, and the M.S. degree in electrical engineering and computer science in 2005 from the Massachusetts Institute of Technology, Cambridge, where he is currently working toward the Ph.D. degree.

His current research interests include the processing and characterization of organic and metal-oxide thin-film transistors for circuit applications.



**Ioannis Kymissis** (S’97–M’03) received the S.B., M.Eng., and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1998, 1999, and 2003, respectively, all in electrical engineering and computer science.

He was a Postdoctoral Associate in the MIT Laboratory for Organic Optics and Electronics (LOOE), where he was initially engaged in research on the new processing strategies for highly integrated organic systems, and later, at a small MIT-based startup, QDVision. He is currently an Assistant Professor at

the Department of Electrical Engineering, Columbia University, New York, NY. His current research interests include the application of organic FETs to large area-compatible sensing and actuation systems.

Prof. Kymissis was the recipient of the IEEE Paul Rappaport Award in 2002 for his contributions to organic FET technology, the Shoulders–Grey–Spindt Medal at the 2002 IVMC for contributions to vacuum microelectronics, and the National Science Foundation (NSF) CAREER Award in 2006. He was on the Program Committees of the Materials Research Society (MRS), the International Society for Optical Engineers (SPIE), and several regional conferences. He is also the Chair of the IEEE Electron Devices Society/Solid-State Circuits Society (EDS/SSCS) New York Section Chapter.



**Akintunde Ibitayo (Tayo) Akinwande** (S'81–M'86–SM'04) received the B.Sc. in electrical and electronic engineering from the University of Ife, Nigeria, in 1978, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1981 and 1986, respectively.

During 1986, he was with Honeywell Inc., where he was initially engaged in research on GaAs complementary FET technology for very high speed-signal processing, and later, on pressure sensors, accelerometers, thin-film field emission, and display devices.

Since 1995, he has been with the Massachusetts Institute of Technology, Cambridge, where he is currently a Professor in the Department of Electrical Engineering and Computer Science. His current research interests include devices for smart displays, large area electronics, field emission, field ionization, gas analysis, electrospray, and electric propulsion. He is the holder of several patents in microelectromechanical systems (MEMS) and display technologies.

Prof. Akinwande was the recipient of the 1996 National Science Foundation (NSF) CAREER Award. He was on Technical Program Committees for various conferences, including the Device Research Conference, the International Electron Devices Meeting, the International Solid-State Circuits Conference, the International Display Research Conference, and the International Vacuum Microelectronics Conference. He is a member of the Materials Research Society, the Society of Information Display, and the Electrochemical Society.



**Charles G. Sodini** (M'82–SM'90–F'95) received the B.S.E.E. degree from Purdue University, West Lafayette, IN, in 1974, and the M.S.E.E. and Ph.D. degrees from the University of California, Berkeley, in 1981 and 1982, respectively, all in electrical engineering.

From 1974 to 1982, he was a Technical Staff at Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in research on the design of MOS memory. Since 1983, he has been with the Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, where he is currently the LeBel Professor of Electrical Engineering. He was a cofounder of SMaL Camera Technologies. His current research interests include mixed signal integrated circuit and system design. He is the coauthor of an undergraduate textbook *Microelectronics: An Integrated Approach* (Prentice Hall, 1997).

Dr. Sodini was on several IEEE Conference Committees, including the International Electron Devices Meeting, where he was the 1989 General Chairman and the IEEE Electron Devices Society Administrative Committee. During 2002–2004, he was the President of the IEEE Solid-State Circuits Society. He is currently the Chair of the Executive Committee for the VLSI Symposium.



**Vladimir Bulović** received the M.S. degree in electrical engineering from Columbia University, New York, NY, in 1993, and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, in 1998.

He was a Senior Scientist and Project Head of Strategic Technology Development at Universal Display Corporation (UDC), where was engaged in research on applications of organic materials to light emitting and photosensitive devices. He is the KDD Career Development Associate Professor of Electrical Engineering at the Massachusetts Institute of Technology, Cambridge.

His current research interests include studies of physical properties of organic/inorganic nanocrystal composite thin films and structures, and development of novel optoelectronic organic and hybrid nanoscale devices. He is the author or coauthor of more than 60 papers published in international journals. He is the holder of more than 40 U.S. patents in areas of organic and nanostructured LEDs, lasers, photovoltaics, photodetectors, and programmable memories, most of which have been licensed and utilized by both start-up and multinational companies.

Prof. Bulovic is the recipient of the U.S. Presidential Early Career Award for Scientist and Engineers, the National Science Foundation Career Award, and figured in the Technology Review TR100 List.