A Fabrication Method for Integrated Filter Elements with Inductance Cancellation

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***Abstract*— This paper outlines a fabrication method for integrated filter elements. An integrated filter element is a three- (or more) terminal device comprising a capacitor and coupled air-core magnetic windings, in which the magnetic windings cancel the effects of capacitor parasitic inductance. This provides greatly enhanced filtration performance over a capacitor alone. Methods for designing and forming cancellation windings are described, along with means for repeatable interconnection with the capacitor and encapsulation of the filter element. The high performance and repeatability of filter elements fabricated with the proposed method are demonstrated with several examples**

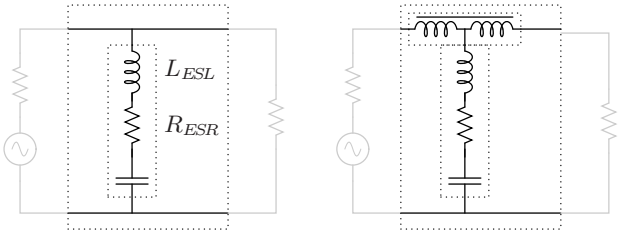

Fig. 1. Single capacitor low-pass filter models with first-order capacitor parasitics; (a) Standard filter, (b) Filter with inductance cancellation.

I. Introduction

Filters designed to suppress electromagnetic interference (EMI) often play a critical role in meeting requirements for device compatibility. Component parasitics, such as the equivalent series inductance of capacitors and the equivalent parallel capacitance of inductors, often limit the size and performance of these filters [1]–[14]. Recent work has addressed methods to compensate for these parasitics, thereby increasing filter performance [5]–[15]. The use of coupled magnetic windings has been shown to be effective in compensating for the effects of capacitor parasitic inductance, increasing its attenuation performance and reducing the filter volume and cost [5]–[7], [14].

Consider the low-pass filter in Fig. 1(a), shown with the first-order capacitor parasitics of equivalent series resistance (ESR) and equivalent series inductance (ESL). At high frequencies the equivalent series inductance of the capacitor causes an increase in the capacitor's impedance, greatly reducing the filtration performance in this region, where it is often most desired. The solid trace in Fig. 2 shows the effect of this increased impedance on the attenuation performance of the simple filter. To compensate for the parasitic effects of the capacitor, additional capacitors providing better high frequency performance are normally connected in parallel with the main capacitor, increasing the circuit size and cost.

An alternative to adding additional capacitors is to try to reduce the effects of the device parasitics. An example of the performance that can be achieved with reduced parasitic inductance can be seen in the dashed second trace of Fig. 2. To achieve this performance, a coupled inductor structure can be inserted into the circuit to induce a voltage that counteracts the voltage due to capacitor equivalent series inductance [5]–[7], [14], as illustrated in Fig. 1(b). The designed cancellation effect can be achieved using the mutual coupling of magnetic flux between coupled inductor windings, illustrated in

Fig. 3. Fig. 4 shows an equivalent two-port T-model. When combining the models of the coupled inductor with that of the capacitor, the model in Fig. 5 results. To completely suppress the effects of the capacitor ESL, the residual shunt inductance, L'_{12}, is designed to be zero. An advantage of this technique is that the coupled magnetic windings used to achieve cancellation can be very small, with inductances on the order of the parasitic inductance, typically 5-25 nH, being canceled.

As developed in previous work, a filter with induc-

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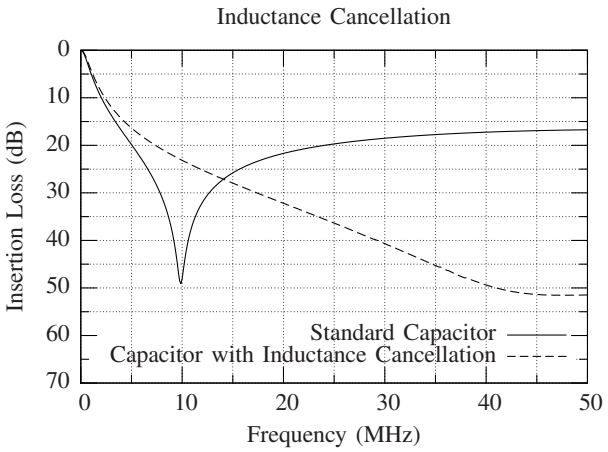


Fig. 2. Measured results from the low-pass filters in Fig. 1 showing the difference in performance between a circuit with a 4700 pF ceramic capacitor and one with the addition of inductance cancellation. The insertion-loss is measured with 50Ω source and load impedances. The capacitor has an approximate ESL of 50 nH.

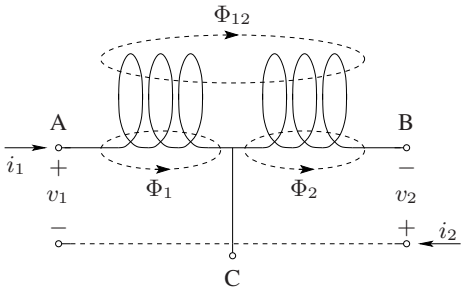


Fig. 3. Flux linkage in "center-tapped" magnetically coupled windings.

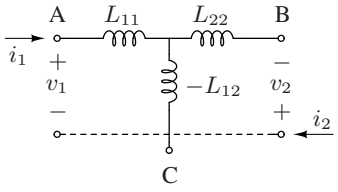


Fig. 4. Equivalent two-port 'T' Model of the coupled-winding structure shown in Fig. 3.

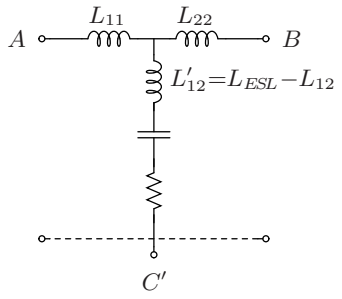


Fig. 5. Equivalent inductive 'T' model of an integrated filter element, additionally showing shunt capacitance and resistance. Inductance cancellation is achieved by matching the winding mutual inductance L_{12} to the capacitor parasitic inductance L_{ESL}.

tance cancellation can be implemented with conventional capacitors and an air-core inductance cancellation winding printed on a circuit board [5]–[7], or discretely constructed [14]. These approaches are both highly effective, but each necessitates significant effort on the part of the circuit designer to design and implement the inductance cancellation winding in the context of a particular application. Another approach, considered here, is the development of an integrated filter element that can be provided to the circuit designer as a basic building block. An integrated filter element is one or more inductance cancellation windings packaged together with a capacitor to form a three- (or more) terminal device that provides greatly enhanced filter attenuation. Integrating the capacitor and windings creates a self-contained filter element that can easily be used in a wide range of circuit designs.

Repeatability is a primary concern when implementing inductance cancellation. Deviation in the final shunt inductance can have a significant impact on the realized performance [6]. Printed circuit board windings provide a consistent, repeatable structure which results in a very small variance, but can require a significant board footprint and must be re-designed for each circuit. For an integrated filter element, the design must only be completed once, but requires a repeatable fabrication method to ensure consistent performance for each device.

This paper develops a method to fabricate a cancellation winding and integrate it with a capacitor within the capacitor casing. The method is validated experimentally and the performance and repeatability of the method are evaluated. Section II outlines the general design and fabrication process for an integrated filter element. Section III details the implementation of the developed process for two EMI filter capacitors. Section IV presents the performance characterization and design validation for the two constructed integrated filter elements. Section V concludes the paper.

II. Integrated Filter Element Design Process

An integrated filter element contains two primary components packaged together: the capacitive element and the magnetically coupled winding. Constraints are placed on the physical size and orientation of the magnetic winding to achieve the desired filtering performance, minimize sensitivity to variations in external conditions (*e.g.* ground plane proximity [6]), and provide spacing to meet voltage breakdown and clearance requirements. Fig. 6 illustrates a cut-away view of how these elements may be oriented and combined into a single package.

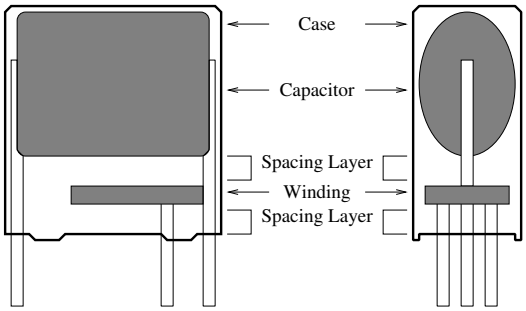


Fig. 6. Basic structure of an integrated filter element, where the magnetic winding is integrated with a capacitor into a single package.

The maximum desirable outline size for the magnetic winding is limited by the capacitor cross sectional area. However, it can be designed to have any number of layers and be constructed from any conductor thickness to obtain the appropriate inductance and series-path resistance.

The fabrication process for the integrated filter element considered here is composed of two primary tasks: first, the design and construction of the coupled magnetic winding; second, electrically connecting and encapsulating the capacitor and winding into a single physical package. The resulting integrated filter elements are tested and characterized to validate the design and fabrication process.

A. Winding Design and Fabrication

Guidelines for the design of inductance cancellation windings on printed circuit boards are given in [6], [7], and more thoroughly developed in [15]. However, the windings designed for integration can have a significantly smaller footprint than those used in the PCB designs, due to the increased thickness of the conductor that can be employed as compared to the thin traces on a PCB. In both cases, the winding should be designed with a mutual inductance equal to that of the equivalent series inductance of the capacitor of interest, including the contribution from any spacing layers.

For the winding designs considered here, an outer footprint is chosen to allow adequate clearance of the capacitor terminals and package edges. Both capacitors considered in this paper have a footprint shape similar to the one shown in Fig. 7, where the positioning of the winding relative to the capacitor footprint and terminals is illustrated by the dashed outline.

Analytical solutions for some geometries of coupled magnetic coils exist [16]–[18], however, the use of a CAD package such as FastHenry [19] greatly simplifies

Fig. 7. Example layout relationship for a winding footprint within the capacitor footprint.

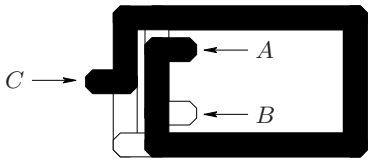


Fig. 8. Example two-layer inductance cancellation winding design to be used as a starting point for winding designs. The top layer is represented in solid black, and the bottom layer in white. The two layers are mirror images of each other and electrically connected at point C.

the process of calculating the inductance and resistance for arbitrary winding designs. While no rules of thumb have been developed to instantiate the design process, over the course of this work it has been found that a two-layer winding design is adequate for a wide range of capacitor package sizes from various manufacturers. Fig. 8 shows a typical two-layer winding pattern that can be used as a starting point for design.

The greatest benefit of a two-layer design comes from its relative simplicity and ease of fabrication. The winding can be inexpensively fabricated from a single-layer pattern that can be constructed from a sheet of conductive material with the appropriate thickness. The desired pattern can be formed in a number of ways: stamping, chemical etching, mechanical milling, or cutting with an abrasive jet (water-jet). This single-layer design can then be folded or joined into its final form. Fig. 9 shows a single-layer winding pattern that can be folded into the two-layer design illustrated in Fig. 8.

Additional leads must be attached to the winding at its endpoints to ensure they extend outside of the final encapsulation. This can be done by soldering or otherwise joining short wires perpendicular to the winding.

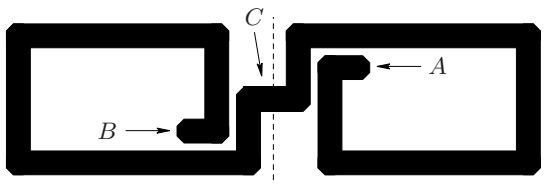


Fig. 9. Example inductance cancellation winding design shown in a single-layer pattern, which can be of folded into the design of Fig. 8.

Alternatively, the two external terminal leads can be constructed as part of the original winding pattern and bent appropriately to extend outward.

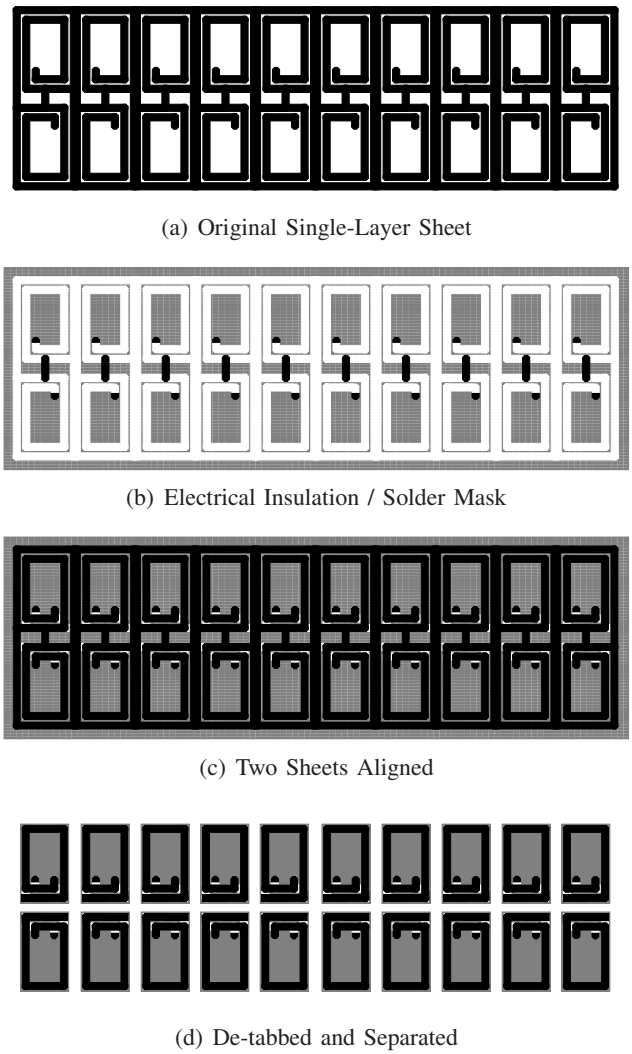
In a controlled manufacturing process, the forming and folding of the windings can be automated to provide a consistent, repeatable result. However, folding the windings individually by hand for prototyping purposes does not necessarily provide the same consistency. For this reason, an alternative process for constructing windings has been developed, which is suitable for either manual or automated fabrication.

The method depicted in Fig. 10 is ideal for forming many identical cancellation windings at a time. By cutting a number of single-layer patterns on a metal sheet such that they are held in by a number of cut-tabs (*e.g.*, as done with lead frames), an upper and lower sheet can be overlaid to align any number of windings simultaneously. If a symmetrical winding design is used, as is done here, a single pattern can be used for both the top and bottom sheets, with one of the two flipped to provide the mirrored pattern. This ensures that each winding is aligned identically to the others on the sheet, greatly reducing the part-to-part variation. The sheet of windings, as shown in Fig. 10(a), produces a total of twenty windings; the number of windings can be easily adjusted to scale from prototyping to volume production. The full process can be separated into three main steps: insulation masking, soldering and alignment, and de-tabbing to separate the windings from the sheet.

The two sheets are electrically insulated with a thin material, such as adhesive-backed Kapton tape, that can withstand temperatures used for joining. Mask holes are cut in the insulating material where the joints between layers will exist, and then solder paste is applied. To join the two sheets together, the top sheet is aligned over the lower one, then placed on a hot plate or in a solder reflow oven. The sheets should be fixed in place to avoid any movement as the solder paste melts and solidifies. After the joining of the two sheets, the windings can be removed from the sheet by cutting at the tabs. The windings are then ready to be integrated with capacitors.

B. Integration and Encapsulation

The process of integration involves electrically joining the cancellation winding with the capacitor and exposing the external terminals. One electrode of the capacitor remains as an external lead for the filter element, whereas the other is connected to the winding; the two endpoints of the winding become external leads of the filter element, forming a three-terminal filter component.



(a) Original Single-Layer Sheet

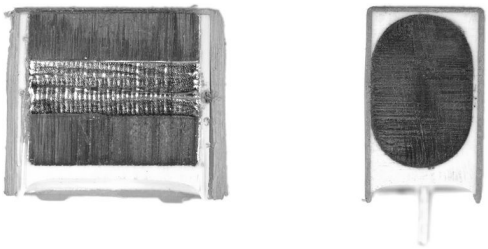
(b) Electrical Insulation / Solder Mask

(c) Two Sheets Aligned

(d) De-tabbed and Separated

Fig. 10. Steps to create a batch of windings from two sheets of a symmetrical single-layer pattern. Black represents the exposed conductor, gray is the insulating mask, and white represents the masked conductor.

Attaching the winding to the capacitor electrode should be done in a manner that can be precisely repeated, as the attachment location on the capacitor electrode impacts the effective shunt inductance of the filter element, in turn influencing the inductance cancellation performance. If the inductance cancellation winding is to be integrated as part of the initial capacitor fabrication process, the winding can be attached to the capacitor lead a specific distance from the metalized film roll a number of ways before encapsulation: placing insulating spacers between the capacitor-transformer and transformer-environment interfaces, forming detents in the filter casing to position the winding relative to the capacitor and case surface, setting the desired spacing by potting each device in separate stages, or controlling



(a) Side-cut (b) End-cut

Fig. 11. Cutaway photos of a Vishay BCcomponents Series MKP338 2222-338-24334 330 nF X2 film capacitor.

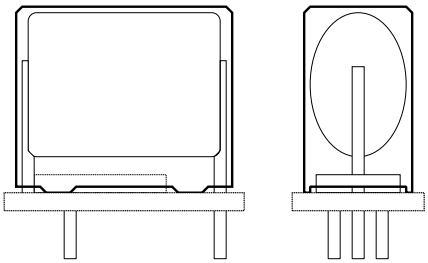


Fig. 12. Example fixture used to position the winding flush with the bottom of the capacitor casing for repeatable alignment and joining with the capacitor.

the insulator thickness of the winding. Multiple methods can be combined to achieve more complex insulation requirements.

If the capacitor is already potted, as shown in the cutaway capacitor of Fig. 11, the winding can be positioned a fixed distance from the bottom of the capacitor case instead, as the winding cannot be positioned directly against the potting compound at the bottom of the capacitor due to the inconsistent potting height, which varies measurably between capacitors. To position the winding relative to the bottom of the case, a small alignment fixture, shown in Fig. 12, is used to hold the winding, allowing it to be repeatably positioned on the capacitor for soldering.

With the capacitor and winding electrically connected and external leads brought out, the final step is to encapsulate the filter element. The encapsulation provides mechanical stability as well aselectrical isolation, and can be used to tune the final filter element performance by setting the spacing to the external interconnect point. The mechanical and electrical characteristics can be controlled by using different sized enclosures, adjusting the positioning of capacitor and winding, or using specialized potting compounds.

To provide adequate clearance between the winding and the bottom of the filter element in prototype designs,

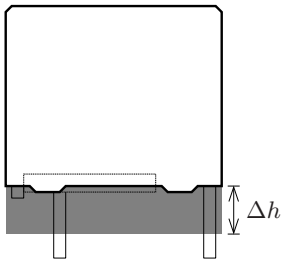


Fig. 13. Illustration of how the potting process can be used to control the filter element residual shunt inductance by modifying the height of the filter element, using the method shown in Fig. 16.

the height of the capacitor may need to be extended. The height may be increased by wrapping adhesive tape around the capacitor, leaving a small overhang at the bottom of the casing extending and past the cancellation winding. This cavity is then filled with a potting compound.

When setting the final filter element height using encapsulant, as shown in Fig. 13, the residual shunt inductance of the filter can be controlled: increasing the height to add additional inductance, or decreasing the height to reduce the inductance. For prototyping work, this allows a fine tuning of the filter element performance at the encapsulation stage without the need to change the winding design or alignment fixture.

C. Validation and Testing

Two measurement methods are used to validate the proper tuning and operation of the inductance cancellation for the integrated filter elements: a method based on multiple two-terminal impedance measurements, and a two-port insertion loss measurement. The impedance measurements are used to calculate the residual shunt inductance of the integrated filter, and insertion loss allows the frequency response of the filter element to be measured directly.

1) Two-Terminal Impedance Measurements: Measuring the residual shunt inductance of the filter element provides a single value that can be used to compare devices and to verify that the fabrication method is providing consistent results. The measured parameters can also be used to determine the parameter values of the filter T-model for use in circuit simulation packages such as SPICE.

Measurements of the inductance between terminals AB, BC', and AC' are required to determine the inductance parameters in the T-model of Fig. 5. These three measurements can be written as

$$L_{AB} = L_{11} + L_{22} \quad (1)$$
$$L_{BC'} = L_{22} - L'_{12} \quad (2)$$
$$L_{AC'} = L_{11} - L'_{12} \quad (3)$$

where L'_{12} is the residual shunt inductance, representing the sum of the cancellation winding mutual inductance, the capacitor equivalent series inductance, and any secondary effects due to inductive coupling between the winding and capacitor. The value of L'_{12}, L_{11}, and L_{22} can be found from the three measurements, using

$$L_{11} = \frac{L_{AB} + L_{AC'} - L_{BC'}}{2} \quad (4)$$
$$L'_{12} = \frac{L_{AB} - L_{BC'} - L_{AC'}}{2} \quad (5)$$
$$L_{22} = \frac{L_{AB} + L_{BC'} - L_{AC'}}{2}. \quad (6)$$

Ideally, the residual shunt inductance L'_{12} is zero. If the residual is less than zero, there is too much cancellation; if the residual is greater than zero, too little. The measured residual is most useful to evaluate the *relative* variance between filter elements in the fabrication process, and not strictly as a measure of general filter performance.

2) Two-Port Insertion Loss Measurement: Insertion loss is a measurement of the attenuation of a filter, and is a common method for evaluating the performance of EMI filters [20]. In the most simplistic arrangement, the measurement is made with a sinusoidal input source with a series impedance driving the input port of the filter, while a load impedance is placed across the output port. The ratio between the magnitude of the source voltage and output terminal voltage measured across the load impedance is the filter insertion loss, and is reported in dB. The insertion loss measurements are most easily taken using a network analyzer which provides the 50Ω source and load impedances internally. Fig. 14 illustrates the measurement setup. Measurements in this paper are made in accordance with those used to evaluate inductance cancellation performance in [5], [15] to allow for direct performance comparison. The filter responses presented in [6] unfortunately are not those of insertion loss, and thus are not directly comparable; however, insertion-loss measurements for these filters appear in [15]. The use of a printed circuit board measurement fixture, as shown in Fig. 15, ensures that the measurement mimics realistic filter element usage as closely as possible.

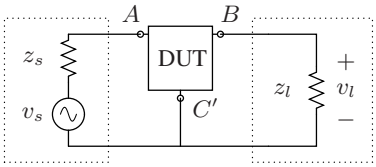


Fig. 14. Measurement setup for two-port insertion loss measurements. Impedances z_s and z_l are 50Ω.

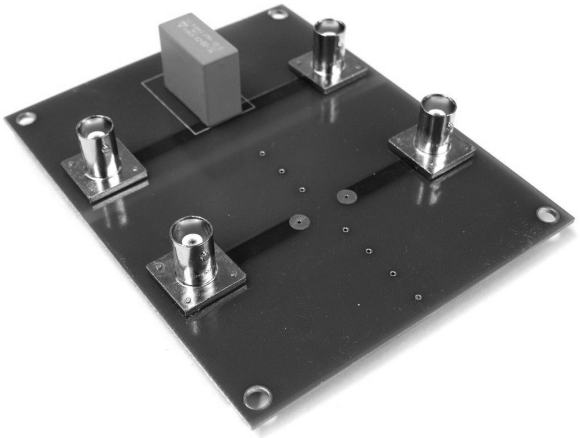


Fig. 15. Photograph of printed circuit board measurement fixture used in the two-port network measurement shown in Fig 14. The mounted capacitor is used as a reference.

With the PCB measurement fixture and a three terminal filter element, the filter performance can be interactively modified by raising and lowering the element with respect to the circuit board, then observing the change in frequency response. By raising the filter element, the length of terminal C' is increased, thereby increasing the effective shunt inductance of the filter element, shown in Fig 16. The change in inductance can be approximated [3] by

$$\Delta L = \mu_0 \frac{A}{w} \quad (7)$$

where A and w are illustrated in Fig 16. This approximate relationship is valid for $\Delta h \ll w$, which should hold for many common sizes of integrated filter elements, providing an intuitive tool for adjusting winding inductances.

This method of adjusting the filter element shunt inductance can be used to determine how close the filter element inductance cancellation is to "optimal". While intuitively it seems that the optimal output response would occur when the residual shunt inductance is zero, it is often advantageous for a small positive inductance to remain. The proper residual shunt inductance allows the resonant frequency of the filter to be positioned

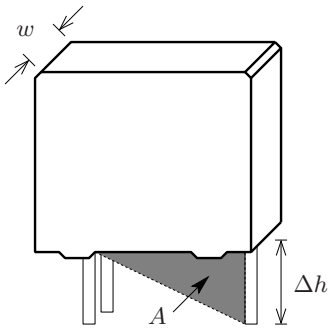


Fig. 16. The effective shunt inductance of an integrated filter element can be increased by lifting the capacitor off the testing fixture to increase loop area.

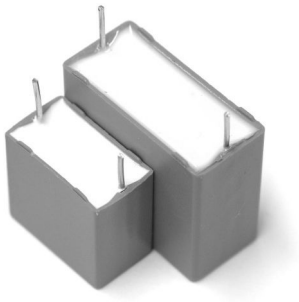


Fig. 17. Photograph of two Vishay BCcomponents Series MKP338 capacitors in 330 nF and 1.0 μF values. Figs. 18 and 22 contain the outer dimensions of each respective capacitor.

near the highest frequency of interest; the insertion loss is increased near the resonance due to the reactive cancellation in the shunt path.

III. Implementation Examples

Using the design, fabrication, and measurement methods developed in Section II, two separate integrated filter element designs are presented here. The two selected capacitors are representative of capacitors used in many EMI filters. Vishay BCcomponents Series MKP338 capacitors in 330 nF and 1.0 μF, part numbers 2222-338-24334 and 2222-338-24105 respectively, are X2 rated polyester-film capacitors, indicating they are approved for both line-to-line and line-to-ground configurations. The two capacitors differ primarily in their capacitance ratings and physical package size; Fig. 17 shows a photograph of the two capacitors. The size difference between the capacitors is indicative of their relative equivalent series inductances; the 1.0 μF capacitor is larger, and has a larger average inductive loop area and equivalent series inductance. The capacitance ratings of the capacitors are illustrative of their use: the 1.0 μF capacitor is more likely to be used in filters with a higher current rating than the 330 nF capacitor.

For both capacitors, twenty integrated elements were fabricated to determine the repeatability of the fabrication method. The windings were constructed using the methods described in Section II-A for fabricating multiple windings simultaneously.

In this section, all simulated inductance values are generated using the FastHenry [19] three-dimensional inductance extraction program. Measured inductance values are taken using an Agilent 4395A Network/Impedance/Spectrum Analyzer at 30MHz, the same frequency as the simulations. The Agilent 4395A is also used for the two-port network measurements of insertion-loss, which provides the 50Ω source and load impedances.

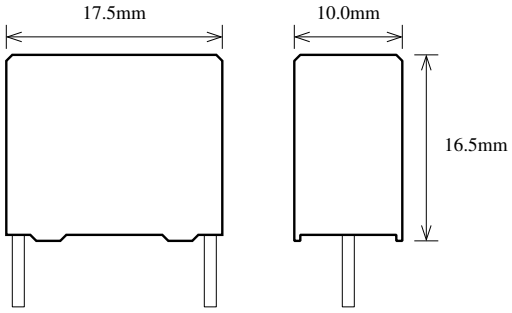


Fig. 18. Dimensioned illustration of Vishay BCcomponents 2222-338-24334 capacitor.

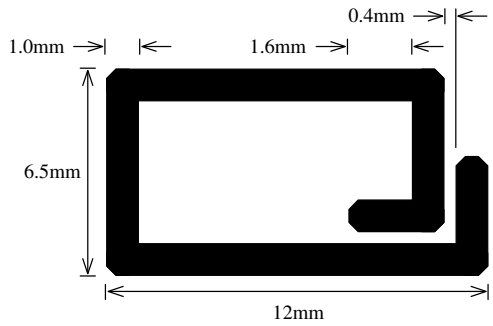
A. Vishay BCcomponents 2222-338-24334 330 nF

This capacitor outline and dimensions are shown in Fig. 18. The measured equivalent series inductance is 9.9 nH.

1) Winding Design: The filter winding is designed to carry series current of up to 5A, with a loss of no more than 0.01% of the power at 240V. This corresponds to a series path resistance of less than 4.8mΩ.

The winding inductance is designed to offset the capacitor equivalent series inductance of 9.9 nH. Using the basic design of the example coil in Fig. 8 as a starting point, the final two-layer coil design shown in Fig. 19 was developed. The single-layer pattern, fabricated from a 1 mm-thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 20 shows both the single-layer winding as originally cut and the winding after the structure has been insulated, folded, and joined into its final two layer form.

Simulation of the winding at 30MHz results in an inductance matrix



(a) Two-Layer Folded

(b) Single-Layer Unfolded

Fig. 19. Inductance cancellation winding design for use with the Vishay BCcomponents 330 nF capacitor. Both the two-layer folded and single-layer unfolded designs are shown. The winding is fabricated from 1 mm-thick copper.

(a) Cut pattern (b) Final Assembly

Fig. 20. Inductance cancellation winding photos of single-layer pattern and final two-layer construction for the 330 nF integrated filter element.

$$L_{sim} = \begin{bmatrix} 14.8 & 11.2 \\ 11.2 & 14.8 \end{bmatrix} \text{nH}$$

and a simulated winding resistance of 2.5mΩ at 60Hz. The measured winding inductances at 30MHz (of one winding selected at random) result in the inductance matrix

$$L_{meas} = \begin{bmatrix} 26.0 & 8.5 \\ 8.5 & 25.1 \end{bmatrix} \text{nH}$$

and a measured winding resistance of 3mΩ at 60Hz.

The measured inductance matrix shows a significant departure from the simulation. This is in part due to the additional interconnect length required to mount the winding on the measurement fixture, which is not reflected in the simulation results. The mutual inductance value is sufficiently close, however, to justify the use of FastHenry for estimation purposes provided the designer takes into account the (consistent) variation between the simulation and real-world measurement setup.

Fig. 21. Photograph of a completed 330 nF integrated filter element with inductance cancellation. The resulting package height is 1.75 mm taller than the original capacitor casing.

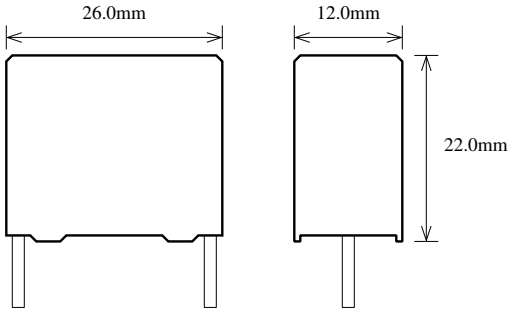


Fig. 22. Dimensioned illustration of Vishay BCcomponents 2222-338-24105 capacitor.

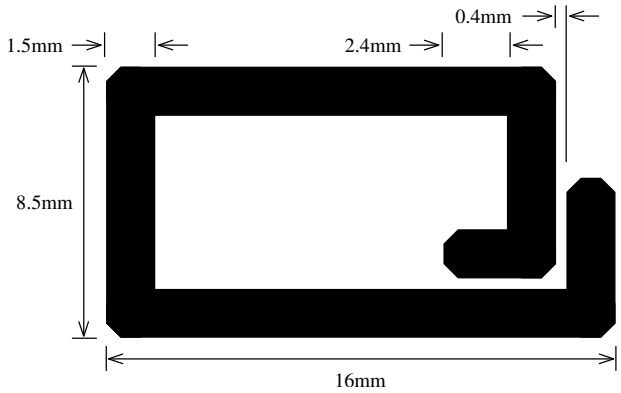
2) Integration and Encapsulation: The final filter element potting height is determined by the desired residual shunt inductance, which determines the filtering characteristics of the device. This height is determined experimentally using the two-port insertion-loss measurements described in Section IV. A sacrificial capacitor and magnetic winding were used to determine the optimal potting height, and this same height was used on all subsequent elements in the batch. The final fabrication result for the 330 nF integrated filter element is shown in Fig. 21. The three terminal device is 1.75 mm taller than the original capacitor casing.

The performance of this integrated filter design is investigated in Section IV.

B. Vishay BCcomponents 2222-338-24105 1.0 μF

This capacitor outline and dimensions are shown in Fig. 22. The measured equivalent series inductance is 13.3 nH.

1) Winding Design: The filter winding is designed to carry a series current of 10A, with a loss of no more than 0.01% of the power at 240V. This corresponds to a series path resistance of less than 2.4mΩ. The winding inductance is designed to offset the capacitor



(a) Two-Layer Folded

(b) Single-Layer Unfolded

Fig. 23. Inductance cancellation winding design for use with the Vishay BCcomponents 1.0 μF capacitor. Shown in both the two-layer folded and single-layer unfolded designs. The winding is fabricated from 1 mm-thick copper.

(a) Cut pattern (b) Final Assembly

Fig. 24. Inductance cancellation winding photos of single-layer pattern and final two-layer construction for the 1.0 μF integrated filter element.

equivalent series inductance of 13.3 nH. Using the basic design of the example coil in Fig. 8 as a starting point, the final two-layer coil design shown in Fig. 23 was developed. The single-layer pattern, fabricated from a 1 mm-thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 24(a) shows the single-layer winding as originally cut, and Fig. 24(b) shows the winding after the structure has been insulated and joined into its final two-layer design.

The simulated winding inductances at 30MHz result in an inductance matrix

$$L_{sim} = \begin{bmatrix} 18.6 & 14.8 \\ 14.8 & 18.6 \end{bmatrix} \text{nH}$$

and a simulated winding resistance of 2.0mΩ at 60Hz.

Fig. 25. Photograph of a completed 1.0 μF integrated filter element with inductance cancellation. The resulting package height is 1.2 mm taller than the original capacitor casing.

The measured winding inductances at 30MHz (of one winding selected at random) result in the inductance matrix

$$L_{meas} = \begin{bmatrix} 34.0 & 12.7 \\ 12.7 & 32.6 \end{bmatrix} \text{nH}$$

and a measured winding resistance of 2mΩ at 60Hz.

Again, the variation between the simulated and measured inductance matrices is significant due to the added interconnect required for the measurement; however, the mutual inductance term L_{12} remains reasonably close for the purposes of estimation.

2) Integration and Encapsulation: The final filter element potting height is determined by the methods described in Section IV. A sacrificial capacitor and magnetic winding were used to determine the optimal potting height; this height was used on all subsequent elements in the batch. The final fabrication result for the 1.0 μF integrated filter element is shown in Fig. 25. The three-terminal device is 1.2 mm taller than the original capacitor casing.

The performance of this integrated filter design is investigated in Section IV.

IV. Fabrication Results

To determine the relative precision of the filter element construction, each batch of twenty filter elements fabricated in Section III was characterized using measurements of the residual shunt inductance and insertion loss as described in Section II-C.

The residual shunt inductance of each filter was found using the three two-terminal impedance measurements in (5), then offset by the geometric mean of all twenty filter elements in the batch to provide a zero-centered measurement. Centering the residual inductances around zero

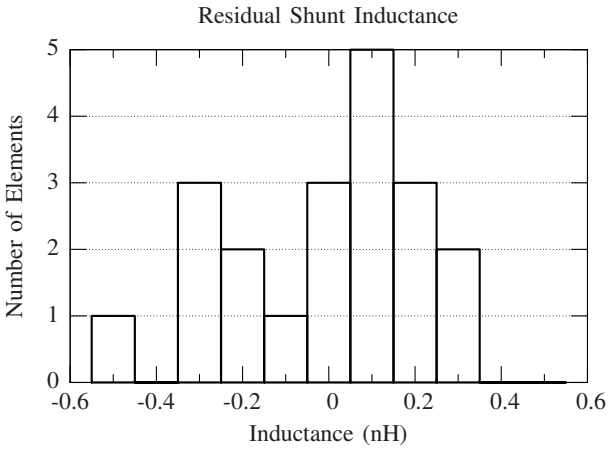


Fig. 26. Zero-centered histogram of measured residual shunt inductance values of twenty 330 nF integrated filter elements.

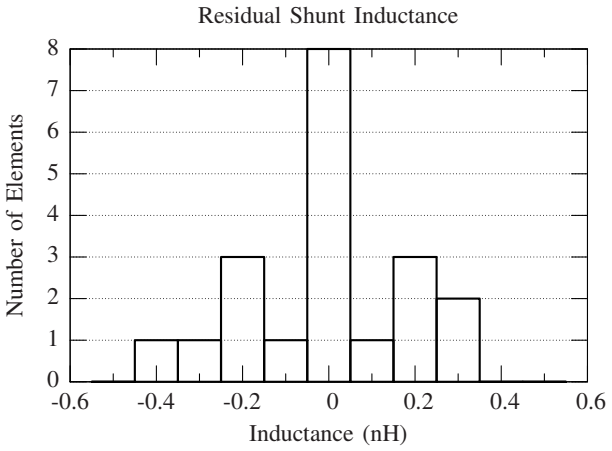


Fig. 27. Zero-centered histogram of measured residual shunt inductance values of twenty 1.0 μF integrated filter elements.

eliminates the inductance of the measurement apparatus and illustrates the error *relative* to the other elements, not necessarily to a specific target residual shunt inductance. Histograms of the residual shunt inductance are presented in Figs. 26 and 27 for the 330 nF and 1.0 μF devices, offset by 1.89 nH and 5.09 nH respectively. This illustrates a maximum variation of 0.88 nH and 0.68 nH, with corresponding standard deviations of 0.24 nH and 0.19 nH, for the 330 nF and 1.0 μF filter element batches respectively. Additionally, it may be useful to consider this data in a normalized form, scaled by the magnitude of the initial capacitor equivalent inductances to allow a comparison between designs. This results in maximum part-to-part variation measurement of 8% and 5%, and standard deviations of 2.4% and 1.9% for the 330 nF and 1.0 μF filter elements respectively.

Fig. 28 plots the frequency response for each batch of filter elements, along with the original capacitor responses. Both integrated filter elements show a significant improvement in performance over their capacitor-only equivalents, gaining more insertion-loss at the higher frequencies where the equivalent series inductance would normally dominate. At 30MHz, the upper bound of the conducted EMI specification [2], the 330 nF and 1.0 μF filter elements both show a minimum improvement of 20 dB. An interesting result in both filter element responses is the unveiling of the resonance located in the low- to mid-frequency range of the figures. This small resonance results from the distributed nature of the capacitor [21], and is normally insignificant relative to the dominating interconnect inductance.

A plot of the difference between the largest and smallest insertion-loss values for both filters is given in Fig. 29, illustrating the maximum variation between filter elements. The maximum variation across the frequency range is 4.1 dB for the 330 nF device and 3.5 dB for the 1.0 μF. This variation can be considered acceptable especially given the greater than 20 dB minimum improvement in insertion-loss obtained at high frequencies. Additionally, the insertion-loss measurements of the 330 nF integrated filter elements can be compared directly with the results presented in [15] for the 330 nF capacitor with inductance cancellation implemented using printed circuit board windings. The use of PCB windings for inductance cancellation appears to offer only a slight decrease in the maximum insertion-loss variation when compared to the hand fabricated integrated filter elements presented here.

V. Conclusion

This paper presents an implementation of inductance cancellation where the coupled magnetic winding is co-packaged with the capacitor to form a self-contained integrated filter element. A design methodology and fabrication procedure is presented, and the integrated filter elements constructed using this fabrication method are shown to have substantial performance improvements over standard capacitors with a low part-to-part variation.

The resulting filter element characteristics and performance measurements validate the feasibility of fabricating devices with repeatable performance results using low-cost construction methods. Additional gains in device repeatability can be expected with a refined process and/or mechanized fabrication and assembly. The approach presented here offers a compelling combination

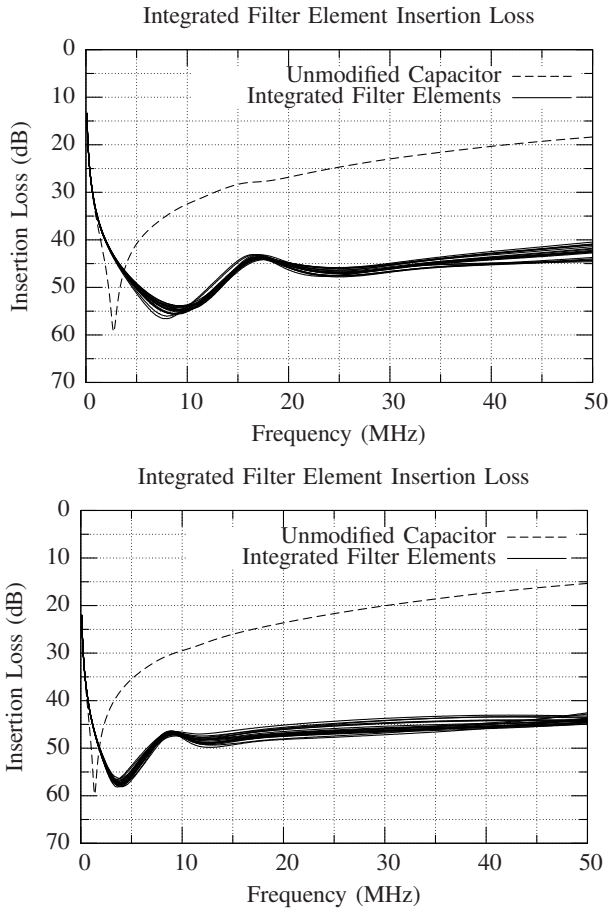


Fig. 28. Insertion-loss measurements for twenty 330 nF (top) and 1.0 μF (bottom) integrated filter elements.

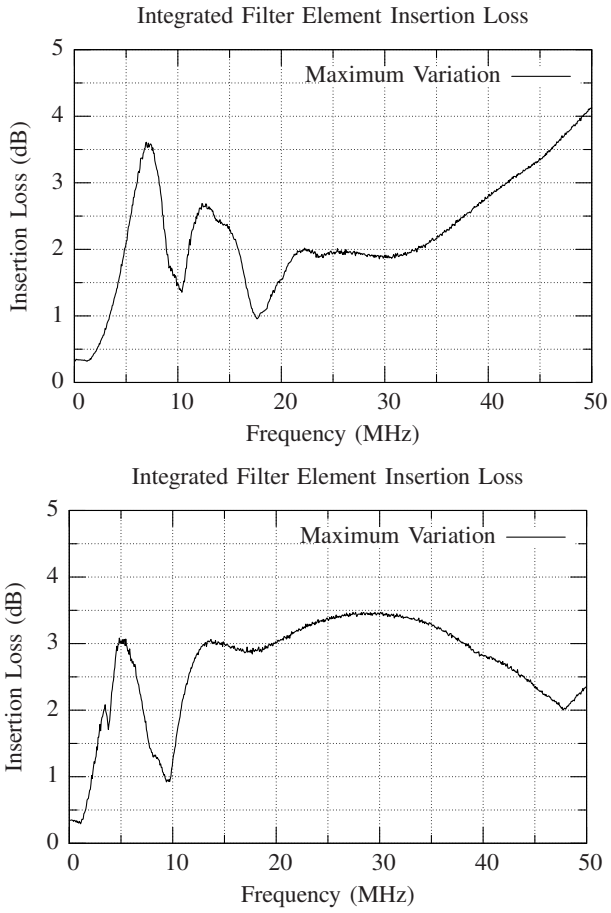


Fig. 29. Maximum variation of insertion-loss measurements for twenty 330 nF (top) and 1.0 μF (bottom) integrated filter elements.

of substantial performance improvements, repeatability, and ease of manufacture.

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