Very High Frequency Resonant Boost Converters

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***Abstract* - This document presents a resonant boost topology suitable for very high frequency (VHF, 30-300 MHz) dc-dc power conversion. The proposed design features low device stress, high efficiency over a wide load range, and excellent transient performance. Two experimental prototypes have been built and evaluated. One is a 110 MHz, 23 W converter which uses a high performance rf LDMOSFET. The converter achieves higher than 87% efficiency at nominal input and output voltages, and maintains good efficiency down to 5% of full load. The second implementation, aimed towards integration, is a 50 MHz 17 W converter which uses a transistor from a 50 V integrated power process. In addition, two resonant gate drive schemes suitable for VHF operation are presented, both of which provide rapid startup and low-loss operation. Both converters regulate the output using high-bandwidth on-off hysteretic control, which enables fast transient response and efficient light-load operation. The low energy storage requirements of the converters allow the use of coreless inductors in both designs, thereby eliminating magnetic core loss and introducing the possibility of easy integration.**

***Index Terms* - resonant dc-dc converter, resonant boost converter, very high frequency, VHF integrated power converter, class Φ inverter, class F power amplifier, class E inverter, resonant gate drive, self-oscillating gate drive, resonant rectifier, harmonic peaking.**

I. Introduction

THERE is an increasing demand for power electronics having reduced size, weight, and cost as well as improved dynamic performance. Passive components (inductors and capacitors) typically dominate the size and weight of a power converter. Increased switching frequency leads to a reduction in the required energy storage and permits use of smaller passive components. Furthermore, higher frequency can substantially improve transient performance and control bandwidth. Sufficiently high frequencies permit the use of coreless magnetics, paving the way towards fully integrated power converters. It is thus evident that many benefits can be realized by operating power converters at greatly increased switching frequencies if loss, efficiency, and control challenges can be addressed.

Soft switched resonant dc-dc power converters are able to maintain high efficiency for increased switching frequency. Because of their resonant nature, however, they typically suffer from high device stresses [1]–[12]. Furthermore, as can be seen in [1]–[3], [6]–[8], [10], it is often difficult to maintain high efficiency over a wide load range with resonant converters.

This paper introduces a resonant boost converter topology and control method suitable for designs at very high frequency (VHF, 30-300 MHz). The topology provides low transistor voltage stress, and requires small passive components, allowing for very fast transient response. Moreover, the design maintains high efficiency across a wide load range. Section II presents the new topology and discusses its design and operation. Two low-loss resonant gate drive schemes suitable for this topology are detailed in Section III, followed by an explanation of the converter control method in Section IV. Section V presents the design and experimental validation of two converters implementing the approach. The first is a 110 MHz, 23 W converter based on a high-performance rf LDMOSFET. The second is a 50 MHz, 17 W design implemented with an LDMOSFET from a 50 V integrated power process.

II. A New Resonant Boost Topology

Figure 1 shows a schematic of the new resonant boost dc-dc converter topology. The design is optimized for low device stress and very high frequency operation at a fixed frequency and duty ratio. This enables the use of resonant gating and zero-voltage switching for high efficiency. The output is regulated by on-off control of the converter (also sometimes called burst-mode control or cell-modulation control [11]–[13]).

The converter can be viewed as a special version of the Class Φ inverter described in [14]–[18], coupled with a resonant rectifier. The multiresonant network comprising L_F, L_{2F}, C_F and C_{2F} is a low-order network designed to approximate the symmetrizing properties of a quarter-wave transmission line [14]–[18]. This network can be tuned to achieve zero voltage switching while at the same time maintaining low device voltage stress. In particular, the drain to source voltage can be shaped to approximate a quasi-square or trapezoidal wave shape, thereby reducing voltage stress across the switch

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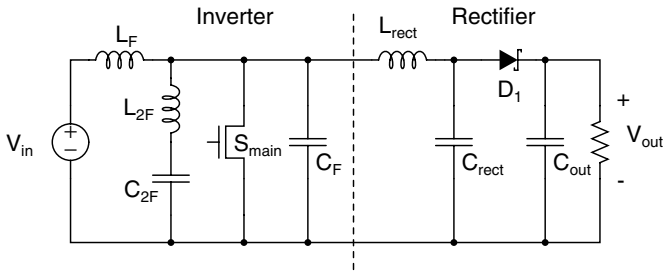

Fig. 1. Schematic of the proposed resonant boost converter topology.

S_{main} as compared to other single-switch inverters such as the class E inverter. To accomplish this, the components L_F, L_{2F}, C_F and C_{2F} are tuned in the following manner [17], [18]:

L_{2F} and C_{2F} are tuned to resonate near the second harmonic of the switching frequency f_s to present a low drain to source impedance at the second harmonic. In addition, the components L_F and C_F are tuned in conjunction with L_{2F} and C_{2F} and the load impedance to present a high drain to source impedance near the fundamental and third harmonic of f_s. The relative impedance between the fundamental and third harmonic can be adjusted to shape the drain to source voltage to approximate a square wave, an effective means to limit the peak switch voltage stress [17], [18].

A complete discussion of the tuning methodology for these components is found in [18]. It is worth reiterating here that L_F, L_{2F}, and C_{2F} can be selected relative to the component C_F in a manner that permits the parasitic output capacitance of the switch to be fully absorbed by the multiresonant network. Consequently, C_F can comprise only the parasitic switch capacitance, or if so desired, can be augmented with an additional discrete capacitor in parallel with the switch.

The inverter is coupled to a resonant rectifier, as shown on the right side of Figure 1. This rectifier is similar to that described in [19] and analyzed in [20], albeit with somewhat different operating characteristics owing to our use of on-off control to regulate the output. The substitution of the properly tuned rectifier for the inverter load resistance can be accomplished with minimal effect on the inverter. The pairing is done in a way that allows dc power flow from input to output. Since the fraction of total power that is transferred at dc is not subject to losses in the switch or resonant elements, higher efficiency can be achieved as compared to a design that delivers all the power via ac coupling.

The resonant elements L_{rect} and C_{rect} of Figure 1 are chosen so that the rectifier delivers the desired power at the specified output voltage. In the rectifier topology presented, the parasitic capacitance of the diode is absorbed by C_{rect}. The discrete capacitor C_{rect} can therefore be reduced, and in some cases completely eliminated when all of the required capacitance is provided by the diode.

Tuning the rectifier may be accomplished by parameterizing L_{rect} and C_{rect} (in this case the sum of diode and external capacitance) in terms of an effective center frequency and characteristic impedance. The center frequency is chosen to make the rectifier appear resistive at the switching frequency when it is driven by a voltage equal to the fundamental of the inverter drain voltage and loaded with a constant dc voltage[1]. The characteristic impedance, Z_o, determines the value of the equivalent resistance of the rectifier. Selection of characteristic impedance is used to control power delivered by the rectifier, with lower Z_o corresponding to lower equivalent resistance. It should be noted that finite diode capacitance will limit both the center frequency and characteristic impedance that can be achieved.

An entire converter design may be accomplished by first designing an inverter and adjusting the rectifier parameters to match the inverter load and then connecting the two. The process may be carried out in reverse order by first designing a rectifier, extracting the equivalent rectifier resistance, and then designing the inverter. In both cases, ac and dc power may be considered independently and the design proceeds accounting only for ac power. When the rectifier and inverter are connected, the total power is typically close to the design power, and may be adjusted to match precisely via the methods outlined in [21].

III. Gate Driver

At VHF frequencies, traditional hard-switched gating typically incurs too much loss for acceptable efficiency. Instead, with a power stage and control scheme designed to operate at a fixed frequency and duty ratio, resonant gating becomes advantageous. By recovering a portion of the gate energy each cycle, much lower power is required to drive the gate, minimizing the effect gating has on overall converter efficiency.

In addition to achieving low power operation, a practical gate drive must reach steady-state rapidly at startup and shutdown to maintain good converter transient response and high efficiency under on-off modulation. To that end, two different low-loss gate drives were designed, one for optimum efficiency and one for easier integration.

In the case of the 110MHz converter, the gate terminal of the switch cannot be driven below the source due to a protection diode integrated with the switch. For this reason, a scheme similar to that presented in [12] was developed. This gate drive realizes a trapezoidal gate waveform which does not drive the gate-source voltage negative, and which yields near minimum loss. The design here, depicted in Figure 2, utilizes fewer parts and achieves a faster startup time than the design in [12]. It is based on the inverter presented in Section II, and uses a low-order lumped network to shape the main-switch gate voltage to be approximately trapezoidal. Added components provide a gate signal to the auxiliary MOSFET, S_{aux}, such that a self-sustained oscillation is achieved. The inductor L_{start} helps to initiate this oscillation when the voltage V_{gate} is applied. Component values for this gate driver are presented in Table I.

The second gate drive scheme was designed with integration in mind and applied in the 50 MHz converter. A resonant drive circuit was sought with as few passive components as possible. The selected approach is similar to that in [22], [23], though different in how the network is tuned. Since the MOSFET in

[1]That is, we create a describing function model for the ac impedance presented by the rectifier.

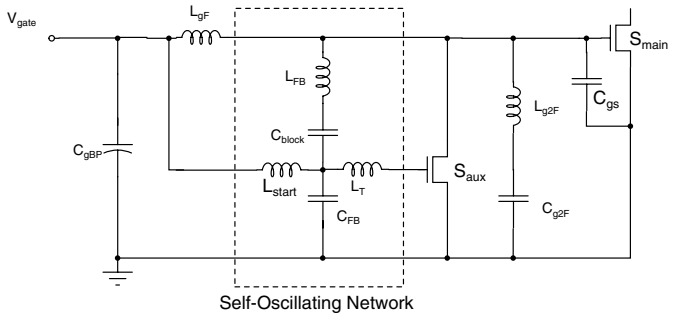

Fig. 2. Trapezoidal resonant gate drive circuit with self-oscillating network. The converter is enabled by applying the voltage V_{gate}, and disabled by setting V_{gate} to zero. This gate driver is employed in the 110 MHz converter (Figure 5).

TABLE I
GATE DRIVE COMPONENT VALUES

50 MHz Design		110 MHz Design	
R_T	2.5 kΩ	L_{gF}	5.5 nH
C_T	15 pF	L_{start}	13 nH
C_B C_P	100 nF	L_{FB}	82 nH
L_S	56 nH	C_{FB}	56 pF
L_P	47 nH	C_{block}	100 pF
R_1	100 kΩ	L_T	68 nH
Q_1	FDV303N	L_{g2F}	3.8 nH
D_1	MA27D27	C_{g2F}	139 pF
Inverter	NC7WZ04	S_{aux}	Polyfet L8821P
		C_{gBP}	5.6 nF

this case can sustain negative V_{GS}, the resonant driver of Figure 3 could be used. In this network, the inductor L_S resonates with C_{ISS} to reduce its apparent value. The inductor L_P is chosen to provide a peak in the transfer function $\frac{V_G}{V_1}$ at the switching frequency, with the capacitor C_P selected as a short at that frequency. An additional constraint is that both inductors are chosen such that when the net reactance is considered together with C_{GD}, the transfer function $\frac{V_{GS}}{V_{DS}}$ satisfies the phase condition for self-sustained oscillation. Since the magnitude condition cannot be satisfied, additional energy is added to the network via a bank of paralleled CMOS inverters. Tuning the network in this way reduces the current through the CMOS inverters, thereby reducing their number and associated losses. The CMOS inverters are driven by one additional inverter configured as a single-stage ring oscillator set to 50 MHz. The gate drive network is able to reach periodic steady state in just over 74 ns which is sufficiently fast for this application. Component values for this gate drive are shown in Table I. More details of the two gate drives appear in [21], [24]

IV. CONTROL STRATEGY

The control strategy employed is an on-off hysteretic control scheme [11]–[13]. When the output voltage falls below a specified threshold, the converter is enabled and delivers power to the output, causing the output voltage to gradually increase. When the output rises above a specified threshold, the converter is disabled, and the output voltage will gradually decrease. Effectively, load power is controlled by changing the

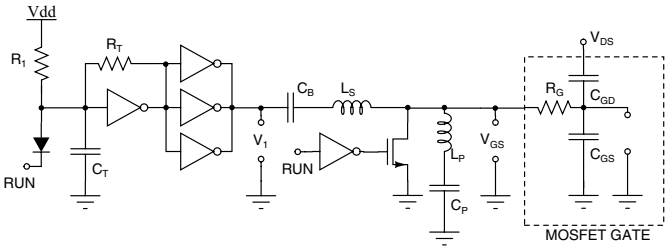

Fig. 3. Sinusoidal resonant gate drive circuit. This driver is employed in the 50 MHz converter (Figure 12).

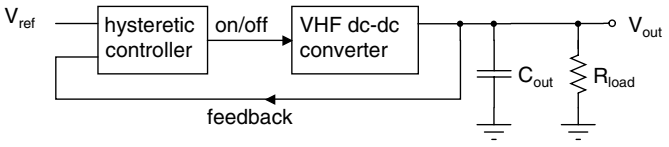

Fig. 4. A block diagram illustrating on/off control of a VHF resonant dc-dc converter. This control strategy enables efficient operation over a wide load range and allows the converter to be optimized for a fixed frequency and duty ratio.

duty ratio with which the converter is modulated on and off. Such a strategy is possible at VHF because the minimal energy storage required allows for rapid start-up and shut-down of the entire power stage.

This scheme realizes the advantages of separating the control and power processing functions. When the converter is on, it operates at a fixed high-efficiency point. When the converter is off, many of its loss mechanisms are removed. The result is efficient operation over a much wider load range than can be achieved with many other strategies.

Figure 4 illustrates this approach. The bulk output capacitance C_{out} is sized to achieve an intended on-off modulation frequency given a load range and the desired ripple voltage. Smaller capacitance will result in higher modulation frequency. Generally, converter efficiency decreases as modulation frequency increases, suggesting a trade-off between bulk capacitor size and efficiency, though the details are somewhat more complicated. It should be noted that the bulk converter input capacitance must also deal with ripple components near the modulation frequency. Nevertheless, the main power stage components are sized based on the very high switching frequency, enabling miniaturization and fast transient response.

The basic scheme presented in Figure 4 utilizes a hysteretic comparator, a voltage reference to set the DC level, and a voltage divider to sense the output voltage. The ripple voltage is determined by the comparator and is equal to the hysteresis band times the divider ratio. Bulk capacitance is added at the output and sized according to the desired modulation frequency range and expected load. It is important to note that the transient performance of the converter is not determined by the modulation frequency, but by the delay around the control loop and the switching frequency of the converter.

V. EXPERIMENTAL RESULTS

This section presents the design and experimental evaluation of two converters of the type proposed here. The first operates

TABLE II

EXPERIMENTAL DC-DC CONVERTER SPECIFICATIONS

Nominal Input Voltage	14.4 V
Nominal Output Voltage	33 V
Input Voltage Range	8 - 16 V
Output Voltage Range	22 - 34 V
Switching Frequency	110 MHz
Nominal Output Power	23 W
Gate Drive Input Voltage	3.6 V

TABLE III

POWER STAGE COMPONENT VALUES

Component	110 MHz Design	50 MHz Design
L_F	33 nH	22nH
L_{2F}	12.5 nH	22 nH
L_{rect}	22 nH	56 nH
C_{2F}	39 pF	115 pF
C_{rect}	10 pF	47 pF
C_{out}	70 μF	40 μF
S_{main}	Freescale MRF6S9060	Integrated process
D_1	Fairchild S310	Fairchild S310

at 110 MHz and uses a high-performance rf LDMOSFET, while the second operates at 50 MHz using an LDMOSFET fabricated in an integrated power process.

A. 110 MHz High Performance Implementation

A dc-dc converter based on the topology introduced in Section II and operated at 110 MHz was built and evaluated [24]. Table II lists the converter specifications.

A photograph of the prototype is shown in Figure 5. The values of the power stage components are given in Table III. Note that the capacitor C_F is provided entirely by the parasitic switch output capacitance, C_{oss}. The control circuitry that regulates the output voltage is placed on the other side of the printed circuit board (not shown).

As can be seen in Table III, the largest inductor in the power stage is 33 nH. The small sizes of the inductors are due both to the high operating frequency of the converter (110 MHz), and to the nature of the topology introduced in Section II.

Converter waveforms are presented in Figure 6, which shows measured drain and gate voltages for $V_{in} = 14.4$ V and $V_{out} = 33$ V. Good zero voltage switching characteristics are observed, and the peak device voltage stress is acceptable. As will be seen in the following section, peak device stress

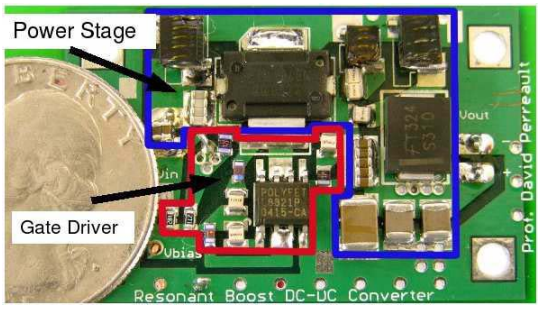

Fig. 5. Photograph of the 110 MHz prototype converter with a U.S. quarter shown for scale.

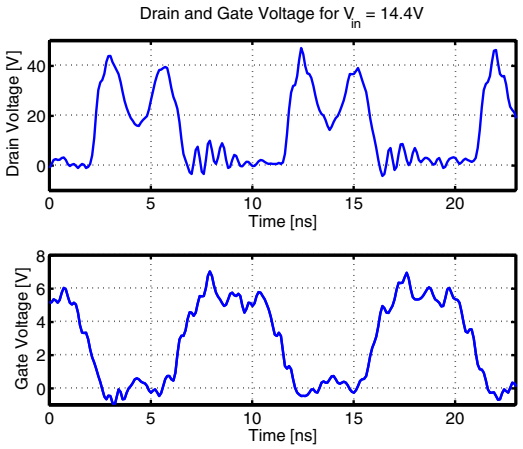

Fig. 6. Drain and gate voltage for experimental 110 MHz converter operating with V_{in} = 14.4 V and V_{out} = 33 V.

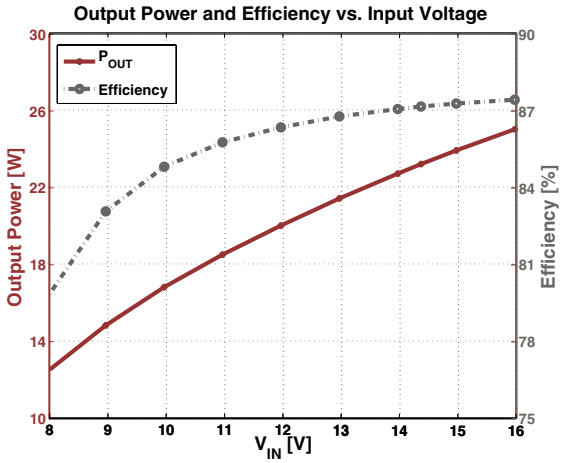

Fig. 7. Open-loop power and efficiency of the 110 MHz converter over the input voltage range for the 110 MHz converter, with V_{out} fixed at 32 V.

can be controlled by design and traded off against other characteristics. Open-loop efficiency and power over the input voltage range are illustrated in Figure 7, where the input voltage is swept from 8 to 16 V, and the output voltage is kept constant at 32 V. This and all following efficiency measurements include the losses of the gate driver and control circuitry, which were powered from the converter input.

Figure 8 shows the output voltage ripple when the converter is regulating the output at 32.4 V. The approximately 200 mV ripple is set by the hysteresis band of the controller and is independent of the output capacitance of the converter. The modulation frequency at which the converter is turned on and off is set by the load resistance, hysteresis band, and output capacitance, and is 50 kHz in the example of Figure 8. If a smaller output capacitance is desired, this modulation frequency can be set as high as several hundred kHz with no noticeable decline in efficiency. The lower part of the figure shows the drain to source voltage of the main switch, and illustrates how the converter is turned on and off as the output is regulated. It is important to note that while the on-off modulation frequency in Figure 8 is 50 kHz, the converter

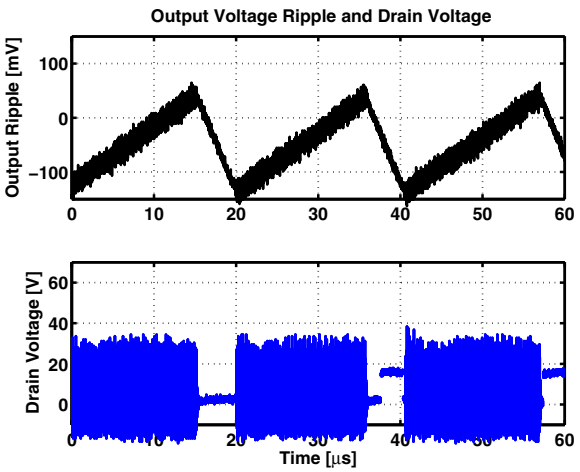

Fig. 8. Top: Converter output voltage ripple of the 110 MHz converter for V_{in} = 14.4 V $V_{out,DC}$ = 32.4 V. Bottom: Drain voltage illustrating on-off control.

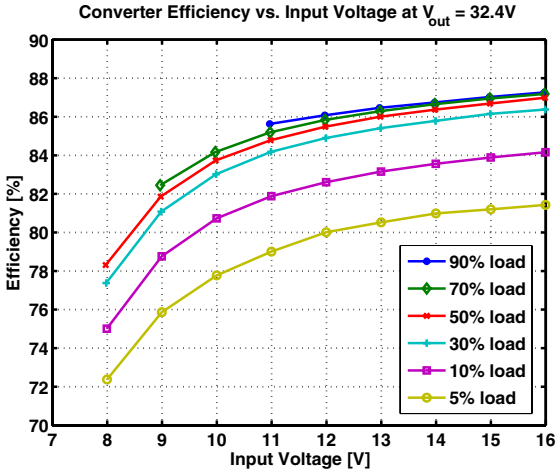

Fig. 9. Closed-loop efficiency of the 110 MHz converter over the input voltage range, parametrized by load. The output voltage is regulated at 32.4 V.

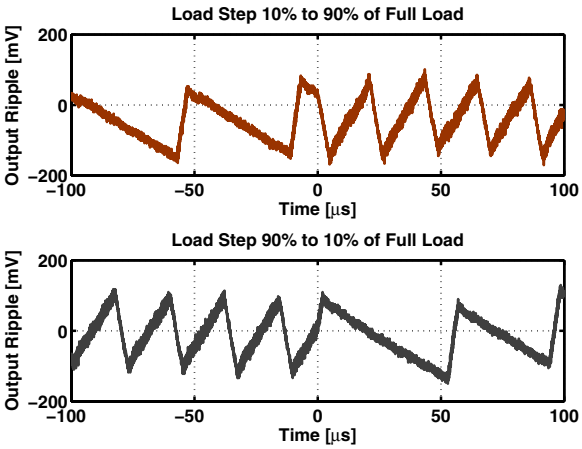

Fig. 10. Output voltage ripple of the 110 MHz for load steps between 10 and 90% of full load.

itself is operating at 110 MHz frequency when it is turned on. In the time scale of Figure 8 this switching frequency is under-sampled, but its effect can be seen as the "hash" in the rising portion of the output voltage ripple and the drain voltage when the converter is turned on.

An important benefit of the on-off control strategy is the high efficiency at light load. Figure 9 shows the closed-loop efficiency over the input voltage range, parameterized by load. The converter regulates the output at 32.2 V and the load is varied from 5-90% of full load[2]. As Figure 9 illustrates, the converter exhibits excellent light-load performance, maintaining above 81% efficiency at nominal input voltage all the way down to 5% load. This substantial improvement in light load operation compared to typical resonant converters can be attributed to the control strategy used, which turns the converter on only for very small periods of time at light load. When the converter is turned off, it consumes no power, and for the brief time when it is turned on, it operates in a highly efficient state. There is quiescent loss in the control circuitry along with a small fixed power loss associated with turning the converter on and off, which explains why overall efficiency still decreases with lighter load. As the delivered power is reduced, the fixed on-off power loss becomes a larger fraction of the total output power, thereby reducing efficiency.

In addition to the size, weight, and cost benefits realized from smaller passive components, an increase in switching frequency also leads to improved transient performance. Because of the small amount of energy stored in the passive components in each switching cycle, the converter can quickly adjust to any changes in load conditions. To illustrate this, Figure 10 shows the measured output voltage ripple when the load is changed from 10 to 90% of full load (top), and from 90 to 10% of full load (bottom) at time t = 0. It can be seen from this figure that there is an instantaneous response to the load step transient, without any voltage deviation outside the ripple range. This formidable transient response can be attributed to the small inductors and capacitors required for operation at 110 MHz. In addition, transient performance is improved by the resonant topology introduced in Section II, which uses only small-valued resonant passive components.

In conventional dc-dc converters, the total required output capacitance is determined by the allowed voltage ripple and the desired transient performance. It is often the latter requirement that determines the minimum capacitance, calling for a larger capacitance than what output ripple requirements alone would require. The VHF resonant boost converter, with its inherently fast transient response, does not have this problem. The output capacitor is sized solely based on the desired on-off modulation frequency and output ripple, not by transient response limitations.

B. 50 MHz Integrated Power Process Implementation

The VHF operation of the converter described here lends itself to the possibility of integration. With this in mind a

[2]For this measurement, full load is defined as the maximum power that the converter can deliver at an input voltage of 11 V, while still regulating the output voltage. Using this definition, 90% of full load corresponds to 16.3 W, and 5% to 0.9 W.

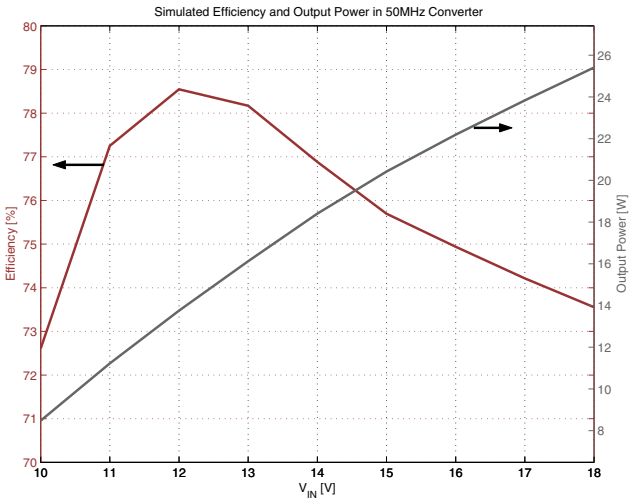

Fig. 11. Open loop power and efficiency vs. input voltage of the 50 MHz power stage for a fixed output voltage of 32 V.

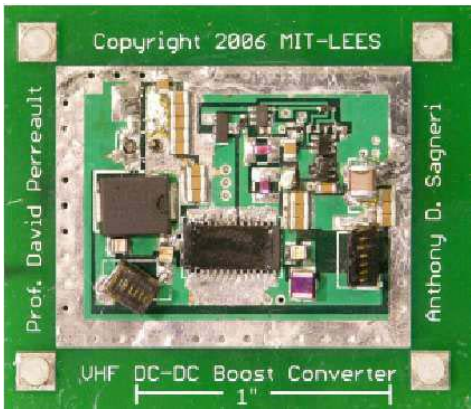

Fig. 12. Photograph of the 50 MHz resonant boost converter prototype.

converter was built where the main switch was fabricated in a 50 V integrated power process and the other components were discrete. The device was not optimized for rf operation or otherwise customized. Instead, the goal was to determine the feasibility of implementing the design in conventional power processes thereby avoiding the cost of a custom rf process. The converter was designed for an 8-18 V input range, a 22-33 V output range, and had a 17 W output power rating at the nominal input voltage of 14.4 V. Figure 11 shows (open loop) power and efficiency vs. input voltage for an output voltage of 32 V. The switching frequency was 50 MHz which held the largest inductor value to 56 nH (a complete list of component values appears in Table III). The small value, air-core passive components are promising candidates to be either co-packaged with a switch/controller IC or perhaps realized on-die. Figure 12 shows a photograph of the 50 MHz converter.

Figure 13 shows the device drain and gate waveforms of the 50 MHz converter. The ability to tune the resonant boost converter to minimize peak switch voltage stress was a key factor enabling the use of the 50 V power process. The peak V_{DS} across the switch was 42 V at 18 V input ($< 2.4\ V_{in}$).

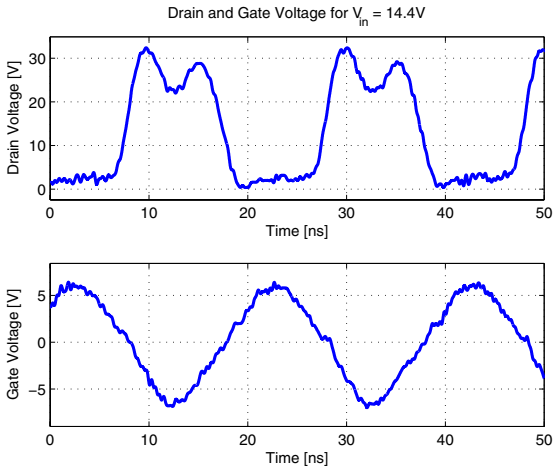

Fig. 13. Drain and gate voltage for experimental 50 MHz converter operating with V_{in} = 14.4 V and V_{out} = 32 V.

This is in contrast to the 65 V peak a class E converter would suffer—well beyond the 50 V process breakdown.

At the nominal input voltage the converter was better than 74% efficient over a load range from 4-17 W under closed-loop operation. A significant fraction of the increased loss over the high performance design is related to the integrated device. It's gate-drive figure of merit ($R_{gate} \cdot C_{gate}^2$) is nearly 80 fold poorer than the rf device. Similarly a larger C_{OSS} and its greater equivalent series resistance contributes to increased device loss along with higher conduction loss owing to the somewhat larger 210 $m\Omega$ R_{DS-on}. Since it was not possible to custom-design the device layout on this iteration, there is room for performance enhancement by simple changes in device geometry, such as choosing a more optimum gate finger length. As a minimum this will reduce gate resistance allowing an increase in operating frequency or greater device area and lower total loss. The detailed efficiency characteristics of the converter are qualitatively similar to those of the 110 MHz converter.

As a consequence of the small energy storage, the transient performance is excellent and the converter can be modulated at 700 kHz with only a 1% loss of efficiency. Under closed-loop operation, the modulation frequency was held to 250 kHz because of a larger than necessary 40 μF bulk capacitance.

This converter has a 100 mV_{p-p} ripple using the hysteretic voltage mode control scheme described above. Load step performance is excellent. The application of a load step from 2 W to 12 W back to 2 W (corresponding to 13.3% load and 80% load) results in a transient response that never leaves the ripple band. That is, under load step, the output voltage is never more than 50 mV away from the reference voltage. This is illustrated in Figure 14.

Additional detail about this design may be found in [21]. The overall good performance achieved with the integrated transistor is encouraging. Plenty of opportunity exists to optimize the device within the constraints of the process and perhaps realize higher efficiency, higher operating frequency, or both.

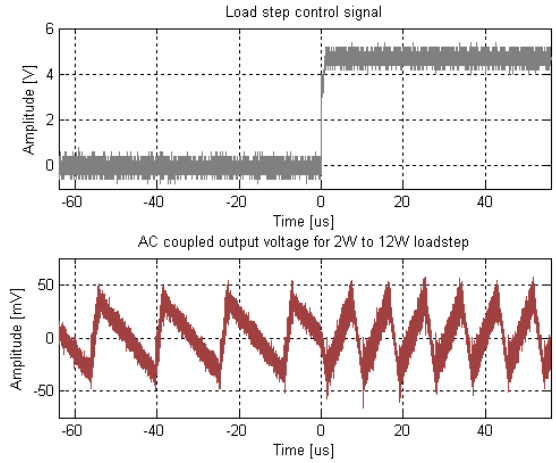

Fig. 14. Transient performance of the 50 MHz converter when the load is stepped from 2W to 12W. The converter output remains within the ripple band.

VI. Conclusion

This document presents a new resonant topology suitable for boost power conversion. The new topology addresses several shortcomings of previous designs, while maintaining all desirable properties necessary for very high frequency power conversion, such as zero voltage switching and absorption of device capacitance.

The paper describes experimental implementations of two resonant boost converters. One is a 110 MHz, 23 W converter using a commercially available LDMOSFET, which achieves efficiency above 87% for nominal input and output voltages. The other is a 50 MHz, 17 W converter using a switch from a standard 50 V integrated power process. Both converters utilize a high-bandwidth control strategy that permits excellent light load efficiency, something that is typically difficult to implement with resonant converters. In addition to greatly reducing the physical sizes of the passive components, the high operating frequency gives the converters an inherently fast transient response.

As this paper has demonstrated, it is possible to achieve miniaturization and high performance of dc-dc power converters without sacrificing efficiency. The design implementations described in this paper are expected to contribute to the development of VHF dc-dc converters, paving the way for power electronics that can satisfy the needs for improved size, cost, and performance that are demanded by modern applications.

References

[1] R. Gutmann, "Application of RF circuit design principles to distributed power converters," *IEEE Transactions on Industrial Electronics and Control Instrumentation*, vol. IEC127, no. 3, pp. 156–164, 1980.

[2] R. Redl, B. Molnar, and N. Sokal, "Class E resonant regulated dc/dc power converters: Analysis of operations and experimental results at 1.5 MHz," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 2, pp. 111–120, April 1986.

[3] R. Redl and N. Sokal, "A 14 MHz 100 Watt class E resonant converter: Principles, design considerations, and measured performance," in *17^{th} Annual IEEE Power Electronics Specialists Conference Proceedings*, pp. 68–77, June 1986.

[4] F. Lee, "High-frequency quasi-resonant converter technologies," in *Proceedings of the IEEE*, vol. 76, pp. 377–390, April 1988.

[5] W. Bowman, J. Balicki, F. Dickens, R. Honeycutt, W. Nitz, W. Strauss, W. Suiter, and N. Zeisse, "A resonant dc-to-dc converter operating at 22 megahertz," in *Third Annual Applied Power Electronics Conference Proceedings*, pp. 3–11, 1988.

[6] W. Tabisz and F. Lee, "Zero-voltage-switching multiresonant technique-a novel approach to improve performance of high-frequency quasi-resonant converters," *IEEE Transactions on Power Electronics*, vol. 4, pp. 450–458, Oct. 1989.

[7] R. Redl and N. Sokal, "A new class-e dc/dc converter family with reduced parts count: Derivation, topologies, and design considerations," in *Technical Papers of the Fourth International High Frequency Power Conversion Conference*, pp. 395–415, 1989.

[8] J. Jozwik and M. Kazimierczuk, "Analysis and design of class-e dc/dc converter," *IEEE Transactions on Industrial Electronics*, vol. 37, pp. 173–183, April 1990.

[9] H. Koizumi, I. M., and M. S., "Class e^2 dc/dc converter with second harmonic resonant class e inverter and class e rectifier," in *Third Annual Applied Power Electronics Conference Proceedings*, pp. 1012–1018, 1994.

[10] S. Mollov and A. Forsyth, "Design and evaluation of a multi-resonant buck converter at 15 mhz," in *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (IEE Conf. Publ. No. 456)*, pp. 139–144, 21-23 Sept. 1998.

[11] J. Rivas, J. Shafran, R. Wahby, and D. Perreault, "New architectures for radio-frequency dc/dc power conversion," in *35^{th} Annual IEEE Power Electronics Specialists Conference Proceedings*, pp. 4074–4084, June 2004.

[12] J. Rivas, D. Jackson, O. Leitermann, A. Sagneri, Y. Han, and D. Perreault, "Design considerations for very high frequency dc-dc converters," in *37th Annual IEEE Power Electronics Specialists Conference Proceedings*, pp. 1–11, 18-22 June 2006.

[13] Y. Lee and Y. Cheng, "A 580 khz switching regulator using on-off control," *Journal of the Institution of Electronic and Radio Engineers*, vol. 57, no. 5, pp. 221–226, September/October 1987.

[14] J. Phinney, J. Lang, and D. Perreault, "Multi-resonant microfabricated inductors and transformers," in *35^{th} Annual Power Electronics Specialists Conference Proceedings*, pp. 4527–4536, June 2004.

[15] J. Phinney, D. Perreault, and J. Lang, "Radio-frequency inverters with transmission-line input networks," in *37th Annual IEEE Power Electronics Specialists Conference*, pp. 1–9, 18-22 June 2006.

[16] J. W. Phinney, *Multi-resonant Passive Components for Power Conversion*. Ph.D. Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., June 2005.

[17] J. M. Rivas, *Radio Frequency dc-dc Power Conversion*. PhD thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, September 2006.

[18] J. M. Rivas, Y. Han, O. Lietermann, A. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low voltage stress," in *Power Electronics Specialist Conference Proceedings 2007*, June 2007. in press.

[19] W. Nitz, W. Bowman, F. Dickens, F. Magalhaes, W. Strauss, W. Suiter, and N. Zeisse, "A new family of resonant rectifier circuits for high frequency DC-DC converter applications," in *Third Annual Applied Power Electronics Conference Proceedings*, pp. 12–22, 1988.

[20] S. Birca-Galateanu and J.-L. Cocquerelle, "Class e half-wave low dv/dt rectifier operating in a range of frequencies around resonance," *IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications*, vol. Vol. 42, No. 2, February 1995.

[21] A. D. Sagneri, "The design of a very high frequency dc-dc boost converter," Master's thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, February 2007.

[22] J. Warren III, "Cell-modulated resonant dc/dc power converter," Master's thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, August 2005.

[23] J. R. Warren III, K. A. Rosowski, and D. J. Perreault, "Transistor selection and design of a VHF dc-dc power converter," in *IEEE Transactions on Power Electronics*. in press.

[24] R. C. Pilawa-Podgurski, "Design and evaluation of a very high frequency dc/dc converter," Master's thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, February 2007.