Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer

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***Abstract*—This paper presents a two-stage architecture that combines a large step-down switched-capacitor transformation stage with a high-bandwidth magnetic regulation stage. The proposed design is particularly well-suited for an integrated CMOS process, as it makes use of the available on-die device characteristics. In such a process, the two-stage architecture presented offers high efficiency, high power density, and high-bandwidth regulation.**

We show that by merging the switched-capacitor stage and the regulation stage in a specific manner, further performance improvements can be attained. When the fast-switching regulation stage is used to provide *soft charging* of the switched-capacitor stage, a substantial improvement in performance is possible. An experimental prototype, implemented using discrete components, validates the approach.

***Index Terms*—switched capacitor circuits, two-stage architectures, soft charging, dc-dc converters, charge pumps, voltage regulator module.**

I. Introduction

THE advent of low-voltage digital circuitry has created a need for improved dc-dc converters. Dc-dc converters that can provide a low-voltage output (< 2 V) regulated at high bandwidth, while drawing energy from a higher (5-12 V) input voltage are desirable. In addition, the size, cost, and performance benefits of integration make it advantageous to integrate as much of the dc-dc converter as possible, including control circuits and power switches. Moreover, it would be desirable - if possible - to integrate the power converter or portions thereof with the load electronics.

One common approach is the use of a switched-mode power converter (e.g. synchronous buck converter, interleaved synchronous buck, three-level buck, and like designs [1]–[8]). For magnetics-based designs operating at low, narrow-range input voltages, it is possible to achieve extremely high switching frequencies (up to hundreds of MHz [3], [6], [7]), along with correspondingly high control bandwidths and small passive components (e.g., inductors and capacitors). It also becomes possible to integrate portions of the converter with a microprocessor load in some cases. These opportunities arise from the ability to use fast, low-voltage, process-compatible transistors in the power converter. However, at higher input voltages and wider input voltage ranges, much lower switching frequencies (on the order of a few MHz and below) are the norm, due to the need to use slow extended-voltage transistors (on die) or discrete high-voltage transistors. This results in much lower control bandwidth, and large, bulky passive components (especially magnetics) which are not suitable for integration or co-packaging with the devices.

Another conversion approach that has received attention for low-voltage electronics is the use of switched-capacitor (SC) based dc-dc converters [9]–[15]. This family of converters is well-suited for integration and/or co-packaging of passive components with semiconductor devices, because they do not require any magnetic devices (inductors or transformers). A SC circuit consists of a network of switches and capacitors, where the switches are turned on and off periodically to cycle the network through different topological states. Depending on the topology of the network and the number of switches and capacitors, efficient step-up or step-down power conversion can be achieved at different conversion ratios.

There are, however, certain limitations of the SC dc-dc converters that have prohibited their widespread use. Chief among these is the relatively poor output voltage regulation in the presence of varying input voltage. The efficiency of SC converters drops quickly as the conversion ratio moves away from the ideal (rational) ratio of a given topology and operating mode. In fact, in many topologies the output voltage can only be regulated for a narrow range of input voltages while maintaining an acceptable conversion efficiency [11], [12], [16].

One means to partially address these limitations is to cascade a SC converter having a fixed step-down ratio with a low-frequency switching power converter having a wide input voltage range [1] to provide efficient regulation of the output. Other techniques [17], [18] integrate a SC circuit within a buck or boost converter to achieve large conversion ratios. However, the regulation bandwidth of these techniques is still limited by the slow switching of the SC stage.

Another approach that has been employed is to use a SC topology that can provide efficient conversion for multiple specific conversion ratios (under different operating modes) and select the operating mode that gives the output voltage that is closest to the desired voltage for any given input voltage

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[12]. None of these approaches are entirely satisfactory in achieving the desired levels of performance and integration.

Section II presents a two-stage architecture that addresses the challenges outlined above. In Section III, a method to further improve efficiency and power density of this architecture is outlined, together with simulated results. Section IV presents experimental results from a prototype using discrete components, Section V concludes the paper.

II. Two-stage Architecture

Fig. 1 shows a block diagram of a two-stage converter that combines a high efficiency switched-capacitor transformation stage with a high-frequency, low-voltage regulation stage. This strategy makes use of on-die device characteristics available in CMOS processes. As examined in the appendix, low-voltage submicron CMOS processes inherently provide far higher achievable switching frequencies than higher-voltage processes. In a given process, one often has access to both slow, moderate-blocking-voltage devices and fast, low-voltage devices. The converter architecture of Fig. 1 is well-suited to the available devices in such a process: The SC transformation stage can achieve a large voltage step-down, and can be designed for very high power density and efficiency using slow, moderate-voltage devices at relatively low switching frequency. The unregulated voltage, V_{unreg} is low so that the regulating stage can utilize fast, low-voltage devices operating at a high switching frequency to provide high-bandwidth regulation and a small additional voltage step-down. Since the regulation stage operates at a high frequency, the size of its passive components can be made small. By separating the transformation and regulation stage in this manner, the benefits typically associated with SC converters (i.e. high efficiency, high power density) can be preserved, while the main drawback (poor regulation) is done away with by the use of a separate magnetic regulation stage. Furthermore, since the regulation stage only sees a very low voltage, it can operate at a much higher frequency and control bandwidth than a single, conventional switching power converter that needs to provide a large step-down in voltage.

It should also be noted that if a switched-capacitor stage capable of multiple conversion ratios (e.g. 1:1, 2:1, and 3:1) is utilized, one can dynamically change the conversion ratio of the transformation stage (e.g. as a function of input voltage). This enables such a system to function over a wide range of input voltages, while preserving a low and relatively narrow voltage range on the regulation stage.

III. Merged Two-stage Converter - Soft Charging

In addition to the benefits listed above, yet another advantage can be realized by a suitable implementation of the two-stage approach. To understand this concept, it is illustrative to first consider the fundamental tradeoffs in efficiency, capacitance, and frequency in a conventional switched-capacitor converter.

The circuit shown in Fig. 2 is a simple example which illustrates the loss mechanism for charging of the capacitors

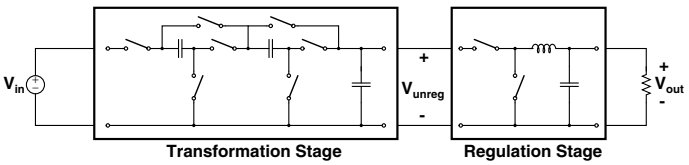
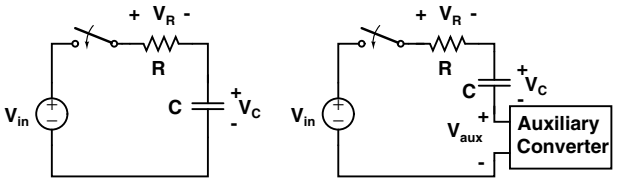


Fig. 1. Block diagram illustrating a two-stage converter. The transformation stage can be constructed using slow, high voltage devices and operated at a slow switching frequency, while the regulation stage can be constructed with fast, low-voltage devices and operated at a high switching frequency.



(a) Hard charging. (b) Soft charging.

Fig. 2. Capacitor charging in a switched capacitor system. (a) Hard charging in a conventional SC system. (b) Soft charging with energy recovery.

in the SC stage. Fig. 2(a) shows an example of the resistive charging process of a capacitor C (as in a conventional SC circuit), where the resistor R represents the combined ESR of the capacitor and switch on-state resistance. The capacitor has an initial charge of V_C, and the switch is closed at $t = 0$. After $t = 0^+$, the difference between voltage V_{in} and the capacitor voltage at each instance in time appears across the parasitic resistor R. If charging is allowed to continue for a sufficient period of time, the voltage across the capacitor will charge up to V_{in}, and the voltage across the resistor will become 0 V. The voltage across the resistor and the current through it results in a power loss during the charging phase of the capacitor which depends on the capacitance and the net charge on the capacitor. It is this loss which limits the efficiency of an SC converter.

It is important to note that this fixed charge-up loss cannot be reduced by employing switches with lower on-state resistance. A lower parasitic R will only result in larger peak currents of shorter duration, but the total power loss in each charge cycle will remain the same. Thus, for a conventional SC circuit, a fixed amount of charge-up energy loss proportional to $\frac{1}{2}C(V_{final}^2 - V_{initial}^2)$ will result at each switch interval, where V_{final} and $V_{initial}$ correspond to the final and initial values of the capacitor voltage. Consequently, conventional SC converters require either large capacitors or high switching frequencies to minimize $\Delta V = V_{final} - V_{initial}$ and achieve high efficiency and power levels [10], [19]. However, as is shown below, this tight dependence of efficiency on capacitance and switching frequency in the SC converter can be mitigated through the appropriate merging between the SC (transformation) stage and the regulating stage in our two-stage converter.

Fig. 2(b) illustrates the proposed method to improve the charge-up efficiency of the SC circuit. In this circuit, an auxiliary converter operating at a much higher switching frequency than the SC stage is used to reduce the energy loss

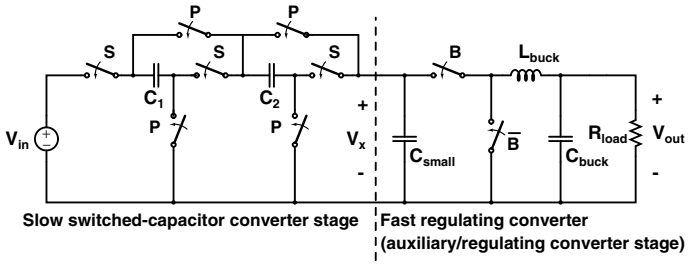


Fig. 3. Example of the switched-capacitor transformation stage circuit coupled with a fast regulating stage which provides soft charging of the switched-capacitor stage.

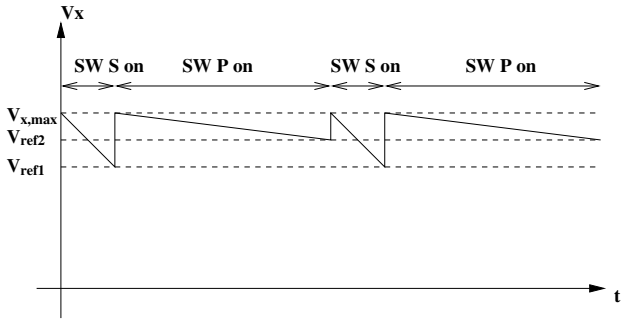


Fig. 4. Example of control strategy based on maximum input voltage of regulating converter.

associated with capacitor charging. The auxiliary converter may be the regulating converter used to supply the output, or it may be a separate converter. The system is designed such that the majority of the difference between the input voltage V_{in} and the capacitor stack voltage V_C appears across the input of the auxiliary converter when the capacitor is charging. Instead of being dissipated as heat in the resistor, the energy associated with charging the capacitor stack is delivered to the output of the auxiliary converter. By using an auxiliary converter to absorb the effective ΔV of the capacitor, the impulse-like charging current spikes typically associated with conventional SC converters is replaced with a smooth and steady charging current. We term this technique *soft charging*[1].

Fig. 3 illustrates how soft charging can be implemented in the two-stage converter. The fast regulating converter (in this case a synchronous buck converter) serves as both the auxiliary converter and the regulating converter stage for the system. It operates at a switching frequency much higher than that of the switched capacitor stage. As the capacitor C_{small} serves only as a filter and bypass for the fast regulating converter, its numerical value can be much smaller than the capacitors C_1 and C_2 of the SC stage.

When the SC stage is configured for charging of C_1 and C_2 (switches S closed), the difference between V_{in} and the sum of the voltages across capacitors C_1 and C_2 appears across the input terminal of the fast regulating converter. C_1 and C_2 thus charge with low loss (soft charging), and at a rate determined by the power drawn from the regulating converter to control the system output. Likewise, when the SC stage is configured for discharging C_1 and C_2 in parallel (switches P closed), the discharge is at a rate based on the power needed to regulate the output.

In operating the system, the SC stage can be controlled to provide a specified maximum voltage V_X at the input of the regulating converter. Fig. 4 illustrates a control strategy utilizing this technique, where two separate reference voltages are used to ensure that the input voltage of the auxiliary converter does not exceed $V_{X,max}$. The reference voltages can be expressed in terms of $V_{X,max}$ and V_{IN}:

[1]Likewise, we will use the term *hard charging* to denote a SC converter operating in a conventional manner.

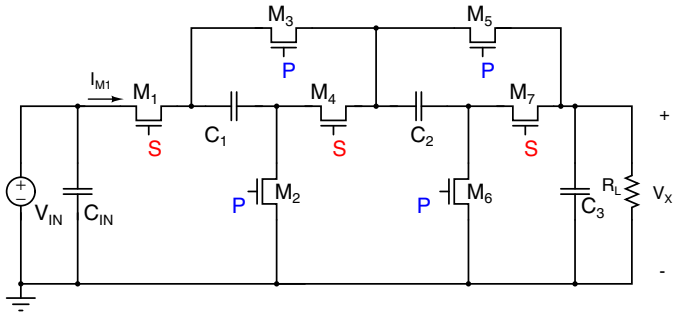


Fig. 5. Schematic diagram of simulation setup.

$$V_{ref1} = V_{IN} - 2V_{X,max} \quad (1)$$

$$V_{ref2} = \frac{V_{IN} - V_{X,max}}{2} \quad (2)$$

In this example, the switches S of Fig. 3 are on (series charging of the capacitors) until V_X falls below V_{ref1}. At this time, switches S turn off, and switches P turn on (parallel discharging of capacitors), until V_X falls below V_{ref2}, at which time the cycle repeats.

A. Simulated Switched-Capacitor Results

To investigate the promise of the soft charging strategy, a 2 W, 3-to-1 switched-capacitor stage was simulated in SPICE, using device characteristics from a 90 nm CMOS process and discrete capacitors. In the analysis presented here, only the performance of the switched-capacitor stage is considered. Fig. 5 shows a schematic diagram of the simulated circuit, which consists of a a 3-to-1 stepdown SC stage with a resistive load. The input voltage is 5.5 V, R_{load}=1.68 Ω, and the switching frequency is 1 MHz. In a full two-stage converter, a regulating converter (switching at a frequency much higher than 1 MHz) would replace the load resistor.

For hard charging operation, capacitors $C_1 - C_3$ are all 10 μF, while for soft charging operation C_1 and C_2 are 1.5μF each, and C_3 is 0.01 μF. Table I presents one metric of the improvement offered by the merged two-stage converter. Listed is the required capacitance for a 98% efficient transformation stage, for both a conventional (hard charging) SC converter and one implementing the soft charging technique. For the

TABLE I
CAPACITANCE REQUIREMENTS FOR TWO-STAGE CONVERTER

Converter	Hard Charging	Soft Charging
Total Capacitance	30 μF	3 μF (10%)
Total Capacitor Volume	3.072 mm^3	0.5 mm^3 (16%)
Total Capacitor Area	3.84 mm^2	1 mm^2 (26%)
Discrete Capacitor Sizes	3 x 0603	2 x 0402

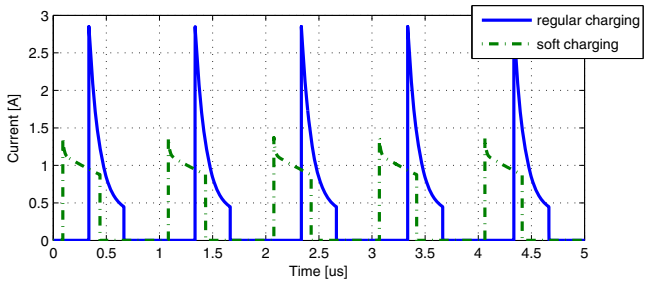


Fig. 6. Simulated current waveforms (I_{M1} of Fig. 5) for the SC converter stage, illustrating reduced peak currents (and, correspondingly, reduced loss) for the soft charging case.

same efficiency, the soft charging implementation enables a 10x reduction in required capacitance compared to hard charging transformation stage. If total capacitance is instead kept constant in the comparison, overall efficiency gains can be realized using the soft charging technique.

The soft charging characteristics of the merged two-stage converter is best illustrated by the waveform of the switch current. In a conventional SC converter, this current will have a large, exponentially decaying peak on top of a steady-state charging current. This peak corresponds to capacitor charging loss, which can be a substantial part of the overall converter loss. Fig. 6 shows the switch current (I_{M1} of Fig. 5) for a conventional SC converter, and that for a converter utilizing the soft charging techniques. As is evident from the figure, the soft charging technique enables a drastic reduction in peak and rms switch current and the associated loss. The output voltage of the SC stage (V_X of Fig. 5) is shown in Fig. 7. The substantially larger voltage ripple associated with the soft charging technique is evident from the two waveforms. This would be undesirable in a SC converter operating as a single stage (whose output voltage is the system output voltage), but in the merged two-stage topology this voltage merely corresponds to an input voltage to the regulating converter that changes slowly (compared to the switching frequency of the regulating converter). The regulating stage is designed to provide a steady output voltage despite a time-varying input voltage such as that shown in Fig. 7.

IV. EXPERIMENTAL RESULTS

A. Discrete Prototype Implementation

In order to verify the validity of the two-stage strategy, an experimental prototype was designed. It should be noted that while the ultimate target platform of the proposed converter is a low-voltage integrated process, this initial prototype is

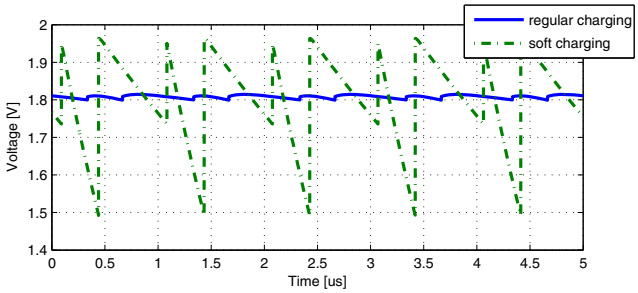


Fig. 7. Simulated output voltage waveforms (V_X of Fig. 5) for the SC converter stage, illustrating increased voltage ripple for the soft charging case.

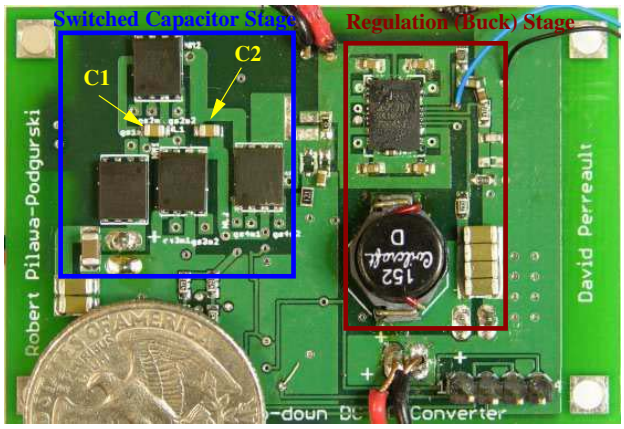


Fig. 8. Photograph of experimental prototype with switched-capacitor stage and regulation stage outlined. U.S. quarter shown for scale.

not implemented in such a process, and thus does not achieve the design scaling and power density that is expected to be possible. The purpose of this discrete prototype is purely to validate the concept and provide design insights for future designs based on integrated processes.

Fig. 8 shows a photograph of the prototype converter, which consists of a 3-to-1 switched-capacitor stage coupled with a commercial synchronous buck converter (LTC3418). The SC stage is controlled in the manner described in Fig. 4 using a microcontroller (ATtiny24) with a built-in comparator to sense the different thresholds, and to provide the logic signals for the gate drive chips. These components are placed on the backside of the board (not shown). A schematic drawing of the converter is shown in Fig. 9, and component values are listed in Table II. The relatively large values of C_{IN} and C_{OUT} are used to ensure steady input and output voltages for more precise efficiency measurements. Resistors R_1-R_4 are used to set the reference voltages V_{ref1} and V_{ref2} (Fig. 4) which determine the discharge level of the capacitors.

The floating high-side gate drive chips are powered from the energy stored on the capacitors C_1 and C_2, while the low-side gate drive chips and the microcontroller are powered from a separate, low-voltage supply. In addition to implementing the control strategy, the microcontroller initiates the startup sequence, which coordinates the turn-on of the SC switches to provide power to the gate drive chips, and to ensure that

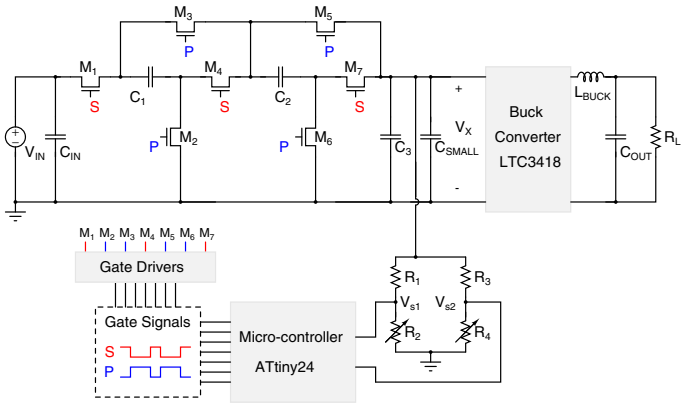


Fig. 9. Schematic of experimental prototype. The microcontroller samples the output voltage through the voltage dividers, and alternates the SC stage between parallel and series configuration.

TABLE II
COMPONENT VALUES FOR PROTOTYPE CONVERTER

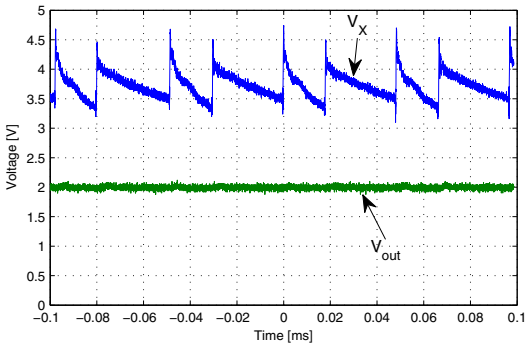
Component	Value
C_{IN}	5x22 μF 1x2200 μF
M_1-M_7	Si7236DP
C_1	10 μF
C_2	10 μF
C_3 hard charging soft charging	10 μF 1 μF
C_{SMALL}	4x0.1 μF
L_{BUCK}	1.5 μH
C_{OUT}	1x100 μF 1x2200 μF
R_1 & R_2	47 kΩ
R_3 & R_4	0-50 kΩ
Gate Drive (high side)	LTC4440-5
Gate Drive (M_2 & M_6)	LM5111

the output voltage of this stage (V_X) stays below its allowed maximum value. The synchronous buck converter, LTC3418 from Linear Technology, is set to operate at a switching frequency of 1 MHz, and an output voltage of 2 V.

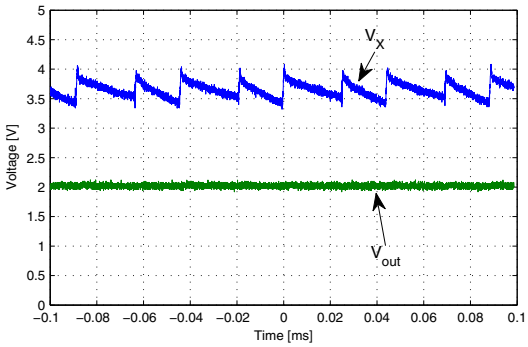
B. Hard and Soft Charging Comparison

To evaluate the merits of soft charging operation in the merged two-stage converter architecture, we compare it to traditional hard charging operation. By placing capacitor C_3 in the circuit of Fig. 9 that is the same size as C_1 and C_2 (10 μF), the SC stage implements regular hard charging operation. For soft charging operation, C_3 instead consists of a small capacitor (1 μF) to filter the 1 MHz input current ripple of the LTC3418.

Fig. 10 shows the measured input and output voltage of the buck converter (corresponding to V_X in Fig. 3), for V_{IN}=12 V, V_{OUT}=2 V, and I_{OUT}=0.4 A for soft and hard charging operation. The switching of the SC stage can be clearly seen in the V_X waveform, with alternating series charging and parallel discharging of the capacitors. Since the switching frequency of the buck converter is much higher (1 MHz) than the frequency of the SC stage (~20 kHz for this load), V_{OUT} can be well regulated with small ripple despite the



(a) Soft Charging.

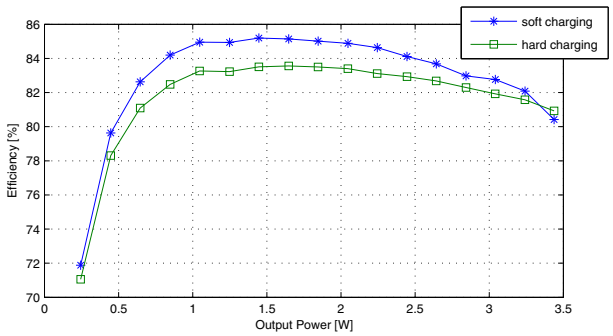


(b) Hard Charging.

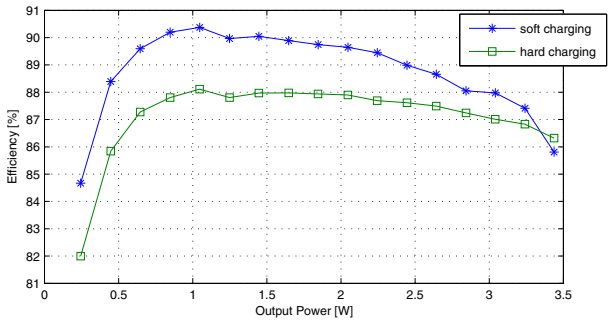
Fig. 10. Measured input and output voltage of the buck converter in the experimental prototype for soft and hard charging implementation.

large ripple seen at V_X, as illustrated by the V_{out} waveforms. Fig. 10 also illustrates the larger ripple of V_X for soft charging compared to hard charging, which is consistent with our earlier discussion. Note that in the case presented in Fig. 10, C_1 and C_2 have the same values for both soft and hard charging operation, and the frequencies of the two modes of operation are made to be approximately equal. In contrast, the simulated waveforms shown in Fig. 7 shows the case where C_1 and C_2 are drastically smaller in the soft charging case while overall efficiency is the parameter that is kept constant for the two modes of operation. Consequently, the voltage ripple is significantly larger for soft charging compared to hard charging in Fig. 7.

In addition to decreased capacitance requirement and reduced current spikes, efficiency improvement is a key benefit of soft charging operation. To estimate the efficiency gains realized by soft charging operation in the discrete implementation presented here, a comparison to hard charging operation was made over a wide load range. It is important to note that the objective of the discrete prototype presented here is not to obtain the highest efficiency achievable, but rather to investigate the feasibility of the soft charging architecture for cases where total capacitance is limited. Thus, absolute measures of efficiency is not the metric with which to evaluate



(a) Measured Overall Converter Efficiency.



(b) Estimated SC Efficiency.

Fig. 11. Efficiency measurements for discrete prototype converter for soft and hard charging operation.

the proposed converter, but rather the relative improvements offered by soft charging.[2]

The resulting efficiency measurements shown in Fig. 11 illustrate the efficiency improvements offered by the soft charging implementation. The efficiency of the SC stage alone is estimated by measuring the efficiency of the buck converter across the load range, and subtracting its loss from the overall converter loss. The resulting estimated SC stage efficiency is shown in Fig. 11(b). It is clear from this plot that soft charging offers a noticeable improvement in efficiency. At 1 W load, the estimated power loss in the SC stage is 25% higher for hard charging than for soft charging.

V. Conclusion

We have presented a two-stage dc-dc converter architecture in which a switched-capacitor transformation stage and a fast, magnetic regulation stage are utilized to achieve both large voltage step-down and high-bandwidth regulation. The transformation stage provides a significant voltage step-down, while the regulation stage provides high-bandwidth control. This architecture is particularly suitable for an integrated design where one has access to both slow devices that can block large voltages, and fast, low-voltage devices. The dramatic increase in achievable switching frequncy at reduced CMOS device voltages (as examined in the appendix) makes this approach advantageous.

[2]Absolute efficiency can, in this case, be improved by utilizing larger energy transfer capacitors ($C_1 - C_3$).

We also show that through the proper merging of the two stages, *soft charging* of the switched-capacitor stage can be achieved. Soft charging enables more efficient operation of the SC stage and/or a drastic reduction in the required capacitive energy storage compared to a conventional, hard charged converter. We have validated this approach with experimental measurements of a merged two-stage, soft-charging converter prototype.

Appendix
CMOS Scaling for Power Conversion

In this appendix we explore how the achievable switching frequency of dc-dc converters in deep sub-micron CMOS processes scale with process voltage. For simplicity, we focus on CMOS synchronous buck converters. First, consider how the required device length (L), oxide thickness (t_{OX}), channel resistivity (ρ_{CH}), and channel depth (t_{CH}) vary with device blocking voltage (V_{SW}). If one assumes constant electric field scaling, then $L \propto V_{SW}$, $\rho_{CH} \propto 1$, $t_{OX} \propto V_{SW}$, $t_{CH} \propto 1$ and we find the following

$$C_g = \frac{\varepsilon_{OX}}{t_{OX}} A_g = \frac{\varepsilon_{OX}}{t_{OX}} LW \Rightarrow C_g \propto W \,, \tag{3}$$

$$R_{on} = \frac{\rho_{CH} L}{A_g} = \frac{\rho_{CH}}{t_{CH}} \left(\frac{L}{W}\right) \Rightarrow R_{on} \propto \frac{V_{SW}}{W} \,, \tag{4}$$

$$R_{on} C_g \propto V_{SW} \,. \tag{5}$$

Where R_{on} is the device on-resistance, C_g is the gate capacitance, and W is the device width. The $R_{on}C_g$ produce is ideally proportional to blocking voltage under this model. The $R_{on}C_{g,eff}$ product is shown vs supply voltage in Fig. 12 and Fig. 13 for NMOS and PMOS devices in various processes. In these plots, the effective capacitance ($C_{g,eff}$) is the combination of the gate capacitance (C_g), fringing capacitance, and Miller capacitance. Typically, the gate capacitance is dominant contributor to dynamic loss in low-voltage CMOS processes. All of these devices are minimum feature size and available in commercial foundries. It can be seen that in fact the $R_{on}C_{g,eff}$ product is proportional to supply voltage as eqn. (5) predicts. There is some deviation from the linear fit and this may be due to the fact that the devices are not scaled with a constant electric field, and in some cases may also be derated due to hot carrier effects.

Now consider how this device scaling characteristic influences converter performance. As shown in [20] the MOSFET losses in a synchronous buck converter can be modeled using an effective bridge capacitance (C_b) and an effective bridge resistance (R_b), as illustrated in Fig. 14. The converter is composed of a low-side switch (S_L) and a high-side switch (S_H) where W_L, W_H, C_{L0}, C_{H0}, R_{L0}, R_{H0} are the widths, effective capacitances and on-resistances of the MOSFETs. Defining:

$$D = \frac{V_{OUT}}{V_{IN}} \,, \tag{6}$$

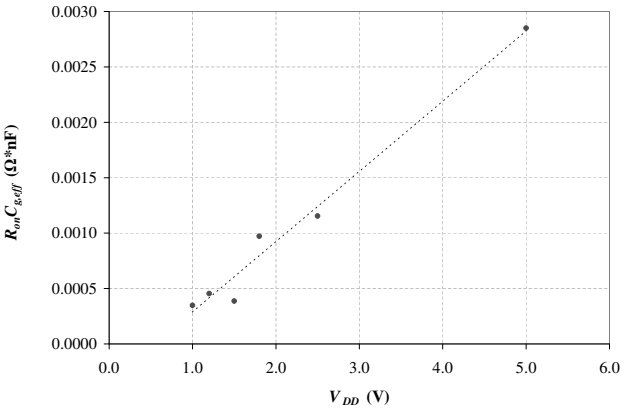


Fig. 12. $R_{on}C_{g,eff}$ vs. Supply Voltage (V_{DD}) for NMOS

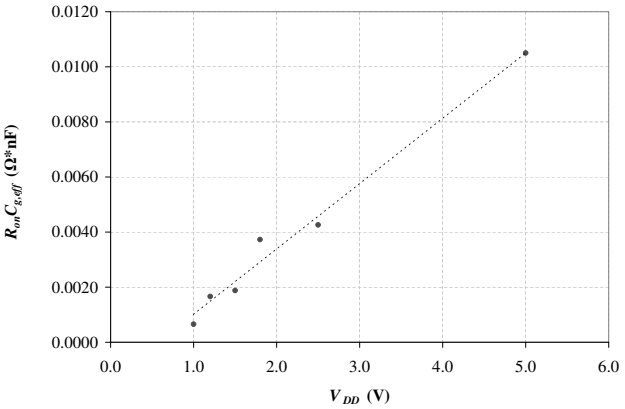


Fig. 13. $R_{on}C_{g,eff}$ vs. Supply Voltage V_{DD} for PMOS

$$C_b = W_L C_{L0} + W_H C_{H0}\,, \tag{7}$$

$$R_b = \frac{R_{L0}}{W_L}(1-D) + \frac{R_{H0}}{W_H}D\,. \tag{8}$$

The optimal width ratio of the high-side device width to the low-side device width (α) [20] can be found by a constrained minimization of C_b at a constant R_b, yielding

$$\alpha = \frac{W_H}{W_L} = \sqrt{\frac{DR_{H0}C_{L0}}{(1-D)R_{L0}C_{H0}}}\,. \tag{9}$$

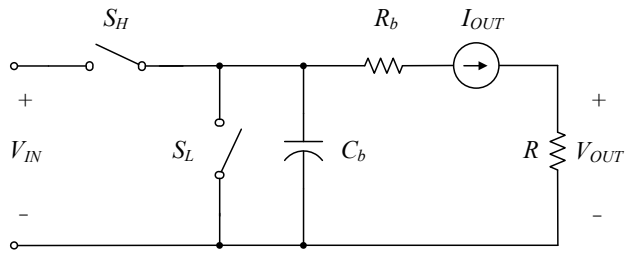


Fig. 14. Buck Converter Model

The total power loss is a combination of the static loss (P_{res}) and switching loss (P_{cap});

$$P_{loss} = P_{cap} + P_{res} = W_b C_0 V_{IN}^2 f_S + \frac{R_0}{W_b} I_{OUT}^2 \tag{10}$$

where

$$C_0 = \frac{C_b}{W_b} = \frac{C_{L0} + C_{H0}\alpha}{1+\alpha} \tag{11}$$

and

$$R_0 = R_b W_b = (1+\alpha)\left[(1-D)R_{R0} + \frac{DR_{H0}}{\alpha}\right]\,. \tag{12}$$

assuming that the power loss is only in the MOSFETs. The optimal bridge width (W_{opt}) can be found by minimizing P_{loss} (eqn. 10) and is

$$W_{opt} = \frac{I_{OUT}}{V_{IN}}\sqrt{\frac{R_0}{C_0 f_S}} \tag{13}$$

while the minimum power loss is

$$P_{min} = 2W_{opt}C_0 V_{IN}^2 f_S = 2I_{OUT}V_{IN}\sqrt{R_0 C_0 f_S}\,. \tag{14}$$

An optimal switching frequency (f_{opt}) can be chosen given a desired power loss (P_{min}) or equivalently, a desired efficiency. This optimum is

$$f_{opt} = \frac{P_{loss(min)}^2}{4I_{OUT}^2 V_{IN}^2 R_0 C_0}\,. \tag{15}$$

Additionally, by combining eqn. (6), (9), (11), (12), (15), holding I_{OUT} and P_{min} constant, and assuming $R_{H0}C_{H0} \propto V_{IN}$ and $R_{L0}C_{L0} \propto V_{IN}$ (in line with eqn. 5), it can be shown that the optimal switching frequency is

$$f_{opt} \propto \frac{\Gamma}{V_{IN}^2\left(V_{IN}\Gamma - V_{OUT}\Gamma + V_{OUT}b\right)(1+\Gamma)} \tag{16}$$

where

$$b = \frac{R_{H0}C_{H0}}{R_{L0}C_{L0}}\,, \tag{17}$$

$$\Gamma = \sqrt{\frac{V_{OUT}b}{V_{IN}-V_{OUT}}}\,. \tag{18}$$

In eqn. 17, b represents a relative performance factor for high-side and low-side devices. If both high-side and low-side devices exhibit the same RC product (e.g. are both NMOS) then b = 1. If, more typically, the high-side device is a PMOS and the low-side device is a NMOS, a b value closer to 3 might be found for a given process. Furthermore, it can be shown empirically that if β and α are both functions of b and V_{OUT} given $V_{IN} > 2V_{OUT}$ then the optimal switching frequency (f_{opt}) fits a power law

$$f_{opt} = \alpha V_{IN}^{\beta}\,. \tag{19}$$

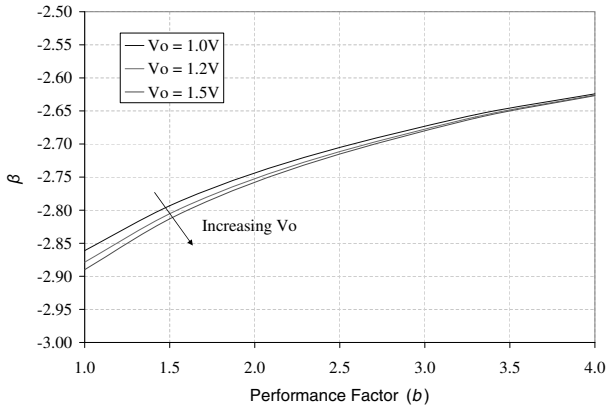


Fig. 15. Exponent β vs relative performance factor (b)

Fig. 15 shows how exponent β varies as a function of device performance factor (b) for various output voltages.

What may be concluded from eqn. 19 and Fig. 15 is that the optimal switching frequency (f_{opt}) increases very rapidly with decreasing input voltage. For example, if $b = 3$ and $V_{OUT} = 1V$ then $\beta = -2.67$. Therefore a buck converter with an input voltage of $1.8V$ should be able to switch 15.3 times faster than a buck converter with an input voltage of $5V$ with equal power loss in the MOSFETs. This leads to less energy storage in the filter elements (L and C) for a given dynamic and static response.

While this analysis does not include all salient loss mechanisms, it nevertheless points to the dramatic frequency capabilities of low-voltage CMOS processes. These capabilities are increasingly reflected in the literature. Recently several high frequency ($>$ 100 MHz) low-voltage dc-dc converters have been demonstrated in deep sub-micron CMOS [3], [6], [20], [21]. The switching frequencies of these converters are roughly 1 to 2 orders of magnitude higher than commercial products. This can be attributed to their use of deep sub-micron CMOS.

For our purposes, we may conclude that separating a design into two stages as proposed here has substantial potential advantages owing to the described scaling characteristics of CMOS.

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