Design and Evaluation of a Cellular Rectifier System with Distributed Control

David J. Perreault John G. Kassakian

Massachusetts Institute of Technology
Laboratory for Electromagnetic and Electronic Systems
Cambridge, MA 02139 USA

Abstract - **This paper presents the design and experimental evaluation of a six-cell, six-kilowatt cellular (parallel) rectifier system which operates at nearly unity power factor. The parallel power converter system implements both distributed load sharing and distributed ripple cancellation, eliminating the need for any centralized control. The implemented system mitigates some of the major drawbacks of its single-converter counterpart, and achieves performance levels that cannot be attained with an equivalent single converter.**

I. INTRODUCTION

One approach to constructing a large power converter such as a switched-mode rectifier is the use of a cellular converter architecture, in which many quasi-autonomous power converters, called *cells*, are paralleled to form the equivalent of a single large converter [1-3]. The cell power rating is selected such that the cells can be constructed using inexpensive high-volume components, and fabricated using automated manufacturing techniques. The use of quasi-autonomous cells means that system operation is not compromised in the event of the failure of a cell.

The cellular architecture has several potential advantages over conventional methods of constructing power converter systems, including performance, reliability, and cost [2]. Performance advantages arise from the ability to achieve a high degree of ripple cancellation among the cells, and also from reductions in the power stage interconnection parasitics. Reliability advantages come from the ability to employ the natural redundancy of a parallel converter system, as well as from the use of highly reliable automated manufacturing and test procedures. The cellular architecture does have some cost liabilities due to the fact that some components, such as sensing and control elements, must be replicated among cells. However, there are also some cost benefits to the approach, including the reduction of labor costs due to the use of automated manufacturing techniques, and the simplification of the thermal management system which is possible due to the distribution of heat generation. Through proper design, it should be possible to achieve cost parity or even a net cost benefit using a cellular architecture.

To fully realize these advantages, however, it is necessary to develop appropriate design and control methodologies and experimentally establish their viability at a reasonable power level. While the cellular architecture is well suited to many power conversion functions, it is particularly advantageous for the design of switched-mode rectifiers. Furthermore, the increasing importance of input power quality (and the advent of regulations and recommendations governing it [4-6]) make improved rectification techniques important for many commercial and industrial applications. For these reasons, we have applied the cellular conversion approach to the task of high-power-factor switched-mode rectification.

This paper describes the design, implementation, and experimental evaluation of a six-cell, six-kilowatt cellular rectifier system. Power is converted from the three-phase 208 V mains to a 410 V dc output at nearly unity power factor. The cellular rectifier system implements both distributed load sharing and distributed ripple cancellation, eliminating the need for any centralized control. Furthermore, the cellular converter system mitigates some of the major drawbacks of its single-converter counterpart, and achieves performance levels unattainable with an equivalent single converter.

Section II describes some of the motivations for the use of a cellular architecture in rectifier applications, and provides an introduction to the cell topology used in the prototype system. Section III quantifies the effects of interleaving the cells on the aggregate input current ripple. Section IV describes the design of the prototype system, including the system architecture, the power stage, the load-sharing control system, and the ripple cancellation control system. Section V provides experimental results from the laboratory prototype, and Section VI draws conclusions and presents a preliminary evaluation of the approach.

II. SWITCHED-MODE RECTIFICATION

The emergence of recent standards and recommendations on power quality reflect a growing need to reduce the impact of electronic equipment on the utility. While only voluntary measures such as IEEE Std 519-1992 are currently in place in the United States [4], the European Community has already moved towards stronger controls. Restrictions on line harmonics are already in place for household and similar electrical equipment up to 415V, 16 A [5,6], and future regulations will apply to equipment with higher ratings [7]. These developments have lead to an increased interest in switched-mode rectifiers which draw quasi-sinusoidal input current at high power factor, and produce a controlled output voltage.

The full-bridge converter is often used for switched-mode rectification. However, this solution requires a high number of active switches (and attendant ancillary circuitry), and is relatively complex to control. Another approach is to utilize a single-phase switched-mode rectifier for each phase of the

0-7803-4489-8/98/$10.00 © 1998 IEEE

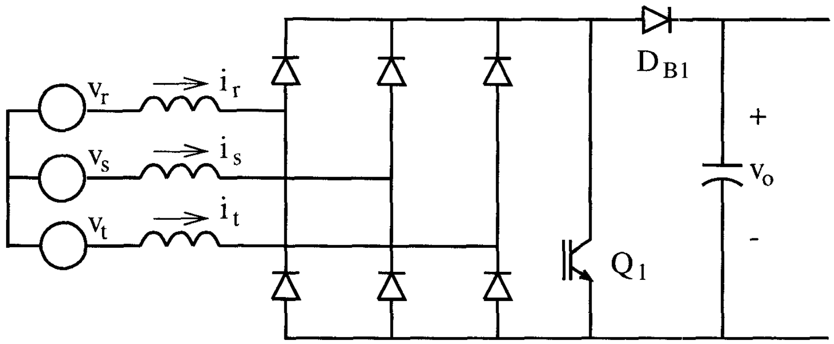

Figure 1 The three-phase single-switch boost rectifier.

three-phase input, though this solution retains much of the complexity of the full-bridge converter. A desire to attain the performance advantages of these rectifiers without the high level of complexity has led to the development of the three-phase single-switch boost rectifier of Fig. 1. This converter topology, introduced in [8], has undergone rapid development in recent years [9-17].

The operating principle of this discontinuous-mode converter is as follows: The switch Q_1 is turned on at the beginning of each (fixed-length) switching period, and held on for a specified duty cycle, *d*. During this on period, the diode-bridge inputs are shorted together through the diodes and switch Q_1. Neglecting the effects of the input filter, the inductor currents i_r, i_s, i_t rise from zero by an amount proportional to their respective phase voltages. When Q_1 is turned off, the inductor currents return back to zero through diode D_{B1} and the output capacitor. Thus, the average current delivered from each phase is approximately proportional to the phase voltage, yielding fundamentally resistive behavior. The average total current delivered to the output is controlled by varying the duty cycle of switch Q_1, while the output voltage v_o is controllable to voltages above the peak line-to-line mains voltage.

With its supporting input filter, this topology provides high power factor input current waveforms using a single ground-referenced active switch and a very simple control strategy. The discontinuous-mode operation minimizes the energy storage requirements of the input inductors and provides soft turn-off of the diodes. However, it also subjects the devices to relatively high peak current stresses. Furthermore, the converter requires a relatively large input filter to attenuate the input current switching harmonics to acceptable levels (to meet conducted EMI requirements, for example). The size of the input filter is perhaps the single largest drawback of the approach.

Consider the benefits of paralleling cells constructed using the single-switch rectifier topology. The single-switch rectifier has many of the desired characteristics for a utility-interface converter, except for its high level of unfiltered input ripple current harmonics. *Interleaving* of paralleled converter cells, in which the individual cells are switched out of phase, allows a high degree of harmonic cancellation between the cell currents [18-21]. This results in greatly reduced aggregate input and output ripple, along with a commensurate reduction in filtering requirements. Interleaving of paralleled single-switch boost rectifiers has been previously demonstrated to be effective for reducing the high input current ripple associated with this topology [16,17]. By using a cellular conversion approach (with distributed control), and applying the concept of interleaving, the topology of Fig. 1 can be applied to create a simple, high power factor utility interface with minimal input filtering.

Other advantages of cellular architectures also apply to this application. For example, utility interface converters often need to be constructed in a variety of ratings. By employing a cellular architecture, it is possible to construct a family of systems with a range of ratings using a single cell design. The power rating of a specific system is determined by the number of cells used. Unlike a single large converter, the individual cells can be constructed using single-die devices in inexpensive packages, and manufactured using an automated assembly process. The coupling of these facts may lead to a significant cost advantage over a conventionally-designed system. Furthermore, because a cellular system can be designed to operate after individual cell failures, significant improvements in reliability and availability may be obtained. Thus, there are several important ancillary advantages to employing a cellular architecture in rectifier applications.

III. Interleaving Benefits

One of the primary benefits of using the three-phase single-switch boost rectifier in a cellular architecture is the ability to use interleaving to cancel the large input (switching) current ripple drawn by the topology. This is an important benefit, since the input filters required for meeting EMI specifications can be quite large for this converter topology (possibly even larger than the converter itself), due to the fact that it operates in discontinuous conduction mode. This section investigates the amount of ripple reduction which can be expected through interleaving, and assesses its likely impact on system design.

One important characteristic of this rectifier is that the switching ripple frequency content includes components not only at the switching frequency and its harmonics, but at the sum and difference frequencies of the line and switching frequencies and their harmonics. Practically speaking, this

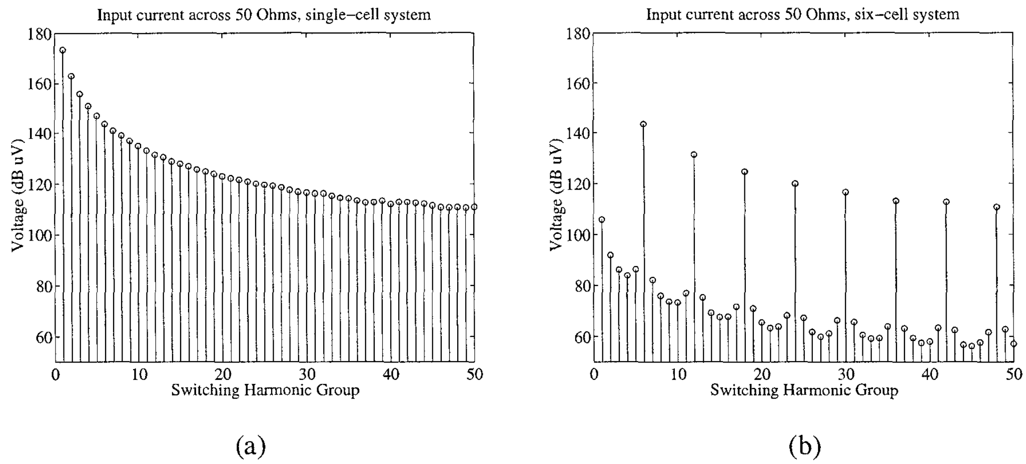

Figure 2 Worst case input current ripple spectral components for example three-kilowatt rectifier systems. (a) Single-cell system. (b) Six-cell system.

means that the switching ripple energy is concentrated in bands, which we term switching harmonic *groups*, centered around multiples of the switching frequency.

Regulatory limitations on input current spectral content (such as those set by agencies like the FCC and VDE) tend to be flat over an extremely wide frequency range, and are not indexed to equipment power level (see [22], for example). Interleaving N converter cells has two beneficial effects in meeting such EMI limits. First, it tends to attenuate (by cancellation) the first N ripple harmonic groups in the spectrum (which are the hardest to attenuate by filtering), as well as harmonic groups at higher frequencies. Second, it reduces the net ripple amplitude by a factor N or more, thus reducing the peak ripple for which the EMI filter has to be designed.

To gain a quantitative understanding of these benefits, consider the comparison of a single large converter with an equivalent interleaved converter systems having 6 cells. For our purposes, an "equivalent" system has the same total magnetic energy storage, cell switching frequency, and output power as a single large converter. We consider the example of a three-kilowatt converter (L = 6.7 µH, f_{sw} = 150 kHz) which generates a 410 V output from a 208 V (line-to-line, rms) input. At each frequency, we compute the worst ripple component that occurs within each switching harmonic group across the load range of the converter and across a +10% / -15% variation in input voltage. Figure 2 (a) shows these worst-case spectral components for the single large converter, while Figure 2 (b) shows the results for an equivalent interleaved converter system with 6 cells.

In the single-cell system, the worst-case harmonic component to filter is 173 dB µV at 150 kHz. For the six-cell case, this worst-case first harmonic group component is reduced by some 65 dB, leaving the sixth harmonic-group component as the worst to be filtered (143 dB µV at 900 kHz). The reduction in amplitude and increase in frequency of the worst-case component considerably eases the requirements on the EMI filter. (Because higher frequencies are much easier to filter, the first switching harmonic group component may in fact *still* be the hardest to filter for this highly interleaved case.) What is clear from these results is that the amount of EMI filtration required to meet a flat EMI standard is reduced considerably when several cells are interleaved. Furthermore, the reductions in filtering requirements are significant even for a modest degree of interleaving.

IV. Prototype System Design

This section describes the design of a six-cell, six-kilowatt prototype system which rectifies the three-phase 208 V mains to a 410 V dc output at high power factor. The input supply voltage is assumed to stay within tolerances of +10% and -15%, while the output voltage is regulated to within ±3% of nominal. The system implements both distributed load sharing (via the UC3907 load-sharing control method [23]) and distributed interleaving (via the method developed in [24, 25]), eliminating the need for any centralized control. To the authors' knowledge, this is the first system developed in which control of both ripple cancellation and load-sharing are entirely distributed. The system is "hot-swap" capable, meaning that individual cells can be removed and inserted (for repair, etc.) while the system is running under load. Furthermore, the system is designed to allow alternative control methods to be easily implemented through the use of "piggyback" control boards.

We will describe the system architecture and cell power stage design, the control structure (including output voltage, load-sharing and interleaving control), and the fusing and protection methods. Additional information about the design, layout and control of the system can be found in [26].

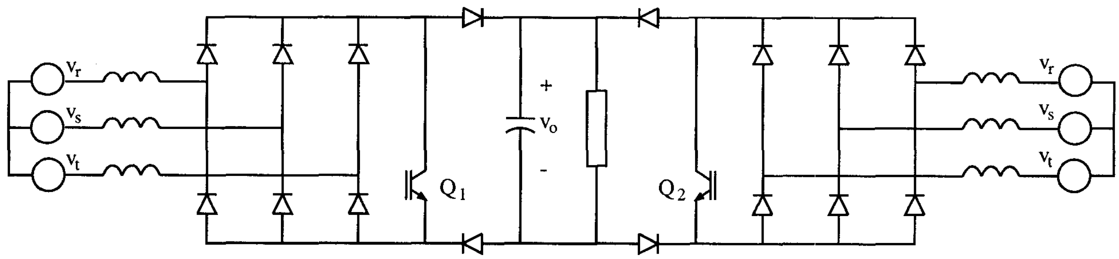

Figure 3 Structure of a single cell composed of two interleaved single-switch converters.

A. System Architecture

The prototype system has six cells, each of which has a nominal output rating of 1 kW and is designed to handle a continuous output power of 110% of nominal. The prototype system fits in a standard 19" rack assembly. Each cell fits in a 6U (10.5") high, 14T (2.8") wide module, and connects into the backplane via a DIN41612MH connector which is indexed to connect the system ground first upon cell insertion. The power portion of the backplane comprises a low-inductance three-phase input bus and a low-inductance output/ground bus, both of which are wired to an external connector. The connections are such that all of the cells are connected to the low-inductance busses through similar impedances. The control portion of the backplane comprises twisted-pair (signal and ground) interconnections among the cells for "single-wire" communication of current-sharing and ripple-cancellation information.

B. Cell Power Stage Design

Each cell is constructed on a single printed circuit board as two interleaved single-switch boost rectifiers (which we term *half*-cells) driven from a common control circuit, as illustrated in Fig. 3. This affords some efficiency in the use of control and sensing circuitry, and reduces the ripple generated by an individual cell. A photograph of a completed cell is shown in Fig. 4. Note the additional diodes used in the output current return paths of the half-cells, as shown in Fig. 3. (The boost diodes and active switch of one of the half cells are visible in Fig. 4, mounted to a heat sink behind the control circuitry.) As described in [16, 17], in order to parallel single-switch rectifiers, each rectifier must have an additional boost diode in its return path. The diode is needed to prevent cross-conduction among different half-cells; without it, current flowing from the positive phase and through the transistor of one half-cell can return through the negative phases of a different half-cell. Incorporating the additional diode in each half-cell ensures that this cannot happen, and makes the half-cells operate independently. In addition to causing a slight decrease in efficiency, the additional diode prevents the active switches from being referenced to ground. As a result, they have to be driven through floating gate drive circuits. However, these disadvantages are heavily outweighed by the tremendous performance increases that can be gained through interleaving.

Design of the cell power stage centered on the task of selecting the cell inductances and switching frequency such that the cell would meet its rated output power over the specified input voltage range with each half-cell operating in discontinuous conduction mode. This had to be accomplished while meeting the conflicting goals of minimizing component size and cost and minimizing the losses and temperature rises. For a candidate switching frequency, the method of [10] was used to select a boost inductor value, expected semiconductor losses were computed, and candidate inductor designs were identified and their expected losses computed. This process was repeated across a wide range of switching frequencies, yielding a set of candidate designs from which the final design was selected.

From the candidate designs, a switching frequency of 150 kHz and line inductances of 40.4 μH were selected for each half-cell. The inductors were constructed using eleven turns of twelve gauge wire on an RM12PA315 core. This core is one size larger than necessary, to provide flexibility for

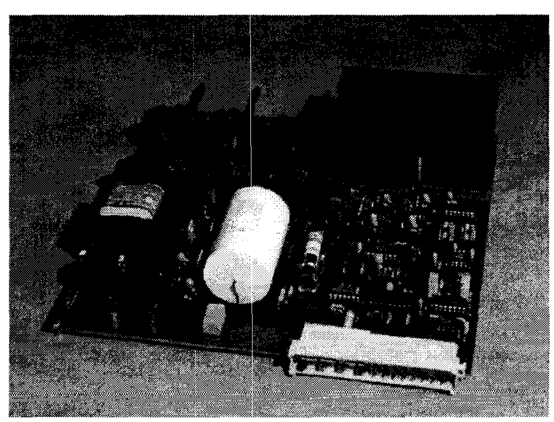

Figure 4 A photograph of a prototype converter cell.

future uses. IRF840G MOSFETs were used for the main boost switches, and HFA08TB60 ultra-fast recovery rectifiers were used for the boost diodes. These were attached to PC-board mountable extruded heat sinks; sufficient cooling was obtained using natural convection, due to the distributed nature of heat generation in the cellular system. MUR160 ultra-fast recovery diodes were used for the input bridges. The use of extremely fast diodes for the input bridges was found to be necessary to achieve proper operation at the selected switching frequency. Because the input is three-phase, there is little low-frequency ripple in the output voltage. Hence, only a single 10 μF film capacitor was used at the output of each cell.

Each cell is provided with high-speed (semiconductor) fuses at the input, and a slower fuse at the output. Inrush current limiters are placed in series with the boost inductors to soften the startup transient, and the UC3825 PWM controller provides both soft-start and current-limit protection functions. The MOSFET switches have RCD snubbers which clamp their drain voltages to a value slightly higher than the output voltage, and a Metal Oxide Varistor (MOV) at the output of each cell provides absolute fault-condition voltage clamping protection. These measures were sufficient to provide for a stable, well controlled startup (even during hot-swap conditions) and to protect the cells during fault conditions.

C. Control Design

Here we discuss the control design for the cellular rectifier system. The control of the rectifier system is entirely distributed. Each cell has its own output voltage control loop, as well as an outer loop which balances current with the other cells. Each cell also has its own interleaving controller which adjusts the switching frequency and phase to achieve ripple cancellation with other cells. We will present details about the output voltage control design, the current-sharing control design, and the ripple cancellation control design.

In the baseline configuration of the system, the individual cells employ duty-ratio control of the output voltage. Due to the discontinuous conduction-mode operation of the half-cells, controlling duty ratio is equivalent to controlling the local average cell output current. The local average output current of the converter is a function of the duty ratio and position in the line cycle, as well as other operating parameters such as output voltage and boost ratio [9]. Using the results of [9], we can make an injected current model for each half-cell

$$i_{out} = K_f d^2 \tag{1}$$

where K_f varies from 13.75 to 55.0 over the line cycle for the parameters of the prototype system. Considering a proportional controller

$$d = K_p\left[v_{ref} - v_o\right] \ , \tag{2}$$

we find an output current characteristic of

$$i_{out} = K_f K_p^2 \left[v_{ref} - v_o\right]^2 \ . \tag{3}$$

The half-cell thus has a (nonlinear) resistive output characteristic, where the output resistance is load-varying, and also varies with position in the input line cycle; the output resistance of a full cell is precisely half that of a half-cell. It is easily shown that the incremental output resistance of each half-cell about an operating point is

$$R_{out} = \frac{1}{2K_p\sqrt{K_f I_{out}}} \tag{4}$$

which decreases with increasing load current, and is only mildly affected by the position in the line cycle.

Using this model, it is easily shown that the output control dynamics are stable and well damped for a resistive or current-source load [27]. For the prototype system, a proportional control gain $K_p = 0.028$ V^{-1} was selected. This value yields load regulation of less than 5% over the load range, and with a 10 μF output capacitor per cell yields an output voltage control bandwidth that exceeds the 360 Hz input voltage ripple frequency. Furthermore, because the output voltage is controlled with high bandwidth, the input line current harmonics are reduced as compared to low-bandwidth control [9].

In its baseline configuration, the prototype system uses the UC3907 single-wire current-sharing control method [23]. This current-sharing method operates as follows: To achieve current sharing with the other cells, each cell shifts its own voltage reference $v_{ref,j}$ via integral control, based on the difference between its own output current and the maximum output current of all the cells minus a small offset ΔI. The j^{th} cell voltage reference is adjustable over a small range from a base value $v_{r,j,base}$ to a maximum value $v_{r,j,max}$, and is prevented from going outside of this range by clamping of the reference at the boundaries. In this manner, the cell voltage references adjust incrementally such that current sharing is achieved. The offset ΔI ensures that the highest-current cell will carry slightly more current than the other cells under static conditions, thus preventing the maximum current signal from chattering among different cell currents. The offset also guarantees that the voltage reference of the highest-current cell will always be driven towards its base value.

The resistive output impedance characteristic of the cells leads to current-sharing dynamics which are guaranteed to be stable and overdamped, as described in the analysis of the UC3907 current-sharing method presented in [27]. This is true regardless of the number of cells which are operated in parallel.

The prototype system implements distributed interleaving within two groups of (up to) three cells each, while the two *groups* of three cells cancel ripple passively, as described in [25]. Thus, within each group, either 2, 4, or 6 half-cells are interleaved depending on the number of operational cells within the group. In the distributed interleaving approach, each cell has its own clock generator. All the clock generators within a group are connected via a single-wire

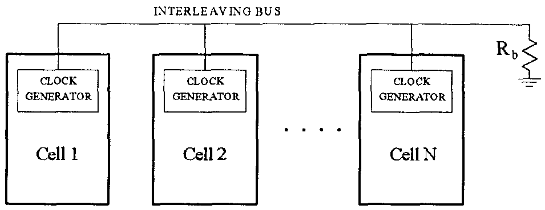

Figure 5 The distributed interleaving approach.

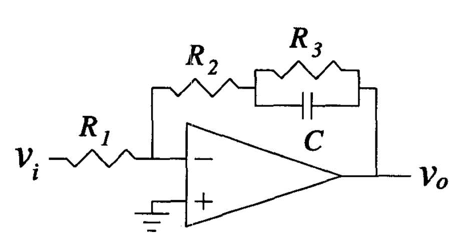

Figure 6 Loop filter structure for the prototype system. C = 0.68 μF, R_1 = 90.9 kΩ, R_2 = 10 kΩ, R_3 = 10 MΩ.

interleaving bus (Fig. 5), over which the clock generators share information about their frequencies and phases. Because shared information is only used to adjust the clock frequencies and phases, failures affecting the interleaving bus may shut down the interleaving function, but do not cause the whole system to fail. Furthermore, the approach automatically accommodates varying numbers of cells within a group; proper clock phasing for ripple cancellation is always maintained (180° for two cells, 120° for three). This leads to an active ripple cancellation system which is simple, effective, and robust to subsystem failures.

The clock generator structure introduced in [24, 25] was used to implement the distributed interleaving system. In this implementation, each clock generator injects its own clock onto the interleaving bus, and uses a special phase-locked loop to lock out of phase with the other clock signals on the bus. The clock generator design is similar to the system developed in [24, 25], with slightly different parameters. The clock generators implemented here employ a phase detector gain, K_d, of 7.95, and a VCO gain, K_o, of 6090 rad/(V-s). Both the base operation frequency and the phase detector gain can be adjusted via potentiometer settings. The loop filter of Fig. 6 is employed in the prototype system, yielding clock-phase control dynamics which are stable and well damped for up to three cells in a group.

V. Experimental Results

This section presents some experimental results from the prototype converter system. The prototype converter system was run both from the Cambridge utility through an isolation transformer, and from a Hewlett-Packard 6834B three-phase AC source.

The prototype system operated as designed over the entire load range. Figure 7 shows operation of the prototype system at 97% of full load. As can be seen, the line current waveforms are quasi-sinusoidal, with the expected waveform shape (*cf* [9]). The measured line harmonic content matches the theoretical predictions of [9] very closely, with the 5th and 7th harmonics contributing the majority of distortion. The power factor for this load condition is 0.994, with 10.3 % Total Harmonic Distortion (based on 40 harmonics), both of which match theoretical predictions.

As can be seen from the small level of ripple in the line current of Fig. 7, the distributed interleaving greatly reduced the input switching ripple as compared to the non-interleaved case. The distributed interleaving circuitry functioned as expected over the load range for the cases of both two- and three- cell groups, and the two interleaving groups operated independently (as desired) for up to the full complement of six cells. Figure 8 shows the clocks of the individual cells with the system at 70% of full load for both the two- and three-cell cases. As can be seen, the distributed interleaving circuitry properly phased the individual switching waveforms in order to cancel the switching ripple in both cases.

The load-sharing and output voltage control behavior of the system also met performance expectations. Figure 9 shows the current-sharing characteristic for six cells over the load range. Acceptable current sharing is achieved over the whole load range, with current sharing within a few percent achieved over most of the range. The output voltage was regulated to within specifications over the whole load range, and the transient response was stable and over damped (as expected) for even large load steps.

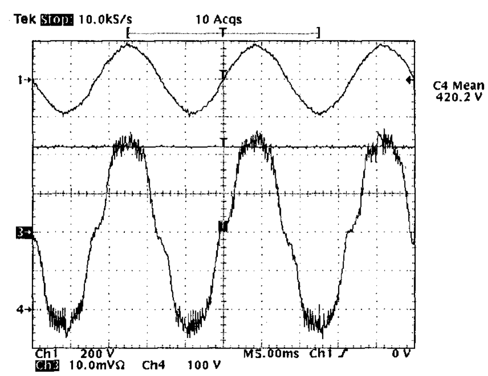

Figure 7 Circuit waveforms for 6 cells operating at 97% of full load (R_L = 30 Ω) from the Cambridge utility through an isolation transformer. Channel 1 is the line voltage (200 V/div), channel 3 is the line current (10 A/div), and channel 4 is the output voltage (100 V/div). Note that the observed switching ripple is undersampled by the oscilloscope.

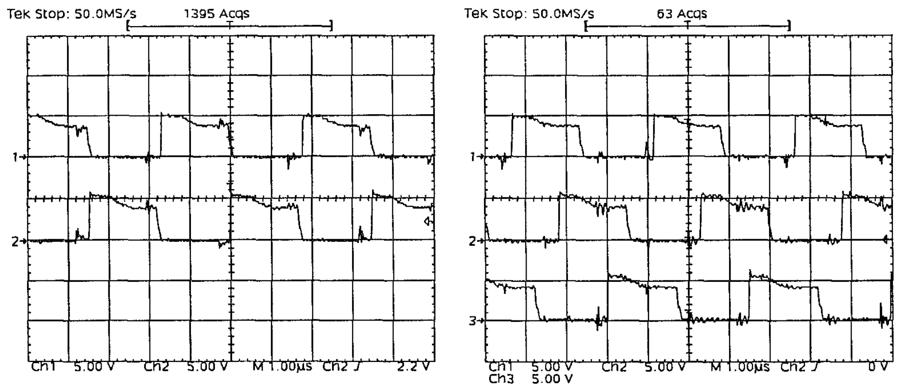

Figure 8 Clock waveforms for two and three cells. The system was operating at 70% of rated load in both cases.

VI. CONCLUSIONS

The use of cellular converter architectures for the construction of switched-mode rectifier systems has several potential advantages over conventional approaches, including improvements in performance, reliability, and cost. To realize these advantages, however, it is necessary to develop appropriate design and control approaches, and demonstrate them experimentally. This paper has presented the design and experimental evaluation of a prototype cellular rectifier system which uses entirely distributed control. The performance increases that can be obtained through interleaving of the cells has been quantified. The design of the cellular rectifier system has been addressed, including the system architecture, the power stage design, and the fusing and protection methods. The control design for the cellular converter has also been described, including the methods used to control the output voltage while regulating current-sharing among cells, and the methods used to obtain ripple cancellation among the cells. Finally, an experimental evaluation of the prototype system has been performed.

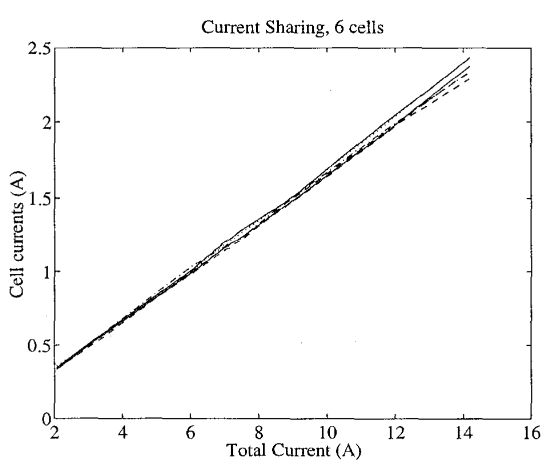

Figure 9 Current-sharing data for six cells.

It may be concluded from the experimental results that the prototype system successfully demonstrates the technical feasibility of the cellular design approach for this application. Controlled, high-power-factor rectification is achieved along with excellent output voltage and load-sharing regulation using entirely distributed control. The system also achieves a high degree of input switching ripple cancellation as compared to a single large converter implementation, without requiring a centralized controller. This advantage alone merits the further development of the approach.

ACKNOWLEDGMENTS

The authors would like to acknowledge the support for this research provided by the Bose Foundation and by the Office of Naval Research under grant number N00014-96-1-0524. Generous equipment grants from the Tektronix and Intel Corporations facilitated this research and are appreciated.

REFERENCES

[1] J.G. Kassakian, "High Frequency Switching and Distributed Conversion in Power Electronic Systems," *Sixth Conference on Power Electronics and Motion Control (PEMC 90)*, Budapest, 1990.

[2] J.G. Kassakian and D.J. Perreault, "An Assessment of Cellular Architectures for Large Converter Systems," *First International Conference on Power Electronics and Motion Control*, Beijing, 1994, pp. 70-79.

[3] T. Kohama, T. Ninomiya, and M. Shoyama, "Characteristics of a Parallel-Module High Power-Factor AC-to-DC Converter System with Current-Balancing Controllers," *IEEE International Telecommunications Energy Conference*, 1995, pp.791-795.

[4] IEEE Standard 519-1992, "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *Institute of Electrical and Electronic Engineers, Inc.*, 345 East 47th Street, New York, NY 10017.

[5] International Standard IEC1000-3-2 (also IEC Publication 1000-3-2), "Electromagnetic Compatability (EMC) - Part 3: Limits - Section 2: Limits for harmonic current emissions," *Bureau of the International Electrotechnical Commission*, 3 rue de Varembé, Geneva.

[6] European Standard EN 60 555-2 (also IEC Publication 555-2), "Disturbances in supply systems caused by household appliances and similar electrical equipment - Part 2 : Harmonics," *European Committee for Electrotechnical Standardization*, rue Brederode 2, B-1000 Brussels.

[7] T. Key, "Standards for Harmonic Control - Protecting the Electric Power Supply," *IEEE Standards Bearer*, April 1994.

[8] A.R. Prasad, P.D. Ziogas, and S. Manias, "An Active Power Factor Correction Technique for Three-Phase Diode Rectifiers," *IEEE Trans. Power Electronics*, Vol. 6, No. 1, Jan. 1991, pp. 83-92.

[9] J.W. Kolar, H. Ertl, and F. Zach, "Space Vector-Based Analytical Analysis of the Input Current Distortion of a Three-Phase Discontinuous-Mode Boost Rectifier System," *1993 IEEE Power Electronics Specialists Conference*, Seattle, WA, 1992, pp. 696-703.

[10] J.W. Kolar, H. Ertl, and F. Zach, "A Comprehensive Design Approach for a Three-Phase High-Frequency Single-Switch Discontinuous-Mode Boost Power Factor Corrector Based on Analytically Derived Normalized Converter Component Ratings," *IEEE Trans. Industry Applications*, Vol. 31, No. 3, May/June 1995, pp. 569-582.

[11] E.H. Ismail and R. Erickson, "Single-Switch 3ϕ PWM Low Harmonic Rectifiers," *IEEE Trans. Power Electronics*, Vol. 11, No. 2, March 1996, pp. 338-346.

[12] K. Chen, A. Elasser, and D.A. Torrey, "A Soft Switching Active Snubber Optimized for IGBTs in Single Switch Unity Power Factor Three-Phase Diode Rectifiers," *1994 IEEE Applied Power Electronics Conference*, 1994, pp. 280-286.

[13] S. Gatarić, D. Boroyevich, and F.C. Lee, "Soft-Switched Single-Switch Three-Phase Rectifier With Power Factor Correction," *1994 IEEE Applied Power Electronics Conference*, 1994, pp. 738-744.

[14] R.L. Lin and F.C. Lee, "Novel Zero-Current-Switching-Zero-Voltage-Switching Converters," *1996 IEEE Power Electronics Specialists Conference*, Baveno, Italy, Sept. 1996, pp. 438-442.

[15] Q. Huang and F.C. Lee, "Harmonic Reduction in a Single-Switch, Three-Phase Boost Rectifier with High Order Harmonic Injected PWM," *1996 IEEE Power Electronics Specialists Conference*, Baveno, Italy, Sept. 1996, pp. 1266-1271.

[16] V. Chunkag and F.V.P. Robinson, "Interleaved Switching Topology for Three-Phase Power-Factor Correction," *Fifth International Conference on Power Electronics and Variable Speed Drives*, London, UK, Oct. 1994, pp. 280-285.

[17] F.V.P. Robinson and V. Chunkag, "Parallel Connection of Single-Switch Three-Phase Power-Factor Correction Converters for Interleaved Switching," *IEE Proc. Electr. Power Appl.*, Vol. 144, No. 6, Nov. 1997, pp. 423-433.

[18] B.A. Miwa, D.M. Otten, and M.F. Schlecht, "High Efficiency Power Factor Correction Using Interleaving Techniques," *IEEE Applied Power Electronics Conference*, Boston, MA, 1992, pp. 557-568.

[19] B.A. Miwa, "Interleaved Conversion Techniques for High Density Power Supplies," Doctoral Thesis, Dept. of EECS, *Massachusetts Institute of Technology*, June 1992.

[20] C. Chang, "Current Ripple Bounds in Interleaved DC-DC Power Converters," *Proceedings of the 1995 International Conference on Power Electronics and Drive Systems*, Singapore, 1995.

[21] C. Chang and M. Knights, "Interleaving Technique in Distributed Power Conversion Systems," *IEEE Trans. Circuits and Systems - I*, Vol. 42, No. 5, May 1995, pp. 245-251.

[22] Federal Communications Commission, Code of Federal Regulations, Title 47, Part 15.

[23] M. Jordan, "UC3907 Load Share IC Simplifies Parallel Power Supply Design," *Unitrode Application Note U-129*, Unitrode Corp., Merrimack, NH.

[24] D.J. Perreault and J.G. Kassakian, "Distributed Interleaving of Power Converters," *Seventh International Power Electronics and Motion Control Conference*, Budapest, Hungary, Sept. 1996, pp. 2/149-2/153.

[25] D.J. Perreault and J.G. Kassakain, "Distributed Interleaving of Paralleled Power Converters," *IEEE Trans. Circuits and Systems -I*, Vol. 44, No. 8, August 1997, pp. 728-734.

[26] D.J. Perreault, "Design and Evaluation of Cellular Power Converter Architectures," Doctoral Thesis, Dept. of EECS, *Massachusetts Institute of Technology*, June 1997.

[27] D.J. Perreault, J.G. Kassakian, and G.C. Verghese, "Stability Analysis of Nonlinear Current-Sharing Techniques," *1997 IEEE Power Electronics Specialists Conference*, St. Louis, MO, June 1997, pp. 665-671.