

# Optimization of Transistors for Very High Frequency dc-dc Converters

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**Abstract**—This document presents a method to optimize integrated LDMOS transistors for use in very high frequency (VHF, 30-300 MHz) dc-dc converters. A transistor model valid at VHF switching frequencies is developed. Device parameters are related to layout geometry and the resulting layout vs. loss tradeoffs are illustrated. A method of finding an optimal layout for a given converter application is developed and experimentally verified in a 50 MHz converter, resulting in a 35% reduction in power loss over an un-optimized device. It is further demonstrated that hot-carrier limits on device safe operating area may be relaxed under soft switching, yielding significant further loss reduction. A device fabricated with 20-V design rules is validated at 35-V, offering reduced parasitic resistance and capacitance. Compared to the original design, loss is up to 75% lower in the example application.

**Index Terms**—resonant dc-dc converter, resonant boost converter, very high frequency, VHF integrated power converter, class  $\Phi$  inverter, class F power amplifier, class E inverter, resonant gate drive, self-oscillating gate drive, resonant rectifier, harmonic peaking.

## I. INTRODUCTION

REDUCTION of size, weight, cost, and greater integration is a continual theme in power conversion. A promising solution uses a resonant power stage with soft-switching and soft-gating operating in the very high frequency (VHF, 30 MHz to 300 MHz) regime. Such converters can achieve very good efficiencies over wide load and input ranges for power levels from a few watts to hundreds of watts [1]–[3]. However, the device losses that dominate in VHF converters are significantly different than under hard-switched operation. As a result only a small subset of commercially available power MOSFETs are suitable for VHF converters. These tend to be discrete RF LDMOSFETs that are expensive and packaged in a manner not suitable for small, integrated converters. On the other hand, while offering a high degree of integration, most semiconductor processes for power conversion are intended for operation at a few megahertz. In this case, optimization for hard-switched operation has driven tradeoffs at the process, design-rule, and layout stages [4]–[6] that produce devices with mediocre VHF performance.

This paper shows that good VHF performance is achievable using an integrated power process. In the case of the power process used for this work, much of the improvement derives from the optimization of the device layout. Thus we focus on understanding how device losses in resonant VHF converters differ from those observed under hard switching (Section II). A set of easily measured device parasitics is chosen and used to parametrize a model that predicts device loss given a particular resonant converter circuit. In turn, these parameters are connected to the device layout which permits a layout optimization with device loss as a cost function (Section III). In an example application, a 38% reduction in device loss is achieved as compared to the devices initially available in the power process.

Further benefit arises through relaxation of the safe operating area (SOA) constraints normally specified for devices under hard-switched operation (Section IV). In particular, we demonstrate that at least in some power processes devices can be operated under soft-switching at higher peak voltages than their specifications for hard-switching. This means that at a given peak operating voltage devices with smaller parasitic resistance and capacitance can be used, reducing device loss and improving overall converter efficiency.

For an example application we show that the combination of layout optimization and relaxation of the SOA leads to better than 57% reduction in device loss for LDMOSFETs fabricated in the available integrated power process. Performance of an optimized device at VHF is verified through the construction and testing of two converters. Results are presented in Section V.

## II. VHF DEVICE LOSS MODEL

Semiconductor device losses place critical limits on the design and performance of power converters. In hard-switched operation the various loss mechanisms are usually split into conduction loss, switching loss (often subdivided into overlap loss and capacitive discharge loss), and gating loss [3]. Unlike conduction loss, the switching and gating losses are frequency dependent. Beyond a few megahertz these mechanisms can

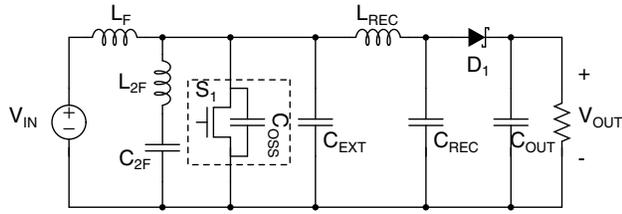


Fig. 1.  $\Phi_2$  resonant boost converter with  $C_{OSS}$  and the external capacitance  $C_{EXT}$  explicitly drawn.

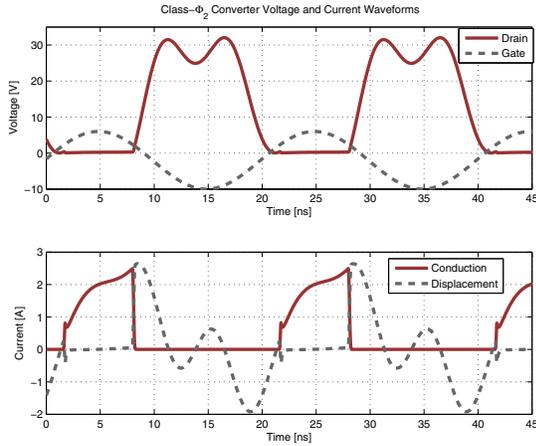


Fig. 2. Simulated  $\Phi_2$  resonant boost converter switch voltage and current waveforms.

quickly dominate total converter loss. Therefore, in seeking higher switching frequencies to reduce converter size, weight, and cost, it is necessary to mitigate switching and gating losses.

One way of decreasing frequency-dependent losses is by using soft-switching and soft-gating topologies such as the Class- $\Phi_2$  converter of Figure 1 [7]. During operation the drain voltage naturally rings to zero before the switch turns on (Figure 2). This eliminates turn-on overlap loss and capacitive discharge loss. Turn-off overlap also remains small because capacitive snubbing via  $C_{EXT}$  prevents the drain voltage from rising appreciably before the switch current falls to zero. Gating loss is minimized by using a resonant gate drive scheme to recover a portion of the energy delivered to the gate. This technique is effective when the desired switching transition is longer than a gate time constant [8].

Mitigating gating and switching loss as described above changes the relative importance of the various parasitic capacitances and resistances associated with the device. For example, with hard gating, device gating loss is independent of gate resistance, while with resonant (soft) gating, gate parasitic resistance is an important consideration in the gating loss. Moreover, the types of circuit topologies that are suitable for VHF operation also bring to prominence loss mechanisms that are negligible with more conventional circuit topologies and operating frequencies. In particular, losses associated with off-state conduction of current through device capacitances

TABLE I  
VHF VS. HARD-SWITCHED LOSS MECHANISMS

Loss Mechanism	Hard-Switched	Soft-Switched VHF
Conduction	$\propto I_{cond,RMS}^2 R_{DS}$	$\propto I_{cond,RMS}^2 R_{DS}$
Gating	$\propto C_{ISS} f_{SW}$	$\propto C_{ISS}^2 R_{GATE} f_{SW}^2$
Off-State Conduction	N/A	$\propto C_{OSS}^2 R_{OSS} f_{SW}^2$
Overlap	$\propto f_{SW}$	N/A
Cap. Discharge	$\propto C_{OSS} f_{sw}$	N/A

(and associated resistances) can become quite significant at VHF frequencies. When a device turns off in a typical low-frequency converter, current commutates to a different device, and the drain-source voltage of the off device is clamped. Therefore, current only passes through the device output capacitance ( $C_{OSS}$ ) during a brief commutation interval. By contrast, in a typical VHF converter such as the  $\Phi_2$  converter,  $v_{DS}$  changes continually when the switch is off. The result is a substantial circulating current through  $C_{OSS}$  during the off state (the displacement current in Figure 2), giving rise to an off-state conduction loss in the equivalent series resistance of the output capacitance,  $R_{OSS}$ .

It should be appreciated that such off-state conduction loss is in fact a frequency-dependent loss: Under soft-switching there is an off-state circulating drain current,  $i_{disp}$ . Thus, the off-state conduction loss is linearly dependent on  $R_{OSS}$  and square-law dependent on the RMS of  $i_{disp}$ . Since  $i_{disp}$  is proportional to  $C_{OSS}$  we see that off-state conduction loss is proportional to  $C_{OSS}^2$ .<sup>1</sup> Gate loss with resonant gating follows a similar pattern and therefore it is proportional to both  $R_{GATE}$  and  $C_{ISS}^2$ .

Table I summarizes the differences between hard-switched and soft-switched losses. It identifies each loss important in the two different operating ranges. Some of the parameters that scale each loss component are also included. These differences highlight the relative importance of switch parameters that ultimately drive different device tradeoffs for switches used at VHF versus those intended for lower-frequency, hard-switched operation.

To adequately represent device loss under soft-switching and soft-gating operation, we consider the model of Figure 3. In this model we neglect the coupling from the output port back to the input port via  $C_{GD}$  in favor of lumping it with  $C_{ISS}$  and  $C_{OSS}$ .<sup>2</sup> The resistances  $R_{DS}$ ,  $R_{OSS}$ , and  $R_{GATE}$  correspond to the three important VHF loss mechanisms: conduction loss, off-state conduction loss, and gating loss. The switch-resistor model is an adequate representation of the dc characteristics of the device because efficient operation of the VHF converter requires that the device never conduct out of triode.

The frequency dependence of each loss mechanism can be

<sup>1</sup>Since the open-switch drain source impedance is held constant for a given VHF converter design we assume that an increase in  $C_{OSS}$  is offset by a corresponding decrease in  $C_{EXT}$ , thus  $V_{DS}$  remains unchanged and  $i_{disp}$  increases proportional to  $C_{OSS}$  owing to falling impedance [1], [3].

<sup>2</sup>This is a reasonable omission. Under soft-switching the  $V_{GS}$  rises through  $V_{TH}$  only after  $V_{DS}$  has already rung to zero. In addition, devices favorable for VHF operation require that  $C_{GD}$  is a small fraction of the gate capacitance, this is typical of lateral power MOSFETS.

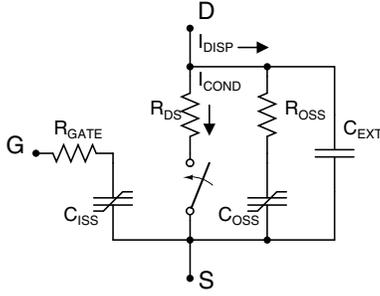


Fig. 3. MOSFET model with loss elements relevant under soft-switched VHF operation

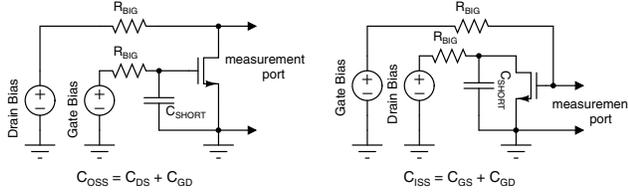


Fig. 4. Two-terminal measurements are taken on an impedance analyzer to determine  $C_{OSS}$ ,  $C_{ISS}$ , and  $C_{GD}$ .  $C_{SHORT}$  functions as an ac-short at 1 MHz, the measurement frequency. The dc biases of  $V_{DS}$  and  $V_{GS}$  are controlled via external sources connected through large resistances.

understood by assuming the shapes of the drain- and gate-voltage waveforms are maintained as frequency is scaled. Conduction loss will remain constant because  $R_{DS}$  is not dependent on frequency and the RMS of  $i_{cond}$  does not change. However, both  $i_{disp}$  and  $i_{gate}$ , the currents associated with off-state conduction and gating loss, flow in branches where the impedance is dominated by capacitance. Falling impedance with frequency causes a proportional rise in current resulting in a square-law dependence of displacement and gating loss on frequency. At a given frequency, increasing the branch capacitances causes a proportional rise in their currents and a square-law rise in displacement and gating loss with capacitance, as discussed earlier.

The device parameters, in addition to adequately capturing loss, can be readily measured for a given device. Here,  $R_{DS}$  was taken as  $R_{DS-ON}$  at the desired gate bias and temperature. The gate bias was driven by an external source from 0 V to the maximum allowed  $V_{GS}$  for the process, in this case 20 V.  $R_{DS}$  was determined by driving a known current into the drain and measuring the resulting  $V_{DS}$ . The remainder of the parameters,  $R_{OSS}$ ,  $R_{GATE}$ ,  $C_{OSS}$ , and  $C_{ISS}$  were measured with a series of two-terminal measurements on an impedance analyzer. Figure 4 shows the electrical configurations used for the measurements. DC bias of both  $V_{GS}$  and  $V_{DS}$  were controlled for the device under test via external voltage sources isolated by large series resistances. The capacitance and resistance were extracted from the measured impedance at each set of bias points. These results are small-signal values that can be used to reconstruct the large signal behavior of the device.<sup>3</sup> In order to minimize contact resistance and parasitic inductance

<sup>3</sup>This assumes that the device is behaving quasistatically during operation. These models have been experimentally validated at frequencies up to 110 MHz, in systems with important harmonics at 330 MHz.

TABLE II  
MEASURED DEVICE PARAMETERS

Parameter	MRF6S9060	Integrated LDMOS (F)
$R_{DS-ON}, V_{GS} = 8 \text{ V}, 25^\circ\text{C}$	175 m $\Omega$	200 m $\Omega$
$C_{OSS}, V_{DS} = 14.4 \text{ V}$	50 pF	132 pF
$R_{OSS}$	170 m $\Omega$	500 m $\Omega$
$C_{ISS}$	110 pF	275 pF
$R_{GATE}$	135 m $\Omega$	1300 m $\Omega$
$P_{TOT}$	213 mW	915 mW

in the measurement assembly, individual jigs were fabricated for each set of measured devices from 10-mil copper sheet that permitted repeatable attachment of the device to the impedance analyzer. The resulting set of data points permits accurate dynamic simulations with behavioral models in SPICE.

Equation 1 is a model for the total device loss under VHF operation. It captures loss in terms of a set of device parasitic parameters and a set of circuit derived parameters ( $K_1$ ,  $K_2$ ,  $K_3$ ).  $C_{EXT}$  is added in parallel with the output capacitance to control drain-source impedance, a technique often used in VHF converters [1], [7].  $K_3$  is shown for sinusoidal resonant gating, but will differ depending on the gate drive scheme (e.g. trapezoidal resonant gating [9]). The currents,  $i_{cond,RMS}$  and  $i_{disp,RMS}$  are circuit-dependent and may be found by SPICE simulation. In some converters such as the Class-E based converters, closed-form expressions exist that allow the direct calculation of the currents [10].

$$\begin{aligned}
 P_{TOT} &= P_{cond} + P_{cond-off} + P_{gate} \\
 P_{cond} &= K_1 \cdot R_{DS-ON} \\
 P_{cond-off} &= K_2 \cdot R_{OSS,eq} \cdot C_{OSS,eq}^2 \\
 P_{gate} &= K_3 \cdot R_{GATE,eq} \cdot C_{ISS,eq}^2
 \end{aligned} \tag{1}$$

$$\begin{aligned}
 K_1 &= I_{cond,RMS}^2 \\
 K_2 &= \left( \frac{I_{disp,RMS}}{C_{TOT}} \right)^2 \\
 K_3 &= 2(\pi \cdot V_{gate,AC-pk} \cdot f_{SW})^2
 \end{aligned}$$

$$C_{TOT} = C_{OSS,eq} + C_{EXT}$$

This formulation of VHF device loss is useful for optimization. It predicts device performance in a given circuit based on its parasitic component values (or vice versa).

In Equation 1 the non-linear capacitance and resistance elements in the device are approximated as linear. This approximation holds under two assumptions: First, that the device terminal voltages  $V_{DS}(t)$  and  $V_{GS}(t)$  are determined primarily by the external circuit. Second, that the form of the non-linearities does not change appreciably as a function of device width or layout. For instance, for a given  $V_{DS}(t)$  there is a current  $I_{disp}(t) = C_{OSS}(V_{DS}(t)) \cdot \frac{dV_{DS}(t)}{dt}$ . Under the above assumptions an equivalent linear capacitance,  $C_{OSS,eq}$ , can be defined for  $C_{OSS}(V_{DS})$  that gives the same RMS current,  $I_{disp,RMS}$ , as the non-linear capacitor under the drive voltage  $V_{DS}(t)$ . Off-state conduction loss then scales directly as the

square of  $C_{OSS,eq}$ , which in turn scales approximately with device width.

A similar procedure is undertaken to determine  $R_{OSS}$ .  $R_{OSS}$  in an LDMOSFET is primarily a function of  $V_{DS}$  (though the dependence is typically weak). The desire is to find an equivalent resistance,  $R_{OSS,eq}$ , that results in the same power dissipation that  $R_{OSS}$  exhibits under the drive current  $I_{disp}(t)$ . The power dissipation in  $R_{OSS}$  is:  $P_{disp} = \frac{1}{T} \int_T R_{OSS}(V_{DS}(t)) I_{disp}^2(t) dt$ . Thus,  $R_{OSS,eq} = P_{disp} / I_{disp,RMS}^2$ . Again, provided that  $V_{DS}(t)$  is not a function of  $R_{OSS}$  and the non-linearity is independent of device width or layout, off-state conduction loss scales linearly with  $R_{OSS,eq}$ , which in turn scales inversely with device width.

In this paper we evaluate devices in the integrated process in the context of a Class- $\Phi_2$  resonant boost converter switching at 50 MHz. This design has  $V_{IN} = 12$  V,  $V_{OUT} = 33$  V,  $P_{OUT} = 12$  W,  $C_{TOT} = 143$  pF,  $i_{disp,RMS} = 954$  mA,  $i_{cond,RMS} = 1040$  mA, and  $v_{gate,AC-pk} = 8$  V. To establish a performance baseline a discrete commercial RF LDMOSFET, the Freescale MRF6S9060, is compared to a custom LDMOSFET fabricated on an integrated BCD power process. Table II shows that the commercial part dissipates only 213 mW, while the integrated device loses 915 mW in the example application.

### III. LAYOUT OPTIMIZATION

#### A. Overview

The model presented in Section II provides a convenient goal function to optimize a device within the context of a particular circuit. In this case, we are looking to find an optimal device for a resonant soft-switched VHF converter, the Class- $\Phi_2$  converter, in particular. Once the circuit dependent constants have been selected, the device loss is only a function of the device parasitic parameters  $R_{DS-ON}$ ,  $R_{OSS}$ ,  $R_{GATE}$ ,  $C_{OSS}$ , and  $C_{ISS}$ . To affect a device optimization then requires that a device is changed in some way, the above parasitic parameters are computed relative to the change, and finally a new device loss is calculated from the model. The better device has smaller total loss.

Process, design rule, or layout (or some combination thereof) changes strongly affect the approach to an optimization method. While changing the process or design rules to better meet the requirements of VHF operation may offer substantial gains in performance, the large number of variables makes an optimization difficult and will come with a substantial cost.

Layout changes within the design rules, on the other hand, are relatively easy to accomplish. Not only is the total number of variables reduced, but the ability to rely on the scalability of the underlying device process means that the device parasitic parameters can be found largely through a set of simple scaling laws. While a change in layout offers the least room for a performance improvement, most integrated power device layout has been accomplished with a very different set of losses in mind. Typically the focus is on reducing specific on-resistance to minimize the total device area (and hence cost). The result is often a device with poor VHF characteristics, leaving much room for improvement.

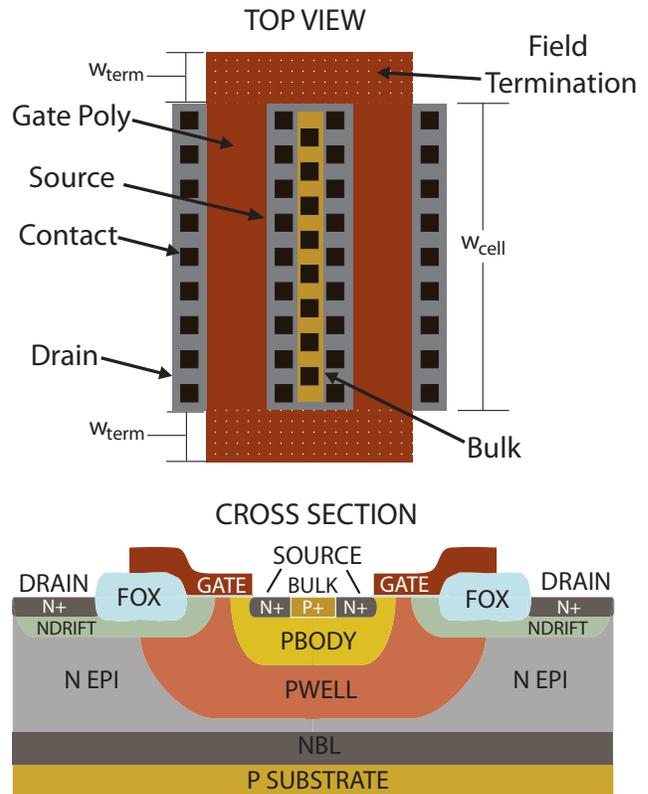


Fig. 5. The top view and cross-section of a single LDMOS cell. All the dimensions are fixed excepting  $w_{cell}$  which is scalable. The number of contacts also scales with cell width.

Even at the layout level, searching the entire range of possible layouts is impractical. Instead, we choose a layout pattern that is widely practiced for power devices as a starting point. Then the number of geometric variables is pared to a subset that has the largest influence over the device parasitic parameters and can be easily handled by a reasonably powerful computer. This set of geometric variables to be optimized completely describes a device when combined with the overarching layout pattern and the design rules.

#### B. Layout Description

Figure 5 and Figure 6 serve to illustrate the basic arrangement of the layout under consideration. In Figure 5 a top and cross section view of a single LDMOS cell is depicted. In the top view, all the horizontal dimensions are fixed by the process design rules. The only scalable dimensions are  $w_{cell}$  and  $w_{term}$ , each of which are variables in the optimization for reasons that will be discussed shortly. The other critical geometric variables of the cell, such as the lengths of the drain, source, and bulk diffusions, and the number of contacts are established by the design rules. For instance, each drain diffusion has a length equal to  $w_{cell}$ . The number of contacts in a drain diffusion is, in turn, set by the total length of the diffusion, the minimum allowable contact dimension, the contact to contact spacing requirements, and the diffusion-edge to contact spacing requirements. In this case, knowledge of one

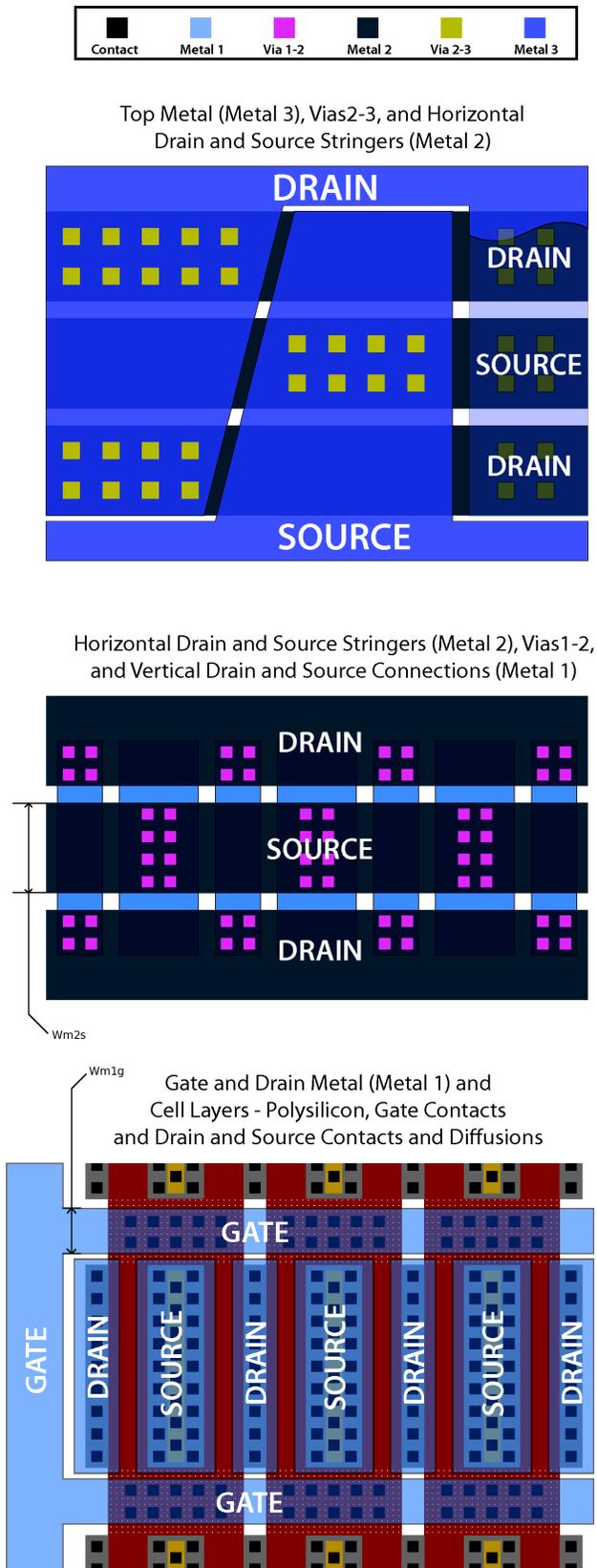


Fig. 6. Diagram showing cell-cell interconnection using the three metal layers in the process used to fabricate the power devices.

dimension,  $w_{cell}$ , very nearly describes a complete LDMOS cell, similar relationships are used to describe the entire device geometry with only a few variables.

The overarching layout pattern is depicted successively in Figure 6. It is effectively an array of cells with their gate, drain, and source/bulk terminals connected in parallel. At the bottommost portion of the figure is the cell layer. The cells are adjoined both vertically and horizontally in an array. The drain and source/bulk contacts of each cell are strapped by vertical segments of the metal-1 layer, while the gate contacts of each row of cells are connected by horizontal metal-1 stringers. The metal-1 stringers are strapped together at their ends to an array of gate pads (for bondwire attachment).

Moving to the middle section of the diagram, which is one layer higher, the cells are no longer depicted, but the vertical metal-1 straps remain. These are connected in parallel through vias to horizontal metal-2 stringers alternately forming drain and source buses.

Finally, the top layer consists of metal-3 straps that run vertically to connect the metal-2 drain buses in parallel and out to the drain and source pads (which would be located above and below the device respectively, but are not pictured). All of the devices fabricated for this work have between 1000 and 1800 cells, each with multiple rows and columns. In the case of multiple rows, drain and source metal-3 is only connected together at the top or bottom row.

With a layout picture in mind we can pare the number of geometric variables. For instance, for a 1000 cell device consisting of 20 rows and 50 columns, the number of metal-1 gate stringers and metal-2 drain stringers is fixed at 21, and the metal-2 source stringers must number 20. The length of the stringers is further fixed by choice of the minimum horizontal cell pitch.<sup>4</sup> Subsequently selecting a value for  $w_{cell}$  and the width of the metal-1 gate stringers,  $w_{m1g}$ , determines the device's overall aspect ratio, the active device area, the height of the metal-3 straps, the number of drain, source, bulk, and gate contacts, and the total width available to be shared among the metal-2 stringers. Choosing the width of the metal-2 source stringers,  $w_{m2s}$ , then specifies the width of the drain stringers and the total number and distribution of vias connecting metal-1 and metal-2. Finally, choosing the taper angle and the frequency of the metal-3 straps also specifies the number and location of the vias connecting metal-2 and metal-3.

Under the above considerations a complete device layout may be specified with only seven parameters: the effective device width,  $w_{cell}$ ,  $w_{m1g}$ , the aspect ratio, the number of metal-3 straps, the taper-angle of the metal-3 straps, the width of the metal-2 source stringer, and the number of gate bondpad arrays (see Table III).

### C. Choice of Layout Variables

The layout variables listed in Table III were chosen because they influence the device parasitic parameters in the model of

<sup>4</sup>While the minimum pitch is set by the design rules, a larger pitch could be chosen. However, this would only serve to increase total device area while simultaneously increasing capacitance and resistance, both negative effects.

TABLE III  
OPTIMIZATION PARAMETERS

Parameter	Importance to Device
Device Width	Sets intrinsic $R_{DS-ON}$ , overall device size
Cell Width	Affects $R_{GATE}C_{ISS}$ and $R_{DS-ON}C_{OSS}$
Aspect Ratio	Trades drain/source and gate metal losses
$w_{m1g}$	Trades $R_{GATE}$ and $C_{OSS}$ and $C_{ISS}$
# metal-3 cuts	Drain-source metal resistance
angle metal-3 cuts	Drain-source metal resistance
$w_{m2s}$	Drain-source metal resistance
# gate bondpad arrays	Trades $R_{GATE}$ and total device area

Section II, as well as describe a complete device. While other aspects of the layout geometry could be used as optimization variables (eg. the number of vias connecting the metal-1 drain and source straps to the metal-2 drain and source stringers) they either have a weak effect on overall device performance over reasonable variations of the parameter, or are already constrained by the selected set of variables. The following discussion serves to illustrate the rationale behind the choice of the optimization parameters.

The effective device width (referred to as "Device Width" in Table III) has a strong influence over the device's usefulness for a particular application. It places a lower bound on  $R_{DS-ON}$ , as this cannot be smaller than the intrinsic resistance. The same is true of the terminal capacitances, which must be at least as large as those of the cells without any surrounding metal. Since conduction loss will fall as the effective width rises and the frequency dependent off-state conduction and gating losses have the opposite behavior, this parameter plays a central role in finding an optimal device. Beyond this, as the overall device area scales, the metallization resistance will grow in importance.

Cell width plays a similar role. Each cell consists of a rectangular polysilicon region. The legs parallel to the drain contacts are effectively two LD MOSFETs that carry current, while the perpendicular legs serve to terminate the electric field and prevent premature breakdown at the ends of the channel. The field termination regions contribute to the cell input and output capacitance, but not to channel conductivity. As Figure 7 illustrates, this means that for a given intrinsic  $R_{DS-ON}$  we could either choose to make a device from a single cell or multiple cells with an equivalent total width. However, in the case of multiple cells, both  $C_{ISS}$  and  $C_{OSS}$  would be higher because the area occupied by the termination regions grows relative to the total area available for the channel. In addition, extra metallization required to connect both devices can contribute to a rise in  $R_{DS-ON}$ . An equally important consideration is the effect of cell width on gate resistance. A shorter cell will naturally have less gate resistance owing to the resistivity of the polysilicon. Further, for a given desired total effective width, shorter (and hence more numerous) cells allows for a larger number of gate stringers, which will lower the metal-1 contribution to gate resistance. Since rising gate resistance and lower capacitance per intrinsic  $R_{DS}$  are opposing trends, it is easy to imagine an optimum.

The overall device aspect ratio is important for its influence

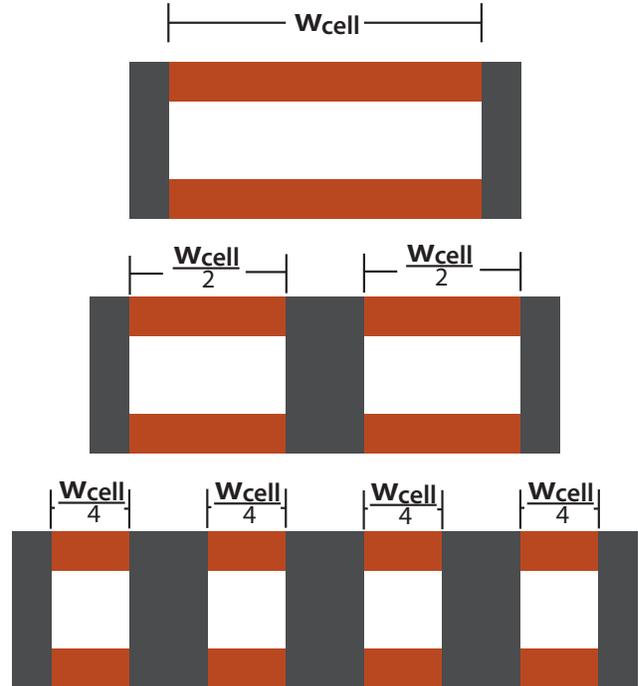


Fig. 7. The horizontal bars represent active gate polysilicon. These bars scale with  $w_{cell}$ . The vertical bars of the polysilicon terminations do not scale. They provide a constant amount of capacitance. As the number of cells at a given  $w_{cell}$  increases, the total area occupied by the terminations increases. This results in higher capacitance for a given  $R_{DS}$ .

on the drain and source metallization resistances. The cells might be stacked in a few rows of many columns or vice versa. For a device with few rows and many columns (high aspect ratio), the gate stringers are very long and relatively few, while the drain and source straps are short and numerous. Thus we might expect that the gate metal resistance in a high-aspect ratio device will be high and the drain-source metal resistance low. For low aspect ratio, the opposite situation attains, suggesting that there is an optimum aspect ratio.

The width of the metal-1 gate stringers,  $w_{m1g}$ , directly affects the gate metal resistance. An increase will lower the metal resistance, a typically dominant fraction of the total gate resistance in the devices considered here. However, this width cannot be increased without also increasing the width the field terminations,  $w_{term}$ , owing to the combined effects of the metal-1 to metal-1 spacing and the contact to metal-1 edge rules. Thus, increasing  $w_{m1g}$  increases the device capacitance relative to  $R_{DS-ON}$ , the length of the metal-3 drain and source straps, and the overall silicon area.

The taper angle of the metal-3 drain and source straps, as well as the total number of straps directly affect the overall resistance of the drain-source metal network. Figure 8 shows different metal-3 taper angles. When the drain-source straps are straight, the current density grows from the end of the strap moving toward the bondpad bus. Taper is added to equalize the current density along the metal-3 straps and lower loss. However, as the angle increases the number of vias between metal-2 and metal-3 is affected, and longer sections of metal-

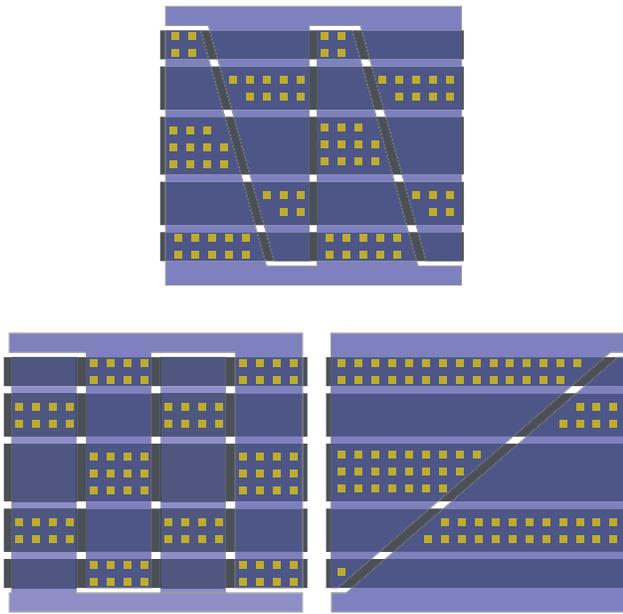


Fig. 8. Varying the angle of the metal-3 cuts affects loss. The bottom left show straight drain-source fingers which suffer from rising current density along their length. At the bottom right, the fingers are tapered reducing metal-3 loss, but metal-2 loss rises because maximum inter-contact spacing increases. The top layout shows an angle that compromises to reduce total metal loss.

2 are required to carry the current back to a metal-3 strap. This increases the metal-2 contribution to resistance, again because of rising current density, and an intermediate angle is desirable. A similar effect occurs as the number of straps is scaled. A higher strap count keeps the current density in the metal-2 layer smaller, but it also reduces the amount of metal-3 available for conduction due to the metal-3 to metal-3 spacing requirements. Of course, the strap-count and taper angle interact and require simultaneous optimization.

With the cell width and  $w_{m1g}$  set, the total width available for the metal-2 drain and source stringers is established. The relative proportion allotted to each is set by selecting the width of the metal-2 source stringer,  $w_{m2s}$ . This affects the distribution, and to a lesser extent the total number, of vias in the drain and source metal networks and can help to minimize the overall loss in the metal.

The final geometry parameter, the number of gate bondpad arrays determines the overall architecture of the device. A single array means that the gate stringers are only contacted out on one end, which is the worst case for gate metal resistance, but the most conservative in terms of die area. Adding another gate pad array at the opposite end of the device increases area but substantially reduces the gate metal resistance. Dividing the device with a third intervening gate pad array lowers the gate resistance even more. At some point further dividing the device gives almost no benefit, but adds substantial area. Overall, additional gate pad arrays allow the drain source network to maintain low resistance without penalizing the gate resistance.

One further point is that the number of bondwires is important when considering parasitic resistance and inductance.

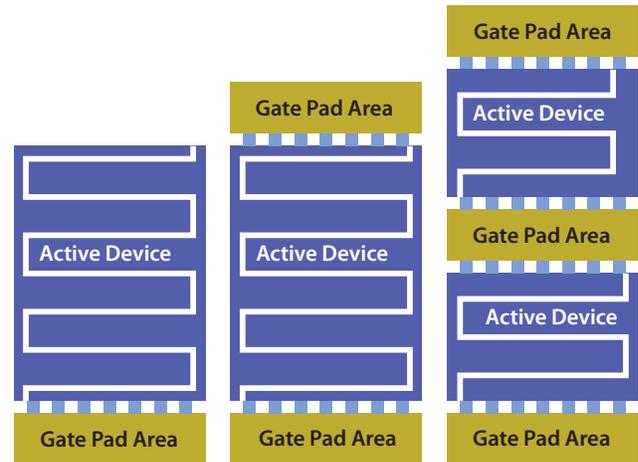


Fig. 9. The leftmost device has only one set of gate pads and correspondingly high gate resistance. Gate resistance is dropped in the picture at center by the addition of a set of pads at the opposite end of the device. On the right, an intermediate set of pads was added to reduce gate resistance further at the expense of more die area (not to scale).

The devices fabricated for this work were packaged in 28-pin TSSOPs with a heat spreader that served as the source contact. The drain was configured with 14-bondpads connecting to one side of the lead frame, the sources have the same number of pads bonded to the spreader, and the gates were bonded to the other side of the lead frame. However, some device configurations, such as very low aspect ratios, may not permit many parallel bondwires. Therefore a lower bound might be placed on the aspect ratio to avoid these problems. While this consideration arises if the devices are to be packaged and used as discretes, as they were here, it is not necessarily a concern if the device to be optimized is part of a co-packaged system. Since the overall goal of this work aims towards the latter scenario, bondwire limitations were only considered as a necessity of being able to work with sample devices rather than a requirement on the optimization.

#### D. Connecting Layout to Parasitics

Up to this point, we have presented a model to compute loss in terms of a set of device parasitic parameters. We also have a set of geometric variables that completely describe a device layout. What remains is to specify how to relate the two. This is accomplished with a combination of process scaling laws and in the case of the metal, circuit models.

Using scaling, the input and output capacitances can be cast in a simple form.  $C_{OSS}$ , for instance can be broken into several components. One portion scales linearly with the effective width of the device, another is fixed by the total area of the field terminations, and the remaining component comes from the capacitance between the drain and source metal. For a given cell, the linear portion arises both from the capacitance along the junction between the drift region and the body, and from the well to substrate capacitance. It is proportional to  $w_{cell}$ . The termination capacitance has the same origin, but depends on  $w_{term}$ . For  $C_{ISS}$ , the situation is nearly identical, with a fixed portion depending on  $w_{term}$ , a portion that scales

linearly with  $w_{cell}$ , and a contribution from overlap of the gate and drain metal. These relationships yield a simple set of equations scaling device capacitance in geometry:

$$\begin{aligned} C_{OSS} &= N \cdot C_{OSS,t} + N \cdot w_{cell} \cdot C_{OSS,l} + C_{md} \\ C_{ISS} &= N \cdot C_{ISS,t} + N \cdot w_{cell} \cdot C_{ISS,l} + C_{mg} \end{aligned} \quad (2)$$

where,  $N$  is the total number of cells,  $C_{OSS,t}$  and  $C_{ISS,t}$  are the per-cell termination input and output capacitances dependent on  $w_{term}$ ,  $C_{OSS,l}$  and  $C_{ISS,l}$  are the per-unit-length cell capacitances, and  $C_{md}$  and  $C_{mg}$  are the contributions due to metalization.

In general both the termination and linear capacitance terms can be calculated using process parameters and the inter-metal terms by keeping track of the overlapping area and using formulas such as those presented in [11]. For this process, there was enough information to calculate the input capacitance terms, but not the output terms (with the exception of the inter-metal portion, which is a relatively small fraction of the total). Therefore,  $C_{OSS,t}$  was ignored and  $C_{OSS,l}$  was approximated by measuring a sample device with a known layout, subtracting the metallization capacitance and dividing the resulting capacitance by the total effective width plus the total width of the terminations to arrive at a value for  $C_{OSS,l}$ .

The resistances of interest  $R_{DS-ON}$ ,  $R_{GATE}$ , and  $R_{OSS}$  can also be found in terms of layout geometry. However, each resistance has a component that relates to the metal interconnect and one that's due to the intrinsic LDMOS cell. This makes it difficult to write expressions similar to those for the capacitances because the equivalent resistance depends on the detailed current flow through the interconnect and the individual cells. The intrinsic component of  $R_{DS-ON}$  comes from the channel and access resistance of the cell. This is well controlled and can be easily related to the parameter  $w_{cell}$ . The intrinsic component of  $R_{GATE}$  is the access resistance to the source along with the resistance due to the gate polysilicon. In the case of  $R_{OSS}$ , the intrinsic component of resistance is related to the loss that occurs when displacement current is conducted through the access resistances at the drain and source of the device as well as the resistance through the substrate that is associated with the drain-substrate portion of  $C_{OSS}$ . The intrinsic resistance components of the cells can be found through simulation if the full process information is available. Otherwise, taking the difference between the measured values of  $R_{DS-ON}$ ,  $R_{GATE}$ , and  $R_{OSS}$ , and the extrinsic resistances due to the interconnect that are calculated as described below will allow an estimate of the intrinsic values. For instance, if we measure  $R_{DS-ON}$  and subtract the metal, bondwire, and leadframe resistances then the per-cell intrinsic resistance is found by multiplying the result by the number of cells. The same applies for  $R_{OSS}$  and  $R_{GATE}$ . These values are then used in the optimization.

The interconnect-related portions of the resistances come from the metal layout, bondwires, and leadframe. Among these, determining the resistance due to the metal layout requires the most effort. Here, the various portions of the

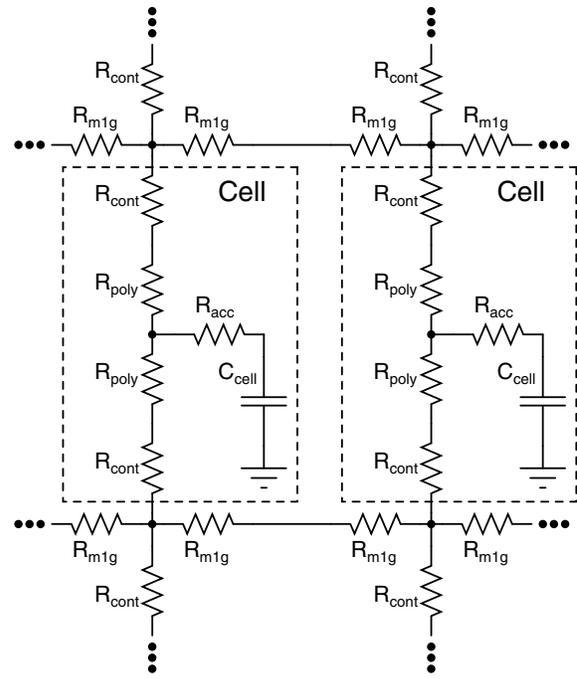


Fig. 10. Network modeling the gate interconnect and individual cell resistances.

interconnect resistance are calculated by approximating the metal layout as a network of resistors with values determined by the sheet resistance and shape of each metal layer segment. This simplification avoids the computational burden of a field solution, while providing results accurate enough for optimization work. The resulting resistor networks are used to populate a conductance matrix which is then solved for the equivalent resistance of the network under a dc current drive.

An example resistor network is illustrated in Figure 10. It is based on the gate metal layout depicted in Figure 6. The horizontal resistances labeled  $R_{m1g}$  represent the resistance along the metal-1 gate stringers between cells. This is easily found as  $R_{m1g} = \rho_{sheet} \cdot pitch_{cell} / w_{m1g}$ . The vertical resistances labeled  $R_{cont}$ ,  $R_{poly}$ , and  $R_{acc}$  are cell parameters.  $R_{cont}$  is the resistance from metal-1 through the contacts and into the poly. It is the resistance per contact over the total number of contacts per cell. Symmetry is exploited in this case, and no current is assumed to flow in the polysilicon across cell boundaries. Thus, while there are 10 contacts per cell to metal-1 intersection in the figure, only five are considered in calculating the value of  $R_{cont}$ . The total number of contacts is a variable depending on the choice of layout geometry and the design rules as described earlier.  $R_{poly}$  is the equivalent resistance of the polysilicon calculated for a steady-state sinusoidal drive current. The polysilicon is simply divided into two parallel RC ladder networks where R and C are determined for each segment by the sheet resistance of the polysilicon and the capacitance per unit area. An equivalent impedance is calculated and the real part is extracted as the equivalent resistance, while the imaginary part gives the cell capacitance. Again, symmetry is exploited, and the cell is cut

in half to find  $R_{poly}$  from either direction. Since the cell consists of two legs,  $R_{poly}$  is halved, and  $C_{cell}$  is doubled. Finally,  $R_{acc}$  is the access resistance from the source side of the cell.

Once the resistor network values are determined, a conductance matrix is populated and solved for the equivalent impedance of the entire gate network, the real part being the resistance.  $R_{GATE}$  is then found as the resistance calculated from the resistor network plus the resistance of the bondwires and leadframe.

A similar procedure is performed for the drain-source network. The resulting network is more complicated, but individual resistance values within the network are easily related back to simple geometric parameters such as cell-pitch, width of the metal-2 stringers, and the number of vias connecting adjacent layers of metal. In order to capture the dependence of the drain and source metal resistance on the cut angle of metal-3, it is necessary to represent these sheets of metal as a 2 dimensional grid of resistors. The granularity with which the network is divided into discrete resistances is arbitrary, but a fine mesh is computationally challenging and a course mesh is not accurate enough. It was found that one node per cell is adequate for the optimization performed here.

The final network includes both drain and source metal as well as the intrinsic cell resistances. This allows for the calculation of an equivalent drain-source resistance that includes the effects of an asymmetric layout.  $R_{DS-ON}$  is found by solving the nodal equations for a dc current drive at the drain with the source shorted to ground. During converter operation, current is either flowing through the interconnect network and the channel, or the interconnect network and the output capacitance. Therefore,  $R_{OSS}$  is found by the same method as  $R_{DS-ON}$ , with the exception that the resistors connecting the drain and source networks are substituted by the intrinsic value of  $R_{OSS}$ , rather than  $R_{DS}$ .

### E. Optimization

With the means to connect layout geometry to device loss, optimization is a relatively straightforward task. Since the set of geometry variables was kept small, a few thousand layouts can be evaluated in the space of an hour. At this rate, a brute force search of the layout space is easily accomplished, avoiding the pitfalls common to algorithms such as gradient descent. The primary challenge to setting up such an optimization is writing code that correctly accounts for the design rules and traps for non-physical situations as the various optimization parameters are varied.

A MATLAB script was created to perform the optimization. It takes various process parameters such as the resistivity of the metal layers and the intrinsic resistances and capacitances as inputs along with the circuit constants that represent the application the device will be optimized for. The code begins by loading the process design rules. It then sequentially permutes the seven geometry variables of Table III. For each set of variables, the code uses the design rules to arrive at a complete geometry, including the cell pitch, metal dimensions, contact and via descriptions, bondpad locations, and the various details

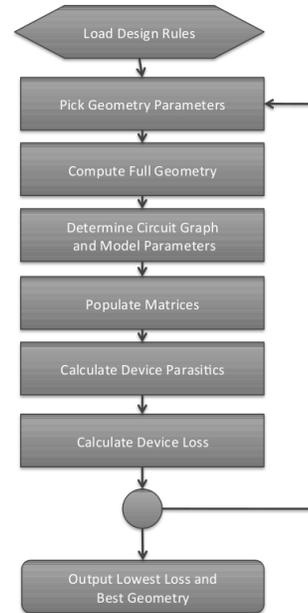


Fig. 11. Optimization flowchart

necessary to extract the device parasitic parameters. Once these dimensions are established, the capacitances can be calculated as described above. To calculate the resistances, the drain, source and gate networks must be created. The circuit graph differs for each set of parameters and is recreated for each geometry. For instance, as the aspect ratio changes the resistor network must change to reflect the varying locations of the cells, contacts, and vias. The individual resistances that represent a particular metal segment are then determined based on each segment's geometry and populated into three admittance matrices. One represents the drain and source metal, plus the intrinsic cell resistance, another the drain and source metal and the intrinsic  $R_{OSS}$  and the third the gate and source metal and intrinsic gate resistance. Once these are solved all five device parameters are available and the device loss is calculated and stored. On completion of the entire set, the device with the lowest loss is considered the optimum.

## IV. SAFE OPERATING AREA CONSIDERATIONS

Soft-switched converters are able to achieve high efficiency at VHF by avoiding voltage and current overlap in the switching device. The resulting switching trajectory closely follows the voltage and current axes for both turn-on and turn-off transitions. Figure 12 shows the simulated switching trajectories for a Class- $\Phi_2$  boost converter and an ideal hard-switched boost converter. In the Class- $\Phi_2$  converter the switch never has simultaneously high voltage and current, while under hard-switching the device experiences both high voltage and current simultaneously. The very different switch stress patterns that result have significant implications for the switch safe operating area as we will see shortly.

Hot carrier effects result from the accumulation of damage in a device caused by high energy carriers [11]–[15]. For

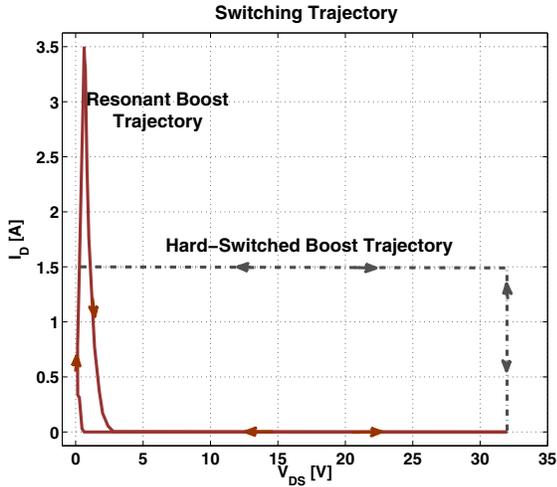


Fig. 12. Switching trajectory for Class- $\Phi_2$  Boost converter and an ideal hard-switched boost for the same voltage and power level.

LDMOS devices, hot carrier effects manifest as shifts in threshold voltage,  $V_{TH}$ , or  $R_{DS-ON}$ . Threshold shifts are generally the result of hot carriers becoming embedded in the gate oxide.  $R_{DS-ON}$  shifts arise as hot carriers create interface traps in any of the lightly-doped drain region, the accumulation region under the gate, and/or the bird's beak region, located at the tip of the FOX-gate interface area. There is some overlap among effects.

Under normal operation, a small number of carriers will attain the energy necessary to cause damage. Over time, the damage accumulates and eventually the shift in  $V_{TH}$  or  $R_{DS-ON}$  becomes severe enough that the device is no longer useful. As the local electric fields increase, a larger fraction of the carrier population has sufficient energy and damage accumulates more rapidly. The simultaneous condition of high current and high fields is particularly bad, and ultimately requires a restriction on the safe operating area (SOA) to prevent operation in regions that will dramatically shorten the service life of the device. For LDMOS power devices hot carrier reliability, SOA, and  $R_{DS-ON}$  are tradeoffs [11], [12] controlled primarily via the drain drift region. To reach a desired safe operating voltage, while ensuring reliability, the device must have certain minimum dimensions and a carefully controlled doping profile. The consideration of hot carrier reliability thus imposes a tax on device design in the form of higher parasitic capacitance for a given  $R_{DS-ON}$ .

In soft-switched VHF converters, device voltage and current are never simultaneously high. Without the conditions to create large numbers of hot carriers, device degradation does not occur, and we are free to extend the peak drain-source voltage towards the much higher avalanche limit. This extension of the SOA was validated through a set of experiments discussed in Section V. The result is significant in terms of VHF device performance. Without having to consider hot-carrier effects, device with a shorter drift region can be used. These devices will have substantially lower capacitance at a given  $R_{DS-ON}$ .

TABLE IV  
MEASURED DEVICE PARAMETERS

Device	$R_{DS-ON}$	$R_{OSS}$	$R_{GATE}$	$C_{ISS}$	$C_{OSS}$
MRF6S	175 m $\Omega$	170 m $\Omega$	135 m $\Omega$	50 pF	110 pF
F	200 m $\Omega$	400 m $\Omega$	1300 m $\Omega$	274 pF	132 pF
HV1	181 m $\Omega$	145 m $\Omega$	370 m $\Omega$	266 pF	126 pF
MV1	113 m $\Omega$	174 m $\Omega$	300 m $\Omega$	136 pF	97 pF
HV2	172 m $\Omega$	165 m $\Omega$	201 m $\Omega$	268 pF	127 pF
MV2	112 m $\Omega$	154 m $\Omega$	133 m $\Omega$	151 pF	108 pF

TABLE V  
CALCULATED LOSS COMPARISON

Device	Conduction	Displacement	Gating	Total
MRF6S	189 mW	18.9 mW	5.2 mW	213 mW
F	216 mW	310 mW	308 mW	835 mW
HV1	196 mW	102 mW	82.7 mW	381 mW
MV1	122 mW	72.9 mW	17.5 mW	213 mW
HV2	186 mW	118 mW	45.6 mW	350 mW
MV2	121 mW	79.9 mW	9.6 mW	211 mW

Since frequency dependent loss in VHF resonant converters is square-law dependent on capacitance, the efficiency improvements are significant, as can be seen in Table V.

## V. EXPERIMENTAL RESULTS

### A. Layout Optimization

Five LDMOSFETs fabricated in the same integrated power process are considered in this work. The process offers two different NLD MOS devices, one rated for 50-V operation, the other for 20-V operation. Three of the devices were fabricated using 50-V design rules, and the remaining two are built with a shorter drift region according to the 20-V design rules. Among the 50-V parts, the first sample device, which is designated the "F" device, was provided to assess the suitability of the process to operate in the VHF regime. The other two 50-V devices, designated HV1 and HV2 respectively, have optimized layouts. In the HV2 device, there is an additional copper layer used in place of metal-3. The 20-V devices, MV1 and MV2, were also designed with optimized layouts. They were fabricated specifically to test the hypothesis that hot carrier effects should be minimal under soft-switching. Like the HV2 device, the MV2 device has copper on the top layer. The five devices and their parasitic parameters are shown in Table IV.

The F, HV1, and HV2 devices have an effective width close to 7.2 cm. This was the as-provided width for the F device. The same width was chosen for HV1 and HV2 to provide a reasonable basis for comparison. Device optimization was performed on HV1 and HV2 as described above. Table IV shows that the optimization had the greatest effect on  $R_{GATE}$ , dropping from 1.3  $\Omega$  in the F-device to approximately 200 m $\Omega$  in the HV2 device. This is directly a consequence of changes to gate metal layout. The F-device has 13 1800  $\mu\text{m} \times 2.7 \mu\text{m}$  gate stringers connected to a gate pad array at one end of the device. In contrast, the HV1 device has 3 gate pad arrays. One pad array is located at each end of the device and the third splits it into two halves. The nine gate stringers in HV1 are nearly twice as wide and less than half as long at 800  $\mu\text{m} \times 5.7 \mu\text{m}$ . HV2 has a similar gate metal layout, but the top

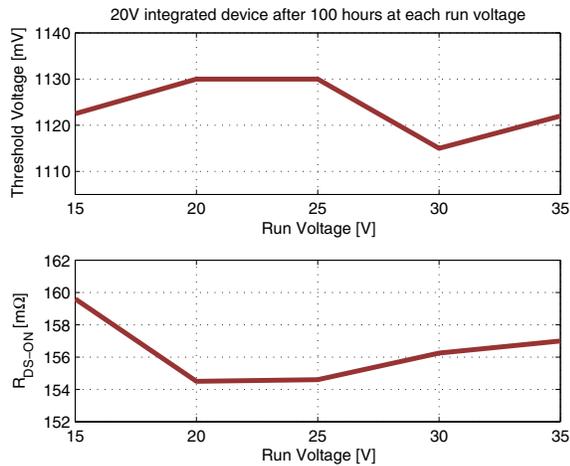


Fig. 13. The shifts in  $V_{TH}$  and  $R_{DS-ON}$  are well within the established testing criteria.

drain-source metal is copper allowing the device to be much more square (F and HV1 are about  $500 \mu\text{m} \times 2 \text{ mm}$ , where as HV2 is about  $1.1 \text{ mm} \times 1.3 \text{ mm}$ ). This doubles the number of gate stringers dropping the total gate resistance to  $201 \text{ m}\Omega$ .

The HV1 and HV2 devices also have  $35 \mu\text{m}$  cells in contrast with the F device's  $25 \mu\text{m}$  cells. This slightly reduces input and output capacitance, which also shows up in Table IV. It additionally allows for wider metal-2 conductors (the largest source of resistance in the drain-source metal for these high aspect ratio devices) in the drain source path. In conjunction with a somewhat shallower metal-3 angle in the HV1 device, a modest reduction in metal resistance was achieved, contributing to a lower  $R_{DS-ON}$ . In the HV2 device, metal-2 and metal-3 are paralleled to further reduce the contribution from the drain and source stringers, and copper is used in place of metal-3 for the topmost layer.

The overall reduction in loss among the 50-V devices from layout optimization alone is substantial, as Table V shows. The losses are calculated using the same example converter as in Section II. It should be noted that the F device is not a typical example of a power device in this process. The choice of high aspect ratio and short finger length was an initial attempt to achieve a device compatible with VHF operation for testing purposes. That fact that a full optimization allowed a further improvement of the  $R_{DS-ON} \cdot C_{OUT}$  product is encouraging. After layout optimization alone, the HV devices have a reduction in loss of up to 55%.

### B. Safe Operating Area

The MV1 and MV2 devices provide even better performance. These take advantage of 20-V design rules that allow for a shorter drift region and lower specific on resistance. When these devices are compared to the discrete MRF6S9060, in the example 50-MHz  $\Phi_2$  converter, they achieve the same total loss. This means that in the intended application at 50-MHz the integrated process can achieve parity with a discrete device picked from among the best available.

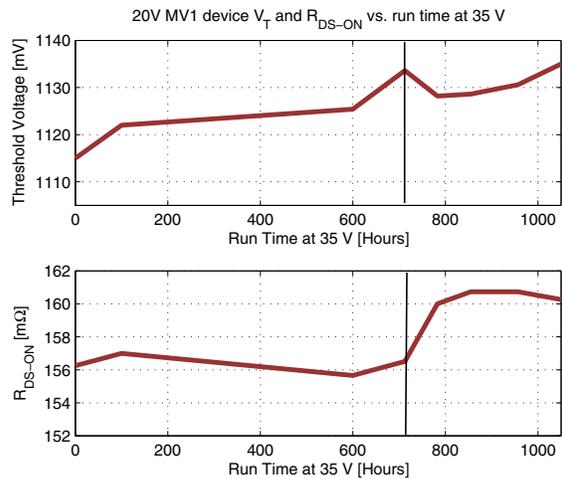


Fig. 14. After 1000 hours of operation at 35V, the 20V MV1 device has a total  $V_{TH}$  shift of around 20mV, and about a 4% change in  $R_{DS-ON}$ . The allowable maximums are 100mV and 10%, respectively.

While improved performance is expected from a device with a lower voltage rating, the point of interest is that it can be used in this application at all. In the experimental converters constructed to test these devices, the peak drain voltage attained during operation is 35 V, a 75% increase over the rated voltage of the MV1 and MV2 devices. As discussed in Section IV, the mechanism that underscores this ability is a switching trajectory that never has simultaneous high voltage and current. This minimizes hot carrier effects, allowing the MV1 and MV2 devices to be used at peak voltages closer to their avalanche voltage which is around 40 V.

To assess hot carrier reliability in this process under soft-switching we used the manufacturer's hot carrier reliability criteria. These require the device to run for 1 year at 10% duty ratio. To meet standards  $R_{DS-ON}$  must shift by 10%, or less, and  $V_{TH}$  by 100 mV, or less. In order to evaluate our devices, we ran the device in a Class- $\Phi_2$  resonant boost converter (see Figure 15 and Table VI) at successively higher voltages for 100 hour periods. The test started with a peak  $V_{DS}$  of 15 V. Once 35 V was reached, the converter was allowed to run for an additional 1000 hours. In terms of the manufacturer test this is more than adequate. Hot carrier damage occurs primarily at switching transitions. Since the test converter ran at 50 MHz, the total number of transitions substantially exceeds what would be expected of a hard-switched converter.

Testing began by measuring  $V_{TH}$  and  $R_{DS}$  of a new device, in this case an MV1 device. Threshold voltage was determined by holding  $V_{DS}$  at 100 mV and measuring the  $V_{GS}$  that results in a current density of  $0.1 \mu\text{A}/\mu\text{m}$ .  $R_{DS-ON}$  was measured with  $V_{GS} = 5 \text{ V}$  and  $V_{DS} = 100 \text{ mV}$ . Over the course of testing, the converter was periodically stopped and the device measured. The plots of Figures 13 and 14 show the accumulated results. Both the threshold voltage and on-state resistance lie well within the requirements. The total threshold shift was approximately 20 mV after 1000 hours of running with a peak  $V_{DS}$  of 35 V, and the shift in  $R_{DS-ON}$

was on the order of 4%. At 712 hours the input voltage to the converter was nearly doubled, stressing the devices and producing the steep rise in  $R_{DS-ON}$  demarcated by the black line in figure 14. Even with this additional stress, the total shift is well within the evaluation criteria.

As a control, a hard-switched boost converter was designed around an MV1 device to operate at the same voltage and power level. The converter was then connected to an electronic load so that average current through the switch could be maintained near 1.75 A, identical to the  $\Phi_2$  resonant boost converter when the peak  $V_{DS}$  is 35 V. After an initial run of 100 hours with a peak drain source voltage of 20 V, little change in  $V_{TH}$  or  $R_{DS-ON}$  was observed. After the initial run, the converter was then operated for 5 minute intervals at successively higher peak  $V_{DS}$ . This short interval was picked because shifts were expected to appear rapidly as the device voltage increased outside of the SOA. At a peak  $V_{DS}$  of 30 V, no changes were evident. Upon increasing the peak drain-source voltage to 35 V, the same voltage at which another MV1 device operated for over 1000 hours under soft-switching, the hard-switched device failed in 18 seconds.

The soft-switching trajectory that permits SOA extension may not exist in the  $\Phi_2$  converter (or other VHF resonant converters) if the converter is not operating in steady state. For example, a typical method of controlling VHF soft-switching converters is full on-off modulation. [9]. During the start-up and shut-down transients, the switching trajectory will not always closely follow the voltage and current axes. During these periods, it is necessary that the trajectory does not leave the SOA defined for hard-switched converters, or significant hot carrier damage could occur. To assess the feasibility of operating an SOA-extended 20-V switch under these conditions, a  $\Phi_2$  converter was configured for modulation. Under modulation, the entire power stage is turned on and off at a frequency far below the switching frequency. In this case, a 50-kHz signal was used to modulate a 50-MHz converter. After running the converter with a peak  $V_{DS}$  of 35 V for 120 hours, there was no measurable shift in either  $V_{TH}$  or  $R_{DS-ON}$ .

The benefits of extending SOA are clearly delineated in Tables IV and V. The MV devices enjoy a 76% reduction in loss over the original un-optimized F device. The primary benefit comes from the lower specific  $R_{DS-ON}$ . This results in substantially lower capacitance and devices with an active area roughly 20% smaller than the HV versions. The smaller dimensions also reduce the total interconnect length and the MV2 device, which has copper top metal and a small aspect ratio posts the lowest  $R_{GATE}$ , 133 m $\Omega$ . While the larger capacitances of the integrated devices over the discrete example (MRF6S9060) means that they won't scale as well in frequency, 50 MHz is sufficiently high to make converters with co-packaged energy storage a possibility.

### C. Converters

To illustrate the gains from device optimization and SOA extension, two 50-MHz Class- $\Phi_2$  resonant boost converters were constructed. The details are found in Table VI. One converter uses an un-optimized F device. The other uses the



Fig. 15. A Class- $\Phi_2$  boost converter built using the MV1 device and operated to 35V. It achieves 88% conversion efficiency at 12W,  $V_{IN}=12V$ ,  $V_{OUT}=33V$ .

TABLE VI  
EXPERIMENTAL DC-DC CONVERTER SPECIFICATIONS

Parameter	w/F LDMOSFET	w/ MV1 LDMOSFET
Device	50V rules	20V rules, 35V validation
Efficiency, $V_{IN} = 14V$	75%	88%
$V_{IN}$ Range	8-18V	8-16V
$V_{OUT}$	33 V	33 V
$P_{OUT}$	17 W	17 W
$D_1$	Fairchild S310	Fairchild S310
$L_F$	22 nH	43 nH
$L_{REC}$	56 nH	90 nH
$L_{2F}$	22 nH	22 nH
$C_{REC}$	47 pF	24 pF
$C_{EXT}$	56 pF	47 pF
$C_{2F}$	115 pF	115 pF

MV1 device, which is layout optimized and operated with an extended SOA to a peak drain voltage of 35 V. The converter using the F device achieves 75% conversion efficiency, and the converter with the MV1 device a substantially higher 88%. A photograph of the converter with the MV1 device appears in Figure 15.

## VI. CONCLUSION

Through optimization of device layout significant improvement can be gained for integrated power devices operating in the VHF regime. By further taking advantage of the switching trajectories inherent in soft-switched VHF designs, the hard-switching SOA for a device can be extended. This permits the use of devices at voltages higher than would otherwise be possible. Extending the reach of a power process under soft-switching allows designers of VHF converters to take advantage of lower specific on-state resistance and the attendant performance benefits. In the 50-MHz example presented here, device loss is reduced by as much as 75% when layout optimization and SOA extension can be used simultaneously. When un-optimized and optimized devices are compared in a VHF converter application, conversion efficiency rises from 75% to 88%, similar to what has been achieved using the best commercially available discrete LDMOSFETS.

The gains demonstrated here were achieved without modification to the process recipe or design rules. In this particular process, a range of devices with alternate design rules having better performance (lower specific  $R_{DS-ON}$ ) were dismissed

for hot carrier reliability considerations. Since these tradeoffs were made relative to hard-switching, it may be possible to achieve still better performance with a set of soft-switching specific design rules.

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