

# Filters With Inductance Cancellation Using Printed Circuit Board Transformers

Timothy C. Neugebauer, *Student Member, IEEE*, and David J. Perreault, *Member, IEEE*

**Abstract**—Capacitor parasitic inductance often limits the high-frequency performance of filters for power applications. However, these limitations can be overcome through the use of specially-coupled magnetic windings that effectively nullify the capacitor parasitic inductance. This paper explores the use of printed circuit board (PCB) transformers to realize parasitic inductance cancellation of filter capacitors. Design of such inductance cancellation transformers is explored, and applicable design rules are established and experimentally validated. The high performance of the proposed inductance cancellation technology is demonstrated in an electromagnetic interference (EMI) filter design.

**Index Terms**—Capacitor parasitic inductance, EMI filter, magnetic windings, printed circuit board, transformer.

## I. INTRODUCTION

CAPACITORS suffer from both resistive and inductive parasitics. At high frequencies, the equivalent series inductance (ESL) of a capacitor dominates its impedance, limiting its ability to shunt high-frequency ripple current.

For example, large electrolytic capacitors often start to appear inductive below 100 kHz, large valued film capacitors become inductive in the 100 kHz–1 MHz range, and small-valued film capacitors and large ceramic capacitors typically become inductive in the 1–10 MHz range. Capacitor parasitic inductance has a significant impact on filter performance [1], resulting in larger, more expensive filters than would otherwise be possible.

This paper explores a new filter design technique that overcomes the capacitor parasitic inductance that limits filter performance at high frequencies. The technique, originally proposed in [2], is based on the application of coupled magnetic windings to effectively cancel the parasitic inductance of capacitors, while introducing inductance in filter branches where it is desired. This paper focuses on the use of air-core printed circuit board (PCB) transformers to realize parasitic inductance cancellation of filter capacitors. As will be shown, the design approach explored here can provide dramatic improvements in filter performance without impacting the filter size or cost.

The paper is organized as follows. Section II introduces the use of coupled magnetic windings to overcome capacitor parasitic inductance. Section III explores the design of PCB transformers for this application, including a comparison of winding

Manuscript received May 29, 2003; revised September 30, 2003. Recommended by Associate Editor T. Lebey. This paper was presented at the Power Electronics Specialists Conference, Acapulco, June 2003. This work was supported by the United States Office of Naval Research under ONR Grants N00014-00-1-0381 and N00014-02-1-0481.

The authors are with the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: neugebaut@mit.edu).

Digital Object Identifier 10.1109/TPEL.2004.826425

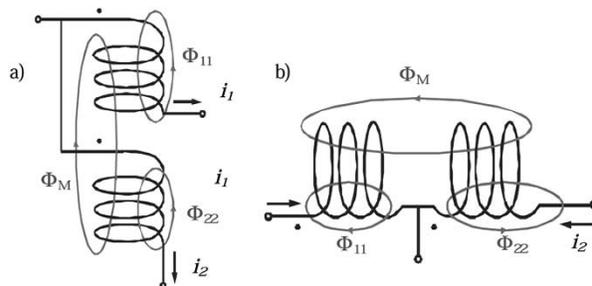
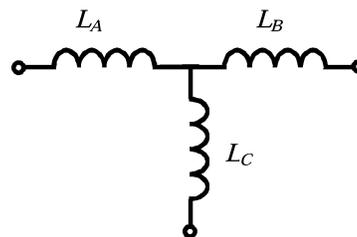


Fig. 1. (a) End-tapped and (b) a center-tapped connection of coupled magnetic windings.



	$L_A$	$L_B$	$L_C$
End-tapped	$L_M$	$L_{22}-L_M$	$L_{11}-L_M$
Center-tapped	$L_{11}+L_M$	$L_{22}+L_M$	$-L_M$

Fig. 2. Equivalent circuit model for the configurations of Fig. 1.

topologies and the development of analytical and computational methods for transformer design. Section IV presents an experimental evaluation of the proposed design approach and explores the impact of second-order effects on the repeatability and sensitivity of filters with inductance cancellation. The design and evaluation of an EMI filter using the proposed technology is addressed in Section V. Finally, Section VI concludes the paper.

## II. INDUCTANCE CANCELLATION

Here we introduce how magnetically-coupled windings can be used to cancel the effects of capacitor parasitic inductance. Fig. 1 illustrates two possible connections of coupled magnetic windings, which we hereafter refer to as “end-tapped” and “center-tapped” connections. Fig. 2 shows an equivalent circuit model applicable to either connection of coupled windings; this model is referred to as the “T” model of the coupled windings. Also shown are the appropriate model parameters for the two connections, in terms of their self and mutual winding inductances. In either connection, appropriate values of self and mutual inductances lead to a negative equivalent inductance in one leg of the T model. It is this “negative inductance”

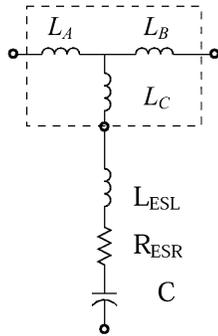


Fig. 3. Application of coupled magnetic windings to cancel the series inductance of a capacitor. Capacitor ESR and ESL are shown explicitly, along with the equivalent T model of the magnetic windings.

effect that is utilized to nullify the parasitic inductance in filter capacitors.

The negative inductance effect arises from electromagnetic induction between the coupled windings. We emphasize that the negative inductance in the T model does not violate any physical laws. Only one leg of the T model has a negative inductance, and the total inductance seen across any winding is—as expected—the positive-valued self inductance of the winding. Nevertheless, the negative equivalent inductance in one notional branch path can be used to great effect in the design of filters.

Fig. 3 shows the application of coupled magnetic windings to a capacitor whose equivalent series inductance (ESL) is to be cancelled. We model the coupled windings with the T network of Fig. 2, and model the capacitor as a series connection of an ideal capacitor, inductor and resistor. When the T-model branch inductance  $L_C$  is chosen to be negative and close in magnitude to  $L_{ESL}$ , a net branch inductance  $\Delta L = L_C + L_{ESL} \approx 0$  results. The combined network is very advantageous in terms of its ability to shunt high-frequency currents into the capacitor branch path. A near-zero impedance in this path (limited only by ESR) is maintained out to much higher frequencies than is possible with the capacitor alone. Furthermore, equivalent inductances  $L_A$  and  $L_B$  serve to increase the order of the filter network over the capacitor alone, further improving filter performance. This approach differs from previous use of coupled magnetic windings in filters (see, e.g., [3]–[9]) in that the coupling of the windings are utilized to cancel the effects of parasitic inductance in the capacitor and interconnects, thus permitting dramatic improvements in filtering performance to be achieved.

### III. TRANSFORMER DESIGN

Typical filter capacitors have ESL values that are in the tens of nanohenries, with a repeatability among units of a few percent. For example, Fig. 4 shows the measured ESL of a large number of 0.22  $\mu\text{F}$  X-type EMI filter capacitors (Beyschlag Centrallab 2222-338-24-224 0.22  $\mu\text{F}$ , 275 Vac). The mean ESL of these capacitors is 16.81 nH with a standard deviation of only 112 pH. Thus, inasmuch as appropriate inductance cancellation magnetics can be realized, tremendous reductions in the effects of capacitor parasitic inductance can be achieved.

Design of the inductance cancellation transformer is the most critical aspect of realizing high-performance induc-

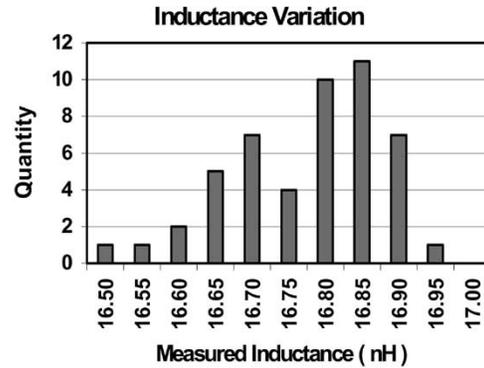


Fig. 4. Histogram of the parasitic inductances found for Beyschlag Centrallab 2222 338 24 224 X-type capacitors (0.22  $\mu\text{F}$ , 275 Vac). The average value is 16.81 nH, with a standard deviation of 112 pH.

tance-cancelled filters. The inductance and coupling of the magnetic windings must be very precisely controlled in order to accurately cancel the effective inductance of the capacitor. Furthermore, these characteristics must be repeatable from unit to unit, and must be insensitive to operating conditions. Air-core transformers printed directly in the circuit board offer these characteristics. Printed windings provide an extremely high degree of repeatability: in the absence of substantial amounts of magnetic material the inductances are purely a function of geometry (making them insensitive to operating condition). Furthermore, to the extent that the PCB space beneath the capacitor can be utilized to implement the inductance-cancellation transformer, there will be no increase in filter size or cost.

In this section, we address the design of printed PCB transformers for realizing inductance cancellation of filter capacitors. We first consider analytical and computational methods for sizing the printed circuit board windings. We then provide a comparison of winding topologies for inductance cancellation transformers.

#### A. Winding Topology

The two transformer topologies shown in Fig. 1 (which we term end-tapped and center-tapped) are useful for realizing inductance cancelled filters. In order for an end-tapped transformer to be effective the mutual inductance of the two windings must exceed the self-inductance of one of the windings<sup>1</sup>. This requirement usually results in one winding that consists of only one turn and another winding that consists of many turns. Since the first winding has only one turn, the trace width is usually designed to be large in order to minimize shunt-path resistance. As illustrated in Fig. 2, the cancellation term depends on both the self-inductance of the single-turn coil and the mutual inductance of the coils being accurate. Center-tapped transformers are easier to design. To be effective, a center-tapped transformer only needs to have windings with a controlled mutual inductance. There are no restrictions on the relative sizes of the two windings, either in terms of total inductance or impact on shunt-path resistance. Because of this, the center-tapped transformer provides more design flexibility.

<sup>1</sup>The mutual inductance is, of necessity, less than the geometric mean of the two self-inductances [2].

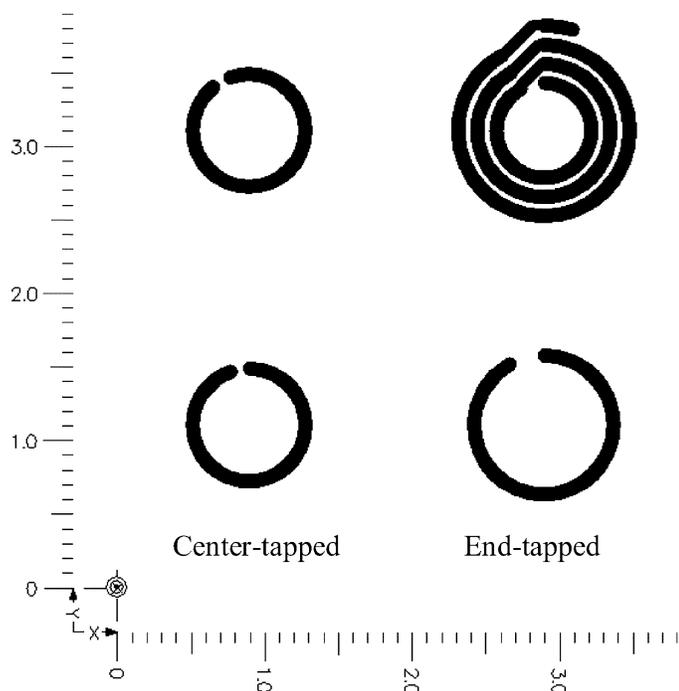


Fig. 5. Examples of center-tapped and end-tapped transformers. These are the transformers used for Table I. The left column has the top and bottom-side traces of the center-tapped transformer as viewed from the top side. The right column has the top and bottom-side traces of the end-tapped transformer as viewed from the top side. Length marks are in inches.

The physical size and characteristics of the transformer depend on the choice of winding topology. In an end-tapped transformer the mutual inductance must exceed the self-inductance of the first coil,  $L_{11}$ , by the amount of inductance to be cancelled. By contrast, the magnitude of the mutual inductance in the center-tapped topology only needs to equal the cancellation value. The mutual inductance must therefore be significantly larger in an end-tapped transformer design than in a center-tapped design. End-tapped designs thus require more turns (and have higher winding self inductance) than corresponding center-tapped designs. Furthermore the low-inductance winding in an end-tapped design should have a relatively wide trace width so as not to introduce excessive shunt-path resistance. Ultimately, the total board area needed for an end-tapped transformer can be significantly larger than that needed for a center-tapped design.

End- and center-tapped designs also differ in that end-tapped designs tend to result in asymmetric branch impedances (e.g.,  $L_B > L_A$  in Fig. 2), whereas center-tapped designs may be either symmetric or asymmetric. The asymmetry in end-tapped designs arises from the need to have  $L_{22}$  much larger than  $L_{11}$  such that the mutual inductance will be sufficiently high for reasonable coupling values within the constraint

$$L_{11} < L_M < \sqrt{L_{11} \cdot L_{22}} < L_{22}. \quad (1)$$

The relatively large inductance and asymmetry found in end-tapped designs are not always disadvantageous, particularly if the large branch inductance can be exploited as part of a filter or converter.

To illustrate these effects, both a center-tapped and an end-

TABLE I  
COMPARISON OF AN END-TAPPED AND A CENTER-TAPPED TRANSFORMER.  $R_{11}$  IS THE RESISTANCE OF THE FIRST COIL AND  $R_{22}$  IS THE RESISTANCE OF THE SECOND COIL.  $L_M$  IS THE MUTUAL INDUCTANCE AND  $L_C$  IS THE SHUNT INDUCTANCE SHOWN IN FIG. 2. AREA IS THE MAXIMUM AREA NEEDED BY ONE OF THE COILS. THE TRANSFORMERS ARE RATED FOR A dc-PATH CURRENT OF 6 AMPS

	End-tapped	Center-tapped
$R_{11}$	1.45 m $\Omega$	1.17 m $\Omega$
$L_{11}$	46.96 nH	35.71 nH
$R_{22}$	4.348 m $\Omega$	1.17 m $\Omega$
$L_{22}$	251.4 nH	35.71 nH
$L_M$	68.54 nH	21.44 nH
$L_A$	68.54 nH	57.15 nH
$L_B$	182.86 nH	57.15 nH
$L_C$	-21.58 nH	-21.44 nH
Area	1.286 in <sup>2</sup> (829.7 mm <sup>2</sup> )	0.608 in <sup>2</sup> (392.3 mm <sup>2</sup> )

tapped transformer were designed and compared using the magnetic modeling tool FastHenry [10]. Fig. 5 shows the layout of these planar transformers. The transformers were designed to compensate for a capacitor parasitic inductance of 21.5 nH, and to provide a dc current path rating of 6 A. The characteristics of the two transformers are listed in Table I. It can be seen that the end-tapped transformer takes up twice the board area of the center-tapped design. Also, for the same negative inductance in branch C (Fig. 2), it has larger, more asymmetric inductances in the remaining branch paths than does the center-tapped design.

There are also second-order differences between center-tapped and end-tapped winding designs. One design consideration is the sensitivity of the transformer to a nearby metal sheet (e.g., a ground plane or metal chassis). This factor is addressed in a later section, but the results show that center-tapped transformers are somewhat less sensitive to this kind of effect. Another consideration is frequency dependence of the cancellation. As frequency increases the inductance of the coils will change slightly. Specifically, the magnitudes of all the inductances will decrease due to skin and proximity effects. For a center-tapped transformer the effective negative inductance magnitude will decrease at higher frequencies, while the negative inductance magnitude for an end-tapped transformer can increase at higher frequencies. This occurs when the self-inductance,  $L_{11}$ , decreases at a faster rate than the mutual inductance. Thus, winding topology can impact second-order frequency dependencies. Nevertheless, this frequency dependence is very small and its presence has not yet been fully evaluated or exploited.

### B. Inductance Cancellation Winding Design

In order to maximize the benefit of inductance cancellation the transformer needs to be designed with a high degree of accuracy. Here we outline analytical, computational, and empirical means for designing and refining PCB inductance cancellation transformers. The first step is to determine the inductance to cancel. The parasitic inductance due to the capacitor itself should be measured, and the additional stray inductance associated with the connection of the capacitor in the circuit should

be measured or estimated. The transformer is designed to compensate for the total inductance in the capacitor path.

The transformer can be designed after the inductance to cancel has been determined. Several characteristics of the transformer can be defined based on the following properties: The coils will have a height determined by the standard weight of copper used on the board. The trace widths are sized to handle the ac and dc currents for the application, routinely fifty mils to several hundred mils ( $\sim 1\text{--}5$  mm). The spacing between layers will be equal to the layer or board thickness, normally 62 mils (1.6 mm) for two-layer boards. The additional board area used by the transformer can be minimized by placing it under the capacitor.

In order to design an appropriate transformer one needs to predict the self and mutual inductance of the printed windings. We have explored three methods for calculating the inductances of a specified geometry. The first method exploits analytical expressions based upon the electromagnetic system in question. The second method utilizes empirical formulas derived from measured data. The last method employs numerical techniques for calculating inductance.

Papers have been published (e.g., [11] and [12]) which derive formulas for determining the self and mutual inductances of flat circular loops of various diameters. We have found that the most accurate prediction for this application is that of [12]. The formula for mutual inductance of circular traces is

$$M_{12} = \frac{\mu_0 \pi}{h^2 \ln\left(\frac{r_2}{r_1}\right) \ln\left(\frac{a_2}{a_1}\right)} \int_0^\infty S(kr_2, kr_1) \cdot S(ka_2, ka_1) \cdot Q(kh) \cdot e^{-k|z|} \cdot dk \quad (2)$$

$$S(kx, ky) = \frac{J_0(kx) - J_0(ky)}{k} \quad (3)$$

$$Q(kh) = \frac{2}{k} \left( h + \frac{e^{-kh} - 1}{k} \right) \quad (4)$$

where  $h$  is the copper thickness,  $r_2$  and  $r_1$  are the outer and inner radii of coil 1,  $a_2$  and  $a_1$  are the outer and inner radii of coil 2, and  $z$  is the relative vertical displacement of the loops.  $J_0$  is a Bessel function of the first kind with order 0.  $M_{12}$  is the mutual inductance between coils 1 and 2. The self-inductance is the mutual inductance of a coil with itself.

Empirical formulas are also commonly used for determining inductances (e.g., [13]–[16]). These formulas generally share a common form, but have various constants that differ depending on the characteristics of the coils that were studied in developing the models. We have developed empirical formulas for the self and mutual inductances of planar rectangular (spiral) coils of a size range that is typical for inductance cancellation windings. Rectangular geometry windings are of interest because they are easy to lay out on a printed circuit board. The empirical formulas described in Appendix A are based on numerical predictions, and have been validated against experimental results. They enable fast approximate sizing of rectangular windings<sup>2</sup>.

<sup>2</sup>It should be pointed out that the empirical and analytical equations fail to capture the field shielding of the outer turns due to the inner turn trace conductors. As a result, the accuracy of the equations tends to diminish for large numbers of turns.

TABLE II  
COMPARISON OF VALUES AS CALCULATED OR MEASURED USING A VARIETY OF SOURCES. THE TRANSFORMER CONSISTS OF TWO SINGLE TURN COILS WITH RADII (TO THE TRACE CENTER) OF 510 MILS ( $\sim 13$  MM) AND TRACE WIDTH OF 100 MILS (2.54 MM)

Source of Inductance Value	Inductance of Circular Coil 1	Inductance of Circular Coil 2	Mutual Inductance of Circular Coils
Measured	46.25 nH	44.7 nH	23 nH
Zierhofer [11]	36.8 nH	36.8 nH	46.6 nH
Hurley [12]	58.2 nH	58.2 nH	38 nH
FastHenry [10]	57.4 nH	57.4 nH	37 nH

Another method to obtain inductance for arbitrary winding patterns is to use a three-dimensional field solver such as INCA3D<sup>3</sup> from CEDRAT or a freeware program, FastHenry [10]. FastHenry, the tool utilized here, can calculate the self and mutual inductances of any three-dimensional air-core winding geometry. These programs allow for arbitrary winding patterns and provide fairly accurate results.

To design an inductance cancellation transformer we use either empirical or analytical formulas to develop a coil design. The design is then refined using numerical computational tools. The formulas for inductances provide a quick method to obtain reasonably accurate designs and show how various parameters of the windings affect the inductances. The numerical software then provides a greater degree of accuracy for the implementation. A comparison of the results from various methods for an example coil pair is shown in Table II.

### C. Design Refinement

Ideally, given good measurements of the parasitic inductance and an appropriate transformer design, the system should have little or no inductance in the shunt path. Unfortunately, the methods used to determine the parasitic inductance and the transformer's T-model parameters are often in error by several nanohenries, a significant amount in such systems! To provide the best cancellation, we routinely add an additional iteration in which a prototype is developed and design refinements are made. We have successfully used three methods to refine transformer design. Here we describe each of these in turn.

The first method of experimental refinement involves fabricating a prototype board incorporating a transformer with multiple tap points. Instead of connecting the cancellation transformer to the remainder of the circuit, the windings are terminated with a set of jumpers or pads at different positions<sup>4</sup>. The connection of the transformer to the remainder of the circuit is made afterwards, with the best connection point determined empirically. The connection method is also important: it should be done in a manner that can be replicated with a printed circuit trace in the final design (e.g., by using a wire or foil link). After the best termination position has been determined, the final board can be built with a printed connection trace.

<sup>3</sup>INCA3D is a product of the Laboratoire d'Electrotechnique de Grenoble. INCA3D is distributed by CEDRAT and its distributor network.

<sup>4</sup>A continuous tap can be implemented by eliminating the solder mask over the winding.

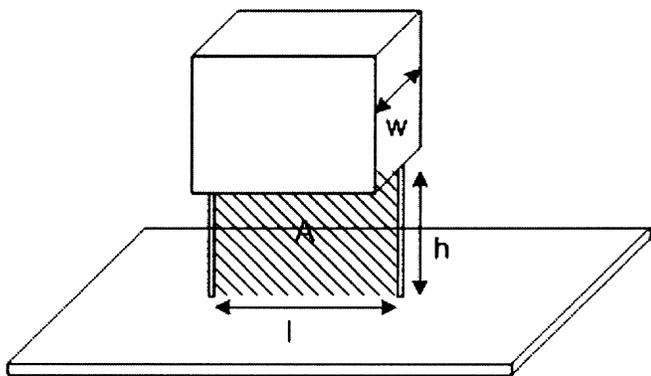


Fig. 6. Parasitic inductance created by lifting the capacitor off the board can be approximated using  $l$ ,  $h$ ,  $w$ , and  $\mu_0$ .

The second refinement method also involves fabricating a prototype board. In this case, a range of printed transformers are fabricated, each with different predicted characteristics (e.g., with predicted negative inductances spaced evenly over a range.<sup>5</sup>) The transformers are designed with identical interconnects to the external circuit, but with slightly varying coil dimensions [e.g., as determined using (2)–(4)]. One of the fabricated sets will provide the best performance, while the others either over- or under-compensate the parasitic inductance. The best transformer and its interconnect pattern (including ground plane, etc.) is then used in the actual design.

The final refinement method is useful when a first-pass design overcompensates the shunt inductance, resulting in a net negative shunt-path inductance. If the capacitor is elevated off the board (i.e., with increased lead length) the shunt path inductance will increase. At some height off the board,  $h$ , the shunt path inductance will be minimized. The additional inductance introduced by the leads can then be estimated [17]

$$\Delta L \approx \mu_0 \cdot \frac{h \cdot l}{w} \quad (5)$$

where the variables  $w$ ,  $h$ , and  $l$  are as defined in Fig. 6<sup>6</sup>. Once the error has been quantified the transformer can be redesigned for an incremental change in shunt path inductance of the desired amount.

#### IV. EXPERIMENTAL EVALUATION AND TESTING

This section presents an experimental evaluation of the proposed design approach and explores the impact of second-order effects on the repeatability and sensitivity of filters with inductance cancellation. It will be shown that filters incorporating printed PCB cancellation windings can be made highly repeatable. Furthermore, the sensitivities to ground planes and other nearby conductors and to magnetic materials are quantified, and found to be low for a wide range of conditions.

Fig. 7 shows a test setup for evaluating the efficacy of inductance cancellation. The device under test (DUT) may be a capacitor with an inductance cancellation transformer or may be

<sup>5</sup>This approach is particularly effective with circular spiral windings designed using the analytical formulas (2)–(4).

<sup>6</sup>This approximation is based on the assumption that the incremental inductance introduced by raising the capacitor stores energy entirely in the gap between the capacitor and the board.

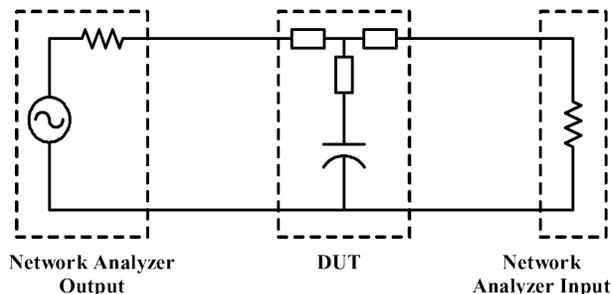


Fig. 7. Experimental setup for evaluating filters and components incorporating an Agilent 4395A network analyzer. The device under test (DUT) comprises of a filter capacitor and a printed circuit board inductance cancellation transformer with their interconnects.



Fig. 8. Test comparison board. A capacitor without inductance cancellation is in the upper right corner. Every other layout has a transformer with a different shunt path inductance.

an entire filter. The DUT is driven from the 50  $\Omega$  output of a network analyzer. As the driving point impedance of the DUT is always much less than the output impedance of the network analyzer, the drive essentially appears as a current source. The response at the output port of the DUT is measured across the 50  $\Omega$  input of the network analyzer. The test thus measures the output response of the DUT due to an input current. This is an effective measure of the attenuation capability of the DUT.

To validate the proposed approach and to illustrate how variations in inductance cancellation impact performance, a set of center-tapped transformers having a wide range of mutual (cancellation) inductances were designed (Fig. 8) for an X-type filter capacitor (Beyschlag Centrallab 2222-338-24-224 0.22  $\mu\text{F}$ , 275 Vac). The design approach of Section III was followed. The transformers were designed using (2) and the designs were verified with the program FastHenry. The effects on filter performance of different amounts of mutual (cancellation) inductance is shown in Fig. 9 (using the test setup of Fig. 7). The highest curve in both Fig. 9(a) and (b) represents the capacitor used in a typical fashion without inductance cancellation. The curves in Fig. 9(a) are the results for transformers with mutual inductances that are less than

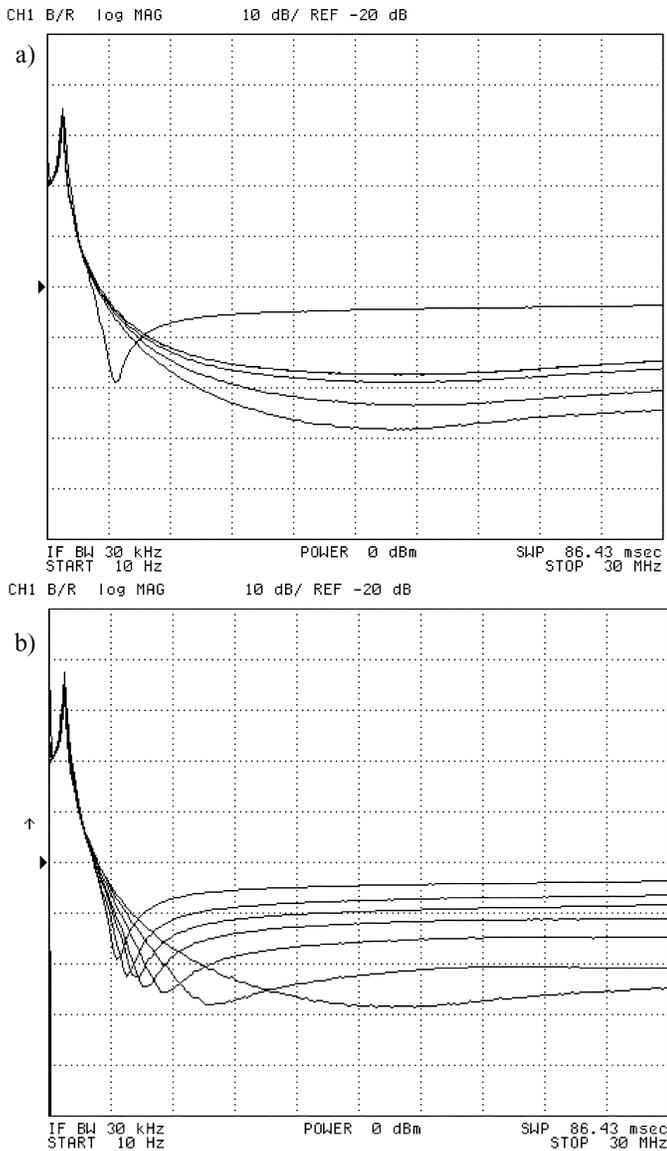


Fig. 9. Highest curve in both (a) and (b) represents the performance of a capacitor without any inductance cancellation in the test setup of Fig. 7. The curves in (a) are the results with center-tapped transformers having mutual inductances between 6 nH and 26 nH at intervals of 4 nH each. (b) The results of having a mutual inductance that is too large; these curves are the results with transformers having mutual inductances between 26 nH and 32 nH with intervals of 2 nH.

the total shunt-path inductance (between 6 nH and 26 nH at intervals of 4 nH each). Fig. 9(b) shows the results of having a mutual inductance that is too large; these curves are the results of transformers with mutual inductances between 26 nH and 32 nH with intervals of 2 nH. Note that the measured parasitic inductance of the capacitor alone (Fig. 4) is 10 nH lower than the design value of the cancellation transformer that provides the best performance ( $\sim 26$  nH). This reflects additional interconnection inductance along with limitations in our ability to precisely predict inductance. We may conclude from these results that correct implementation of inductance cancellation can provide large performance improvements (more than a factor of 10 improvement in attenuation across a wide frequency range for the cancellation transformer with the best matching). To achieve this, however, parasitic inductance

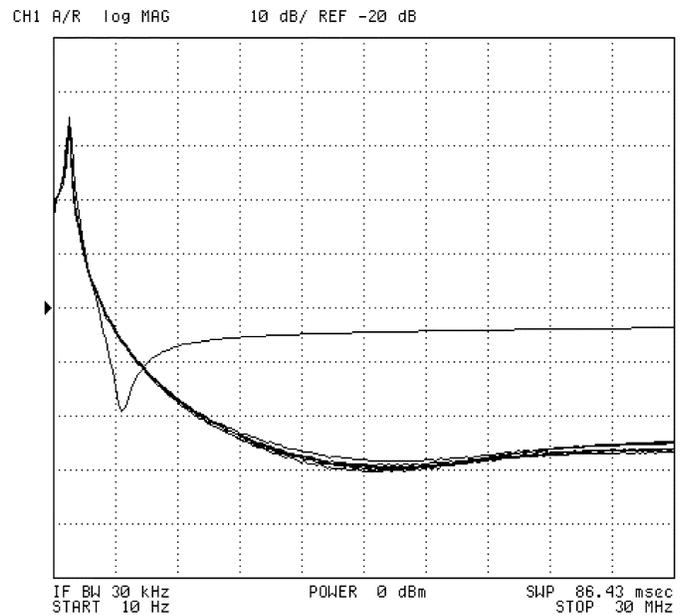


Fig. 10. Repeatability curves. The higher curve is a capacitor alone (no cancellation). The lower curves are results with six nominally identical circuits incorporating printed cancellation windings. Note that the curves are all within 3 dB of each other.

estimation (measurements and calculations) must be done very accurately, and must include all interconnect inductance in the desired configuration.

In order for the proposed inductance cancellation technique to be practical, the cancellation must be highly repeatable. It has already been demonstrated that the equivalent series inductance of off-the-shelf film capacitors can be very repeatable (similar results were found for electrolytic capacitors in [2]). Furthermore, one can reasonably expect that printed air-core transformers will provide very repeatable inductances, since inductance is only a function of tightly controlled geometric factors in this case. Here we demonstrate that inductance cancellation using printed circuit board transformers is highly repeatable. Six inductance-cancelled filters comprising nominally-identical PCB transformers populated with randomly-selected X capacitors (of the type used above) were constructed. Fig. 10 shows the performance of these filters in the test setup of Fig. 7. The top curve shows the response with a capacitor alone (without use of inductance cancellation). The lower six curves show the performance of the six filters incorporating printed cancellation windings. The performance of the six inductance-cancelled filters are nearly identical, with variations among units of less than 3 dB at frequencies up to 30 MHz. In every case, more than a factor of 10 (20 dB) improvement in attenuation is achieved over a capacitor alone across a wide frequency range. It may be concluded that the proposed approach can achieve large and very repeatable improvements in filtering performance.

Another characteristic that would benefit the practical proposed inductance cancellation technique is if the capacitor can be replaced with similar (but not identical) parts. Typical filter designs will admit alternative capacitors from a different source. The proposed technique will work best when the replacement part exhibits the same parasitic inductance. Fig. 11 shows the

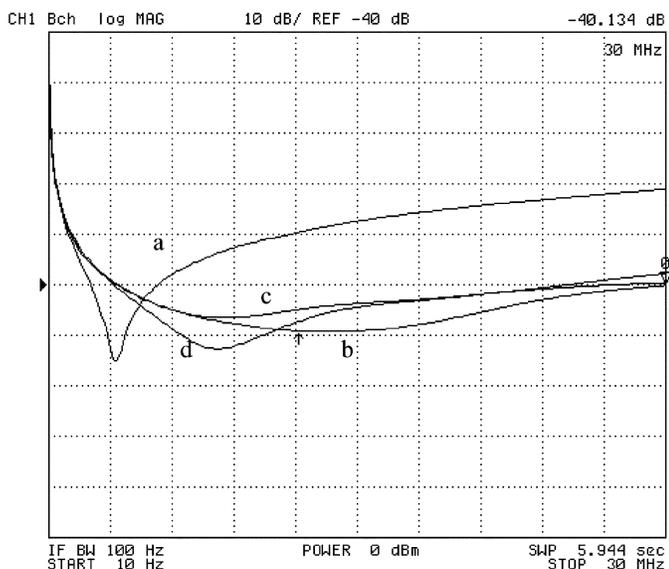


Fig. 11. Performance of an inductance cancellation filter using different types of capacitors, as measured using the test setup of Fig. 7. Trace (a) is the performance of a Beyschlag Centrallab 2222-338-24-224 capacitor without inductance cancellation. Traces (b), (c), and (d) use the Beyschlag Centrallab 2222-338-24-224 capacitor and the Panasonic capacitors ECQ-U2A224MG and ECQ-U2A224ML. The Panasonic capacitors have the same rating (0.22  $\mu$ F, 275 V<sub>ac</sub>) and pinouts, but different packages.

performance of a filter using three different types of X capacitors using the test setup of Fig. 7. The three capacitors have the same pin spacing, but different packages, so they are not identical replacement parts. The inductance cancellation transformer was designed for the Beyschlag Centrallab 2222-338-24-224 capacitor; the Panasonic capacitors (ECQ-U2A224MG and ECQ-U2A224ML) have about 4 nH more inductance and therefore the performance of the systems with these capacitors differ from that of the original. Nevertheless, despite the fact that these are not identical replacement parts, performance is still greatly improved as compared to the uncanceled case. It may be concluded that the proposed approach is at least reasonably tolerant of component replacement and second sourcing.

Ground planes are often used in high-performance power circuits and filters. Clearly, however, a ground (or other) plane should not usually be placed under a printed inductance cancellation transformer<sup>7</sup>. Furthermore, the edge of any plane should be placed some radius away from the coil so that it will not interfere with the coil coupling (and will allow a flux return path). To quantify the size of the keepout region needed around a PCB cancellation transformer to prevent changes in its performance, we simulated (circular) transformers of various outer diameters and with various ground plane configurations in FastHenry. Each ground plane consisted of a plane with a circular hole of specified radius centered on the cancellation transformer. (Center-tapped transformers were realized as two coils with one turn each, while end-tapped transformers were realized as a three turn coil and a one turn coil. In each case, the coils were on different layers with a 62 mil (1.6 mm) spacing. We then identified the minimum radius of the ground-plane

<sup>7</sup>If this is done, the pcb cancellation transformer will be larger and have a higher ac resistance.

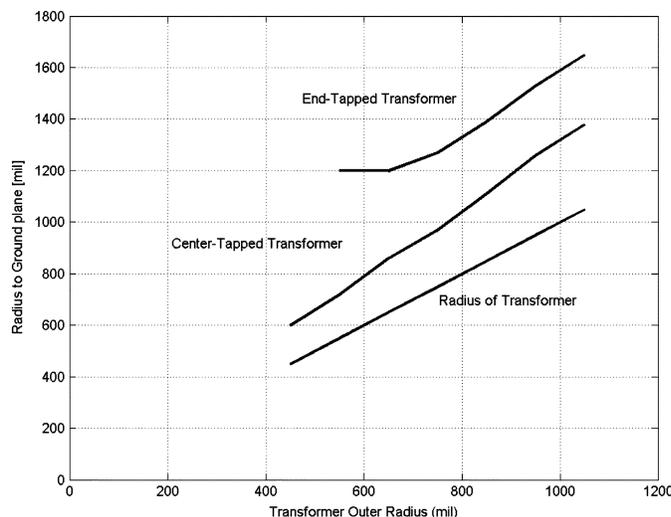


Fig. 12. Amount of spacing that is needed between the transformer and the groundplane to ensure that the shunt path inductance is within 1 dB of its desired value. The lowest curve represents the outer edge of the transformer coil. The spacing needed for a center-tapped transformer is about 33% larger than the outer radius of the transformer. The radius needed for end-tapped designs is larger.

keepout region needed such that the effective negative inductance provided by the printed transformer was within 1 dB of the value achieved without a ground plane present. The results of this study are illustrated in Fig. 12. For a circular center-tapped transformer of the dimensions considered, the radius of the ground plane keepout region should be at least 33% larger than the outer radius of the cancellation transformer. The results are somewhat more complicated for end-tapped designs, but generally a larger keepout radius is needed, as per Fig. 12. Subsequent experimental measurements confirmed that the proposed keepout regions are sufficient for maintaining the desired level of performance.

To validate the effectiveness of FastHenry for predicting groundplane keepout effects, two closely related systems were fabricated, tested, and simulated. Inductance cancellation transformer and ground planes were fabricated with at least 0.5 mils precision. The transformers each comprised of 100 mils (2.5 mm) wide traces with an outer radius of 368 mils (9.35 mm) with two coils having two turns and one turn. In the first system, a keepout radius of 568 mils (14.43 mm) was used, while in the second system a keepout radius of 468 mils (11.89 mm) was used. The effective shunt-path inductances of each of these systems were estimated using the test setup of Fig. 7. Estimates were made by measuring the response voltage and fitting the data while neglecting the effect of the series-path inductances. At several frequencies above 15 MHz (A frequency in which the shunt path inductances dominate the impedance) the inductance of the two systems were calculated and the difference in inductance was recorded. The two transformer layouts were also simulated in FastHenry, and the difference in inductances was recorded. Table III lists the results of this experiment, the measured and simulated absolute inductances vary because the simulation does not take into account any of the interconnection inductances. However, the difference in inductance between the two keepout radii found

TABLE III  
EXPERIMENTAL VERIFICATION OF FASTHENRY SIMULATIONS OF THE GROUNDPLANE. TWO LAYOUTS ARE TESTED WITH ALL FEATURES IDENTICAL EXCEPT THAT THE KEEPOUT GROUNDPLANE CIRCLE WILL HAVE RADII OF 568 AND 468 MILS (14.4 AND 11.9 MM). THIS EXPERIMENT COMPARES THE DIFFERENCE IN INDUCTANCE FOR BOTH SIMULATED AND MEASURED RESULTS

Freq	Measured Output Voltage For Keepout R = 568 mil	Measured Output Voltage For Keepout R = 468 mil	Corresponding Difference in Inductance (nH)	FastHenry Predicted Difference in Inductance (nH)
15 MHz	-51.80 dB	-50.26 dB	1.181	1.19
20 MHz	-47.60 dB	-46.31 dB	1.187	1.26
25 MHz	-43.943 dB	-43.06 dB	0.68223	1.31
30 MHz	-42.938 dB	-41.65 dB	1.349	1.35

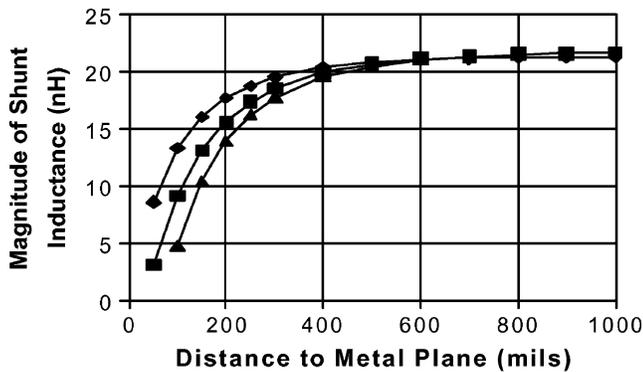


Fig. 13. Simulation-based calculation of the effect of a metal plane on the effective negative shunt inductance. The results are for the transformer designs used in Table I. The highest curve shows the effect for a center-tapped transformer. The two coils for an end-tapped core are always different. One coil must have a low inductance, while the other is much higher. The middle curve shows the effect for the end-tapped core in which the metal plane is approaching the low-inductance coil. The lowest curve shows the effect when the plane approaches the high-inductance coil of the transformer.

in simulation and experiment are quite close. One may thus conclude that the FastHenry prediction of ground-plane effects sufficient for design purposes.

The flux path in an air-core transformer is not as well defined as in a transformer with a high permeability core. The presence of a large sheet of metal in the space directly above or below the transformer may alter the flux path. (An outer circuit enclosure or other large metallic object in close proximity to the transformer could have this effect, for example.) We have used simulation and experimental measurements to study the effects of such external planes on PCB cancellation transformers. End- and center-tapped transformers similar to those shown in Fig. 5 were simulated in the presence of a plane of metal at a fixed distance below the board. The results of this study are illustrated in Fig. 13 where the magnitude of the negative equivalent inductance is plotted against the distance between the board and the metal plane. Three cases are presented. In one case, the plane approaches either coil of the center-tapped transformer. In the second case a plane is positioned near the low inductance coil of the end-tapped design, and in the third case the plane is near the high inductance coil of an end-tapped design.

A simulation-based experimental test, similar to that of Fig. 12 was carried out to show the effects of the presence of an external plane. In this test the distance to a metal plane beneath a transformer is varied so that the effective negative

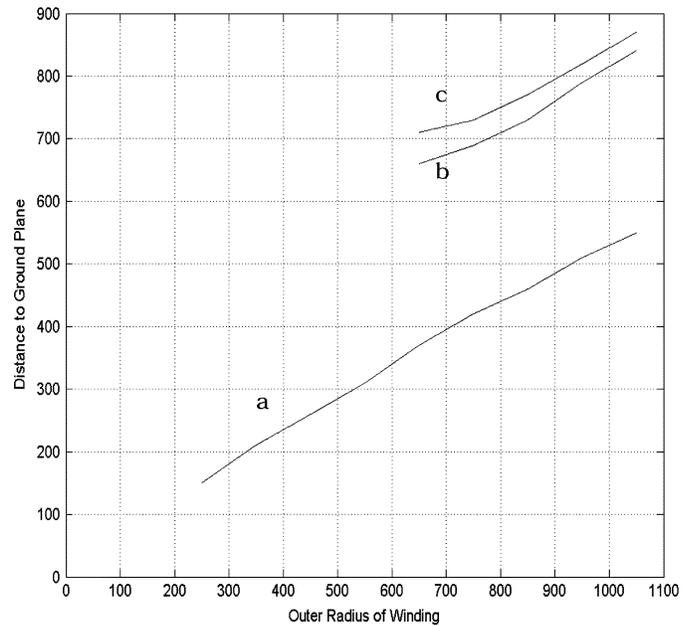


Fig. 14. Simulation based calculations of the distance between a metal plate and the transformer needed to perturb the shunt path inductance by 1 dB. Center-tapped transformers (a) are much less insensitive to the presence of a metal plane. In end-tapped transformers, the case in which the metal plane approaches the low-inductance coil (b) has lower sensitivity than when the plane approaches the high inductance coil (c).

inductance of the transformer decreases by 1 dB. The test considered center-tapped transformers that consist of one turn on each side of the board and with various outer diameters. End-tapped transformers for this test had three turns on one side and a single turn on the other. The outer radii of both coils are equal and the trace width is 100 mils. As seen in Fig. 14, the center-tapped designs are less sensitive to the presence of an external plane. Furthermore, for end-tapped transformers the coil with less inductance can be placed closer to an external plane.

It is reasonable to expect that the presence of magnetic material near the air-core transformer could also adversely affect its performance. The presence of material with permeability other than  $\mu_0$  near the core will influence the flux patterns and may change the inductances in the transformer. Fig. 15 shows the effect of magnetic material (type 3F3) when it is placed next to a device under test in the test setup in Fig. 7. In this case the transformer used is a 1 turn by 1 turn center-tapped transformer with radius 325 mils ( $\sim 8.3$  mm) and a trace width of 100 mils (2.54 mm). The figure shows that the performance of the transformer is only affected when the magnetic material is placed over the windings and that the amount of influence is related to the distance the magnetic material is from the board. The conclusion of this empirical test is that having magnetic material on the same board and close to the capacitor and windings is not an issue, as long as the material does not impinge directly on the transformer. Also, if the system is placed near other boards (e.g., in a rack) some spacing [in this case 200 mils ( $\sim 5$  mm)] is needed if magnetic material will be positioned directly below the air-core transformer. Based on these results, we do not anticipate that this issue poses a significant problem.

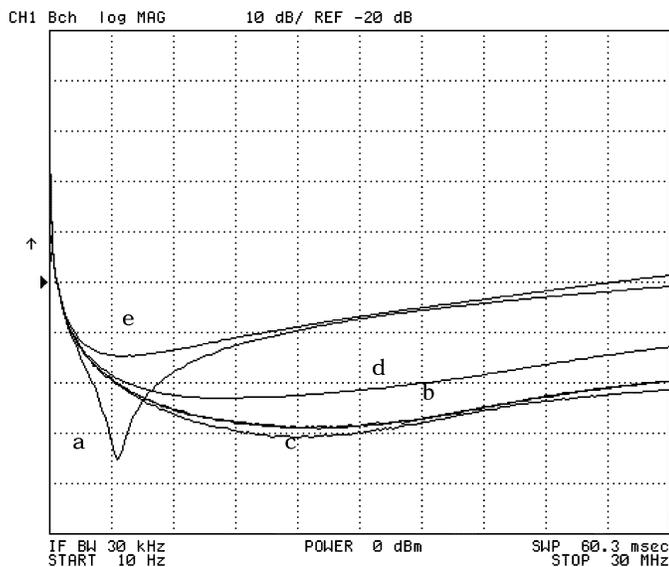


Fig. 15. Effects of magnetic material on the performance of inductance cancellation. Signal a shows the performance of a capacitor with no inductance cancellation windings, while signal b shows the performance with cancellation. When a ferrite core is placed adjacent to the capacitor and air-core windings there is not much change (c). The maximum amount of interference occurs when the core impinges directly on the windings. When the core is approximately 100 mils from the board, directly over the coils (d) the performance drops. When the core is placed directly over the windings, inductance cancellation is completely ineffective (e).

V. DESIGN AND EVALUATION OF AN EMI FILTER

A capacitor with an inductance cancellation transformer is a two-port filter rather than a (one-port) capacitor. The use of an inductance cancellation transformer will benefit some applications and not others. For example, the technique benefits filtering applications where transmission through the network is of primary concern, but does not benefit applications such as decoupling or snubbing where network output impedance is of primary concern. A general rule to determine if this technique will be useful for a given application is to examine all three branches in the T model. A candidate application should significantly benefit from a reduction in inductance in one branch, but not be overly sensitive to inductance increases in the other branches.

EMI filtering is one application where this technique excels. In addition to improving capacitor performance, the branch inductances introduced by the transformer serve to enhance filtering performance by increasing series-path impedance. This section explores the design of an inductance cancellation transformer for an EMI filter application. The performance of a filter utilizing inductance cancellation is then compared to a conventional implementation.

Fig. 16 shows a structure that can be used to realize a variety of filters. With a direct connection between the two stages, the two capacitors appear in parallel. If an inductor is used in one branch, a pi filter is formed, and if inductors are used in both branches a split-pi filter results. If a common-mode choke is used (as is done in many ac applications), one gets common-mode filtering from the choke, and differential mode filtering from the capacitors and the (relatively small) choke leakage inductance. Here we consider the effect of utilizing

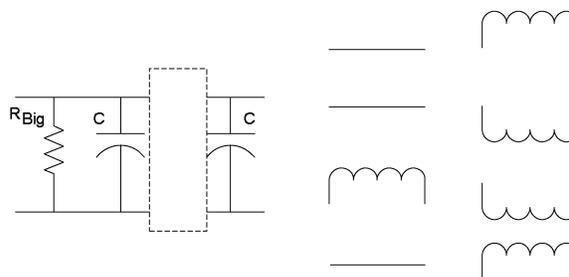


Fig. 16. EMI filter under test. The box can be replaced by any of the four connections shown. The filter can also use capacitors with or without inductance cancellation.

inductance cancellation on the (differential-mode) capacitors of Fig. 16. To simplify evaluation, we consider purely differential-mode connections of the circuit in Fig. 16 (i.e., connections 1 and 2). Nevertheless, the basic results apply to the differential-mode behavior of filters providing both common- and differential-mode filtering.

The procedure in section three was used to design the transformer for both the capacitors. The inductance formulas (2)–(4) were used to determine the inductance for center-tapped transformers with a one turn and a two turn coil. The entire circuit was modeled in FastHenry and refined using the procedures in Section III-C. The final design uses a transformer with a trace width of 100 mils (2.54 mm) and an outer radius of 345 mils (8.76 mm). According to the inductance formula (2) this transformer has a mutual inductance of 19 nH. The layout for the board is shown in Fig. 17, along with the layout of the conventional filter.

The performance of the filter circuit for several filter connections (with and without inductance cancellation) is illustrated in Fig. 18. These results were obtained using the test setup of Fig. 7, as described previously. Trace d of Fig. 18 shows the measurement noise floor (the response with the network analyzer input and output both disconnected from the filter). Trace a shows the performance of the circuit without inductance cancellation connected in configuration 1 (capacitors in parallel). As expected, substantial attenuation is achieved, but it becomes poorer above the 3 MHz self-resonant frequency of the capacitors. Trace b shows the performance of the same configuration using the design with inductance cancellation. Attenuation is greatly improved (over the case without cancellation) for frequencies above the self resonant frequency of the capacitors, reflecting the benefit of nulling their parasitic inductance. At high frequencies, as much as 40 dB of improvement in attenuation is achieved over the conventional implementation.

Despite the large performance improvement that is achieved, the performance still isn't as good as one might anticipate. It can be clearly seen that the rate of improvement of the inductance-cancelled design over the conventional design drops rapidly at about 6 MHz. This occurs because at frequencies above 6 MHz the output response of the filter is dominated by parasitics that entirely bypass the capacitors and cancellation transformers. In fact, for those frequencies, the performance remains unchanged even if the connections between the first and second capacitor networks are removed entirely! Measurements reveal a 1.3 pF parasitic capacitance from the filter input to the filter output that

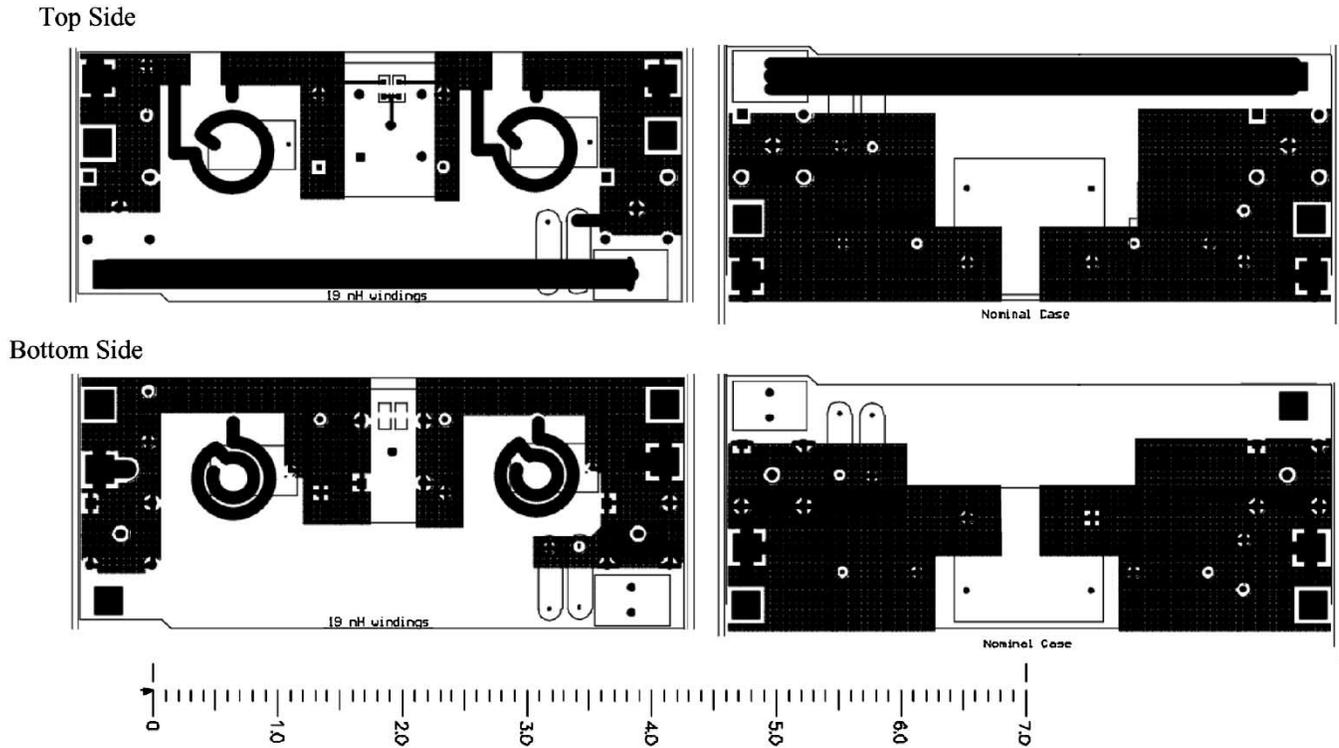


Fig. 17. Layout of the filter containing capacitors with and without inductance cancellation. The traces in the middle area of the inductor cancellation board are for testing the capacitors and are removed afterwards. The left column shows top and bottom-side of the filter board with inductance cancellation. The right column shows the top and bottom-side of the filter board without inductance cancellation. Length marks are in inches.

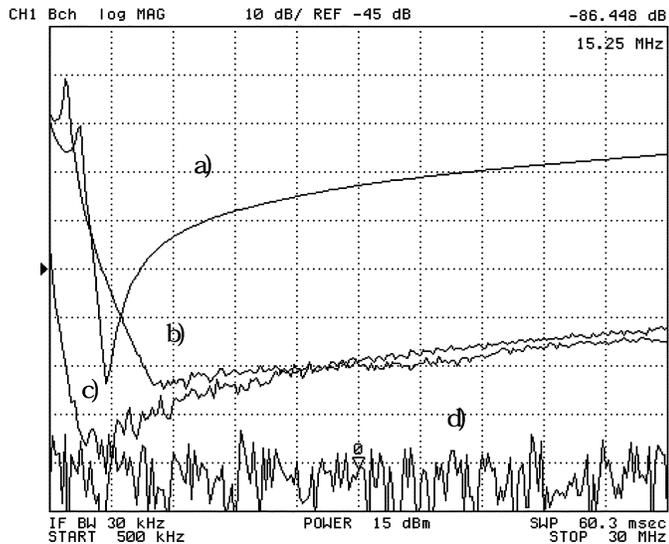


Fig. 18. Results of the EMI Filter test. Signal a is the performance of two normal capacitors. Signal b is the performance of two capacitors with inductance cancellation. Signal c is the performance of a normal capacitor with a single inductor in the series path. Signal d is the noise floor.

at least partially accounts for this parasitic coupling. Hence, the introduction of inductance cancellation has improved the filter performance to such an extent that small parasitic paths (e.g., associated with layout) are the dominant factor in performance.

Trace c of Fig. 18 shows the performance of a pi filter connection (Fig. 16 connection 2) without inductance cancellation. As can be seen, filter performance is greatly improved, with the output response falling quickly to the “coupling floor” (the

level at which parasitic coupling past the filter components dominates). A  $20 \mu\text{H}$  inductor was selected for the filter. This is the smallest inductor sufficient to drive the output response down to the coupling floor out to 30 MHz. (It was found that a larger inductance did not further increase attenuation at high frequencies, and a smaller inductance provided less attenuation.) Thus, we find that at frequencies above 6 MHz the capacitors with inductance cancellation provide the same attenuation performance as the full pi filter (without inductance cancellation), though the pi filter provides better performance at low frequencies. Depending on the EMI specification and system parasitics, inductance cancellation methods can be as effective as higher-order filtering in achieving high attenuation. With either approach, eliminating filter parasitic coupling (by layout, shielding, etc.) is critical for achieving maximum filter performance.

Initial testing with shielding indicates that the coupling floor can be reduced. A 10 mil thick and 150-mil wide piece of copper tape that encircles the capacitor and transformer was added perpendicular to the board. For both the nominal case and the system with inductance cancellation the coupling floor is reduced by 5 dB for frequencies below 30 MHz. In both cases the reduction in coupling floor directly corresponds to an improvement in the measured response of the filters. Thus the reduction in parasitic coupling is equally beneficial to the two systems.

## VI. CONCLUSION

Capacitor parasitic inductance often limits the high-frequency performance of filters for power applications. However,

these limitations can be overcome through the use of specially-coupled magnetic windings that effectively nullify the capacitor parasitic inductance. This paper explores the use of printed circuit board (PCB) transformers to realize parasitic inductance cancellation of filter capacitors. Design of such inductance cancellation transformers is explored, and applicable design rules are established and experimentally validated. The high performance of the proposed inductance cancellation technology is demonstrated in an EMI filter application.

#### APPENDIX A

##### EMPIRICAL INDUCTANCE CALCULATION FORMULAS

In this section we present empirical formulas for calculating self and mutual inductance of planar rectangular coils. In general approximate formulas can be found by curve fitting a given set of datapoints. In this case all the formulas were derived by curve fitting simulation data found using the program FastHenry. The formulas describe rectangular coils with the relative sizes and shapes that are typically needed for inductance cancellation techniques. This includes coils with dimensions between .5 in and 2 in on a side. Similar formulas can be developed for any shape or size coil.

These formulas only consider coils made up of full turns. Multiple turn coils will be considered as mutually coupled coils in series in which the total inductance  $L_T$  is calculated as

$$L_T = \sum_{i=1}^n L_{ii} + \sum_{i=1}^n \sum_{j=1}^{i-1} 2 \cdot L_{ij}$$

where  $L_{ij}$  is the mutual inductance between turns  $i$  and  $j$ ,  $L_{ii}$  is the self inductance of turn  $i$ , and  $n$  is the number of turns.

The self-inductance of any turn can be given as

$$L_{ii} = L_{sq} \cdot K_W \cdot K_R$$

where each of these factors are defined in this Appendix.

$L_{sq}$  is the inductance of an equivalent square coil with a 100-mil trace width. The equivalent square coil is defined as a square coil with the same area as the rectangle coil.  $L_{sq}$  is defined as

$$L_{sq} = 82.25 \frac{\text{nH}}{\text{inch}} \cdot s_{eq}[\text{in}] - 23.51 \text{ nH}$$

$$s_{eq}[\text{in}] = \sqrt{L[\text{in}] \cdot W[\text{in}]}$$

where  $s_{eq}$ ,  $L$ ,  $W$  are the length of the side of the equivalent square coil, the length of the rectangular coil, and the width of the rectangular coil. This formula applies to square coils with areas between .25 and 4 square inches.

The factor  $K_W$  is used to compensate for the width,  $w$ , of the trace. This factor depends on the width of the trace and the length of a side of the equivalent square coil.  $K_W$  is defined as

$$K_W = B + A \cdot \ln(w[\text{mil}])$$

where

$$A = 0.0833 \cdot \ln(s_{eq}[\text{in}]) - 0.3297$$

$$B = 1 - A \cdot \ln(100).$$

For rectangular coils the factor  $K_R$  is needed. This factor depends on the ratio of the sides of the rectangle  $k_r$ . (Note that  $k_r$  will always be greater than 1.)

$$K_R = 1 + (k_r - 1) \cdot 0.055.$$

The mutual inductance between two coils is given by

$$L_{ij} = L_m \cdot K_{R-ave} \cdot K_Z.$$

$L_m$  is the mutual inductance assuming both coils are square and that they are on the same layer.  $K_{R-ave}$  and  $K_Z$  modify this number to compensate if the coils have unequal sides or if the coils are on different layers of the PCB.  $L_m$  is given by

$$L_m = C_m \cdot e^{D_m \cdot s_{eq2}}$$

$$C_m = E_m \cdot \ln(s_{eq1}) + F_m$$

$$D_m = G_m \cdot \ln(s_{eq1}) + H_m$$

$$E_m = 0.0092(w_1) - 0.0008$$

$$F_m = -0.005(w_1) + 1.4426$$

$$G_m = -0.0096(w_1) - 1.8523$$

$$H_m = 0.006(w_1) + 3.5207$$

where  $s_{eq1}$  is the length of the side of the equivalent square coils in inches for the larger turn,  $s_{eq2}$  is the equivalent length for the smaller turn, and  $w_1$  is the trace width of the first coil in mils. If the two coils have different trace width then define the coil with the smaller width as coil 1.  $L_m$  will be in nH.

$K_{R-ave}$  is the average of the rectangular coil constant  $K_R$  and is given as

$$K_{R-ave} = (K_R|_{coil1} + K_R|_{coil2}) \cdot \frac{1}{2}.$$

The last factor,  $K_Z$ , accounts for displacement between coils on different layers. Typical board spacing is either 31 or 62 mil spacing. This factor is approximated as a constant factor for a given spacing  $K_Z$  is 0.99 for 31-mil spacing and 0.975 for 62-mil spacing.

With these inductance formula the following case was examined. A two-turn inductor has a trace width of 150 mils. The first turn has sides of lengths 1200 mils and 1000 mils, and the second turn has sides of 800 mils and 600 mils.

The terms to calculate the inductance for the first turn are

$$s_{eq1} = 1.095 \text{ inches} \quad L_{eq} = 66.6 \text{ nH}$$

$$A = -0.3220 \quad B = 2.4829$$

$$K_W = 0.8694 \quad k_r = 1.2$$

$$K_R = 1.011 \quad L_{11} = 58.5 \text{ nH}.$$

The terms to calculate the inductance for the second turn are

$$s_{eq2} = 0.6928 \text{ inches} \quad L_{eq} = 33.47 \text{ nH}$$

$$A = -0.3603 \quad B = 2.659$$

$$K_W = 0.8536 \quad k_r = 1.333$$

$$K_R = 1.0183 \quad L_{22} = 29.09 \text{ nH}.$$

The terms to get the mutual inductance are

$$\begin{aligned} E_m &= 1.3792 & F_m &= 0.6926 \\ G_m &= -3.2923 & E_m &= -4.4207 \\ C_m &= 0.81776 & D_m &= 4.1219 \\ L_m &= 14.22 & K_{R-ave} &= 1.01465 \\ K_Z &= 1 & L_{12} &= 14.43. \end{aligned}$$

The inductance for the inductor becomes 116.45 nH. The FastHenry prediction for this inductor is 123.37 nH.

#### ACKNOWLEDGMENT

The authors would like to thank J. Phinney for his work and support.

#### REFERENCES

- [1] T. K. Phelps and W. S. Tate, "Optimizing passive input filter designs," in *Proc. 6th National Solid-State Power Conversion Conference*, May 1979, pp. G1-1-G1-10.
- [2] T. C. Neugebauer, J. W. Phinney, and D. J. Perreault, "Filters and components with inductance cancellation," in *Proc. IEEE Industrial Applications Society Annual Meeting*, Oct. 2002, pp. 939-947.
- [3] G. B. Crouse, "Electrical Filter," U.S. Patent 1 920 948, Aug. 1, 1933.
- [4] D. C. Hamill and P. T. Krein, "A 'zero' ripple technique applicable to any DC converter," in *Proc. IEEE Power Electronics Specialists Conference*, June 1999, pp. 1165-1171.
- [5] S. Feng, W. A. Sander, and T. G. Wilson, "Small-capacitance nondissipative ripple filters for DC supplies," *IEEE Trans. Magnetics*, vol. 6, pp. 137-142, Mar. 1970.
- [6] R. P. Severns and G. E. Bloom, *Modern DC-to-DC Switchmode Power Converter Circuits*. New York: Van Nostrand Reinhold, 1985.
- [7] J. W. Kolar, H. Sree, N. Mohan, and F. C. Zach, "Novel aspects of an application of 'zero' ripple techniques to basic converter topologies," in *Proc. IEEE Power Electronics Specialists Conference*, June 1997, pp. 796-803.
- [8] G. E. Bloom and R. Severns, "The generalized use of integrated magnetics and zero-ripple techniques in switchmode power converters," in *Proc. IEEE Power Electronics Specialists Conference*, 1984, pp. 15-33.
- [9] S. Senini and P. J. Wolfs, "The coupled inductor filter: Analysis and design for AC systems," *IEEE Trans. Ind. Electron.*, vol. 45, pp. 574-578, Aug. 1998.
- [10] A. Kamon, L. M. Silveira, C. Smithhisler, and J. White, *FastHenry User's Guide*. Cambridge, MA: MIT, 1996.
- [11] C. M. Zierhofer, "Geometric approach for coupling enhancement of magnetically coupled coils," *IEEE Trans. Biomed. Eng.*, vol. 43, pp. 708-714, July 1996.

- [12] W. G. Hurley and M. C. Duffy, "Calculation of self and mutual impedances in planar magnetic structures," *IEEE Trans. Magnetics*, vol. 31, pp. 2416-2422, July 1995.
- [13] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York: Dover, 1946.
- [14] H. E. Bryan, "Printed inductors and capacitors," *Tele-Tech Electron. Industries*, vol. 14, no. 12, p. 68, Dec. 1955.
- [15] H. G. Dill, "Designing inductors for thin-film application?," *Electron. Design*, pp. 522-559, Feb. 17, 1964.
- [16] H. A. Wheeler, "Simple inductance formulas for radio coils," in *Proc. I.R.E.*, vol. 16, Oct. 1928.
- [17] C. R. Sullivan and A. M. Kern, "Capacitors with fast current switching require distributed models," in *Proc. IEEE Power Electronics Specialists Conference*, June 2001, pp. 1497-1503.



**Timothy C. Neugebauer** (S'03) received the B.S. degree in electrical engineering from Union College, Schenectady, NY, in 1997 and the M.S. degree from the Massachusetts Institute of Technology (MIT), Cambridge, in 1999, where he is currently pursuing the Ph.D. degree in the LEES Laboratory.

Since 1997, he has been a graduate student in LEES Laboratory, MIT. He has worked in the areas of dc/dc converters, multilevel inverters, and the design of passive elements.



**David J. Perreault** (M'98) received the B.S. degree from Boston University, Boston, MA, in 1989, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 1991 and 1997, respectively.

In 1997, he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate, where he later became a Research Scientist in 1999. In July 2001, he joined the MIT Department of Electrical Engineering and Computer Science as an Assistant Professor.

He teaches a graduate-level course in power electronics at MIT, and is a consultant to industry in the field. At present, his research interests are in design, manufacturing, and control techniques for power electronic systems and components, and in their use in industrial, commercial, transportation, and medical applications.

Perreault received the IEEE Richard M. Bass Outstanding Young Power Electronics Engineer Award and the ONR Young Investigator Award. He is a Member of Tau Beta Pi and Sigma Xi.