

# Lossless Multi-Way Power Combining and Outphasing for High-Frequency Resonant Inverters

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**Abstract**— A lossless multi-way power combining and outphasing system has recently been proposed for high-frequency inverters and power amplifiers which offers major performance advantages over traditional approaches. This paper presents a new outphasing control strategy for the proposed system that enables output power control through effective load modulation of the inverters while minimizing loading admittance phase. Moreover, we present the first-ever experimental demonstration of the proposed outphasing system. The design of a 27.12 MHz, four-way power combining and outphasing system is described, and used to experimentally verify the power combiner's characteristics and evaluate the effectiveness of the proposed outphasing law to control output power over a 10:1 range.

**Keywords**— Outphasing, phase-shift control, LINC, power combining, Chireix combiner, RF power amplifier (RF PA).

## I. INTRODUCTION

High-frequency switched-mode power amplifiers (PAs), or resonant inverters, find wide applicability in numerous areas including radio-frequency (RF) communications, industrial processing, medical imaging and power conversion. At very high powers and frequencies, it is often preferable to construct multiple low-power PAs and combine their output power to form a high-power PA. Moreover, such PAs or inverters must often be able to: (1) provide dynamic control of their output power over a wide range, and (2) maintain high efficiency across the operating range.

Proposed originally in the 1930's, *outphasing* (or phase-shift control) of power amplifiers (PAs) or inverters is a key technique (illustrated in Fig. 1) for simultaneously satisfying these requirements [1]. Power from multiple small PAs ( $PA_1 - PA_n$ ) is losslessly combined and delivered to a load. Power control is achieved by appropriately adjusting the phases ( $\Phi_1 - \Phi_n$ ) of the PAs, causing them to interact in such a manner that their power output is modulated. In particular, the real component of the effective loading admittances of the PAs ( $Y_{in,1} - Y_{in,2}$ ) vary with outphasing, changing the total delivered power (load modulation).

The Chireix combiner (Fig. 2A) is a traditional implementation of the outphasing concept with two input power ports  $P_{in,A}$  and  $P_{in,B}$ , and one output power port  $P_{out}$  [1]. Although ideally lossless, the susceptive loading this combiner presents to the PAs varies considerably with outphasing (and power delivery). This adversely impacts the efficiency of the

overall system owing to the sensitivity of inverters and power amplifiers suitable for very high frequencies to reactive loads, and to the additional losses owing to reactive currents [2].

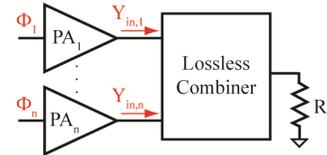


Figure 1. Outphasing: controlling relative PA phases ( $\Phi_1 - \Phi_n$ ) modulates the effective PA loading admittances and determines the power delivered to the load  $R_L$ .

A new power combining and outphasing system has recently been proposed to overcome the loss and reactive loading problems of traditional outphasing approaches such as Chireix combining [3]. It provides ideally lossless power combining from four or more PAs, along with nearly resistive individual PA loading over a very wide output power range. Fig. 2B depicts one possible implementation of such a combiner for four PAs (four-way combiner). As with the Chireix combiner, the output power it delivers is determined by the amount of phase shift (outphasing) between the PAs. An outphasing control strategy that enables output power control by minimizing susceptive variations in the PA loading has already been described [4]. Furthermore, a design procedure for selecting the combiner reactances  $X_1$  and  $X_2$  based on the desired operating output power range (Fig. 2B) has been previously presented [4].

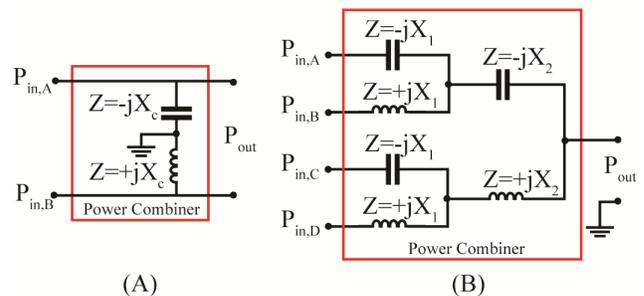


Figure 2. (A) Chireix combiner; (B) A four-way implementation of the proposed multi-way combiner [4]. Reactance values are shown for the fundamental output frequency.

The purpose of this paper is to both experimentally demonstrate this new outphasing system for the first time, and to introduce a new outphasing power control strategy for the outphasing system which minimizes the phase of the PA loading admittance over an operating power range. We also describe an appropriate combiner design methodology. Finally, the implementation and experimental performance of a 27.12 MHz, four-way power combining system is presented.

## II. THE NEW OPTIMAL PHASE OUTPHASING CONTROL

Consider the four-way combiner of Fig. 3 driving a resistive load  $R_L$ . To simplify analysis, the PAs, or resonant inverters driving the combiner are treated as ideal sinusoidal voltage sources  $V_A - V_D$  with constant amplitude  $V_S$  and phasor relationships according to Fig. 4. Here we describe a means to control output power and voltage through outphasing (or phase shift) of the inverters driving the combiner, and detail a control law that provides desirable loading characteristics for the PAs.

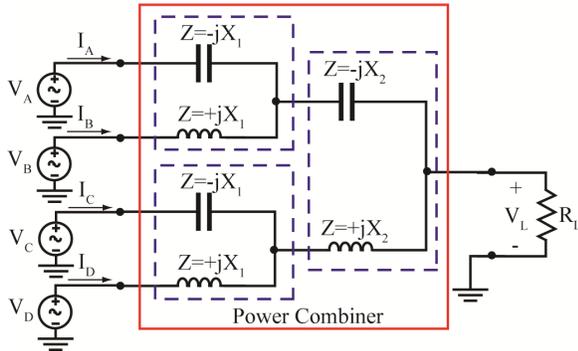


Figure 3. Four-way combiner driving a resistive load with PAs being treated as ideal voltage sources [3].

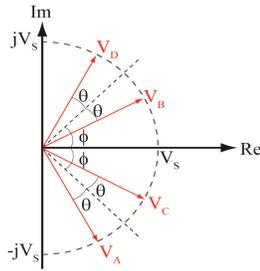


Figure 4. Phasor relationship among voltage sources  $V_A - V_D$  driving the four-way combiner of Fig. 3 [3].

It has been demonstrated that the effective admittances seen by the PAs driving the combiner (the complex ratio of current to voltage at a combiner input port with all driving sources active) are a strong function of the outphasing angles  $\theta$  and  $\phi$ , and are given by (1)-(4), where  $\gamma = R_L/X_1$  and  $\beta = X_2/X_1$  [4]. Furthermore, the combiner output power is given by (5) for any pair of outphasing angles:

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} \sin^2(\phi) \cos^2(\theta) \quad (5)$$

$$Y_{eff,A} = X_1^{-1}(\gamma - \gamma \cos(2\phi + 2\theta) - \gamma \cos(2\phi) + \gamma \cos(2\theta) - \beta \sin(2\phi)) + jX_1^{-1}(1 - \beta - \gamma \sin(2\phi + 2\theta) - \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (1)$$

$$Y_{eff,B} = X_1^{-1}(\gamma - \gamma \cos(2\theta - 2\phi) - \gamma \cos(2\phi) + \gamma \cos(2\theta) + \beta \sin(2\phi)) + jX_1^{-1}(-1 - \beta - \gamma \sin(2\theta - 2\phi) + \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (2)$$

$$Y_{eff,C} = X_1^{-1}(\gamma - \gamma \cos(2\theta - 2\phi) - \gamma \cos(2\phi) + \gamma \cos(2\theta) + \beta \sin(2\phi)) - jX_1^{-1}(-1 - \beta - \gamma \sin(2\theta - 2\phi) + \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (3)$$

$$Y_{eff,D} = X_1^{-1}(\gamma - \gamma \cos(2\phi + 2\theta) - \gamma \cos(2\phi) + \gamma \cos(2\theta) - \beta \sin(2\phi)) - jX_1^{-1}(1 - \beta - \gamma \sin(2\phi + 2\theta) - \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (4)$$

By solving (5) for  $\theta$  and  $\phi$  for a given output power, along with the additional constraint of minimizing the resultant effective input admittance phases, a set of non-linear equations (6) results which can be solved numerically to yield the desired optimal-phase (OP) outphasing control angles.

$$\begin{aligned} \frac{P_{out} X_1^2}{8R_L V_S^2} &= \sin^2(\phi) \cos^2(\theta) \\ \sin(2\phi) &= \frac{2\gamma \cos^2(\theta)}{\beta^2 + 4\gamma^2 \cos^2(\theta) - 2\beta\gamma \sin(2\theta)} \end{aligned} \quad (6)$$

Fig. 5 depicts the resultant optimal-phase control angles for an example four-way combiner design with  $R_L = 50 \Omega$ ,  $X_1 = 36.69 \Omega$ , and  $X_2 = 48.97 \Omega$ , and compares them to the outphasing angles computed according to the previously proposed optimal-susceptance (OS) control method [4]. As can be seen, both control strategies result in nearly identical control angles over most of the operating power range. This suggests that for all practical purposes, OP control simultaneously implies OS control and vice versa.

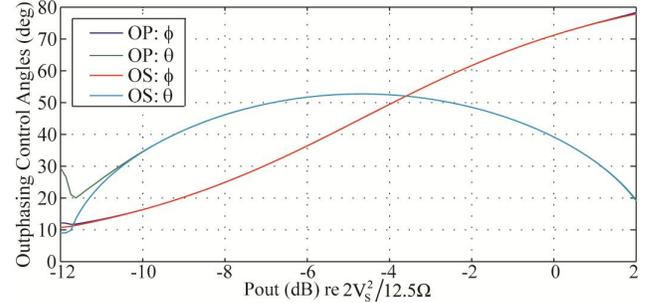


Figure 5. Outphasing control angles  $\theta$  and  $\phi$  for the Optimal-Phase (OP) and Optimal-Susceptance (OS) [4] control methods for an example four-way combiner design with  $R_L = 50\Omega$ ,  $X_1 = 36.69\Omega$ , and  $X_2 = 48.97\Omega$ .

The resultant effective input conductance and admittance phase seen by each of the four PAs over the operating power range for the above example design are illustrated in Fig. 6. As can be seen, the proposed OP control effectively modulates the combiner input conductance in accordance with the output power, while limiting variations in the admittance phase (and hence, susceptance) to less than  $2^\circ$  over an output power range

of approximately 10 dB (10:1 power range). It is important to note that for most of the output power range, the PAs see roughly the same conductance, and hence, are loaded equally. This control technique, when used with the proposed combiner, enables control of output power over a wide range while preserving desirable loading characteristics for the inverters.

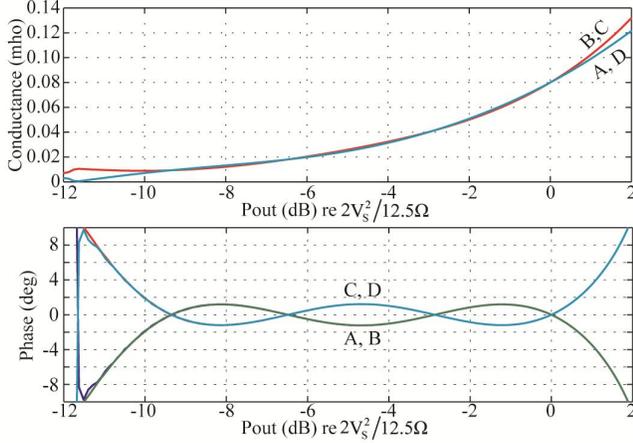


Figure 6. Effective input conductances and admittance phases for an example four-way combiner design with  $R_L = 50 \Omega$ ,  $X_1 = 36.69 \Omega$ , and  $X_2 = 48.97 \Omega$  under OP control.

### III. COMBINER DESIGN

A previously presented combiner design approach [4] entails the selection of reactances  $X_1$  and  $X_2$  according to (3)

$$\begin{aligned} X_2 &= \frac{2R_L}{k+1} \\ X_1 &= \frac{X_2}{k + \sqrt{k^2 - 1}} \end{aligned} \quad (3)$$

where  $k$  is a design parameter which uniquely determines the performance and behavior of the power combiner.

Fig. 7 provides a set of numerically-computed design curves which facilitate the selection of the optimal  $k$  value for a particular output power range ratio (PRR) under OP control. PRR is the ratio of the maximum to the minimum output power over which admittance phase is to be minimized (and approximately corresponds to the outer two power levels at which the input admittance phases become zero as in Fig. 6). The value of  $k$  is optimal in the sense that it results in the smallest worst-case input admittance phase over the specified operating PRR. The value of  $k$  can be determined by horizontally tracing from the specified PRR to the Power Ratio Curve, and then vertically to the  $k$ -axis. The corresponding worst-case admittance phase seen by the PAs can be obtained in turn by tracing the selected  $k$  to the Phase Curve, and then horizontally to the Phase axis.

For the system implementation discussed in this paper, the combiner was designed to operate over an output power range of approximately 10 dB and into a  $50 \Omega$  termination ( $R_L = 50 \Omega$ ). In accordance with Fig. 7, a  $k$ -value of 1.042 was selected, which in turn yields combiner reactances  $X_1 = 36.69 \Omega$ , and  $X_2$

$= 48.97 \Omega$ . As can be seen from both Fig. 6 and Fig. 7, the admittance phase over the suggested operating range is limited to less than  $2^\circ$ .

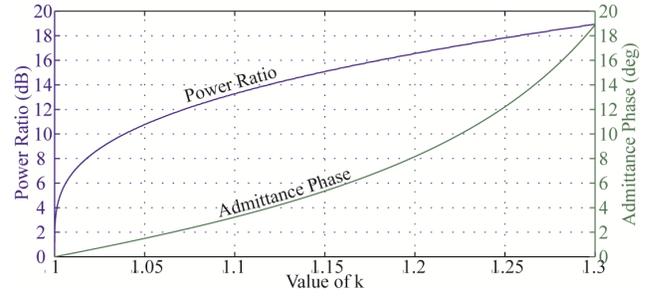


Figure 7. Effective input admittance phase-minimizing design curves for a four-way combiner under OP control methodology.

### IV. SYSTEM IMPLEMENTATION

A block diagram of the entire power combining and outphasing system, designed to operate at 27.12 MHz, is shown in Fig. 8. The input power ports of the combiner are driven by four identical class-E PAs which have been designed to deliver 25 W maximum output power at a  $12.5 \Omega$  load, and operate over a 10:1 load modulation ratio ( $12.5 \Omega$  to  $125 \Omega$ ) and corresponding power ratio [5]. For the results shown here, the PAs were operated over their full load-modulation and output power range, with each PA providing a peak output power of 25 W (amplitude of  $V_s = 25$  V in Fig. 4), with a combiner peak output power (delivered to the  $50\Omega$  load) of 100W.

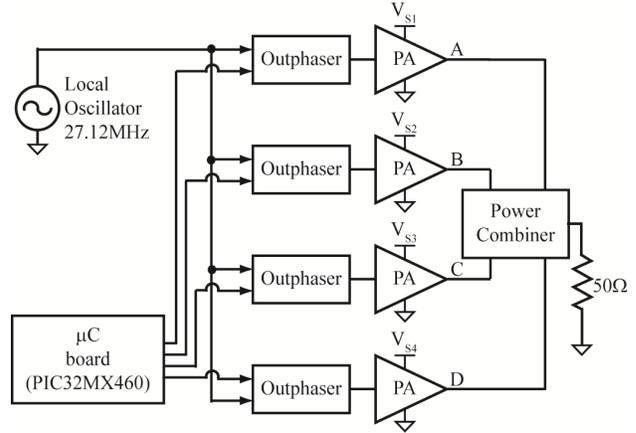


Figure 8. Block diagram of the implemented power combining and outphasing system.

In order to control the output power sourced from the PAs and delivered to the load, the PAs are outphased according to the outphasing control strategy discussed above (see Fig. 5). This task is accomplished by employing specially designed outphasers which take a reference sinusoidal input from a 27.12 MHz local oscillator and output a phase-shifted version of the input, which in turn serves as the PA driving signal. The amount of phase shift introduced by each outphaser is digitally controlled by a microcontroller (PIC32MX460, Microchip

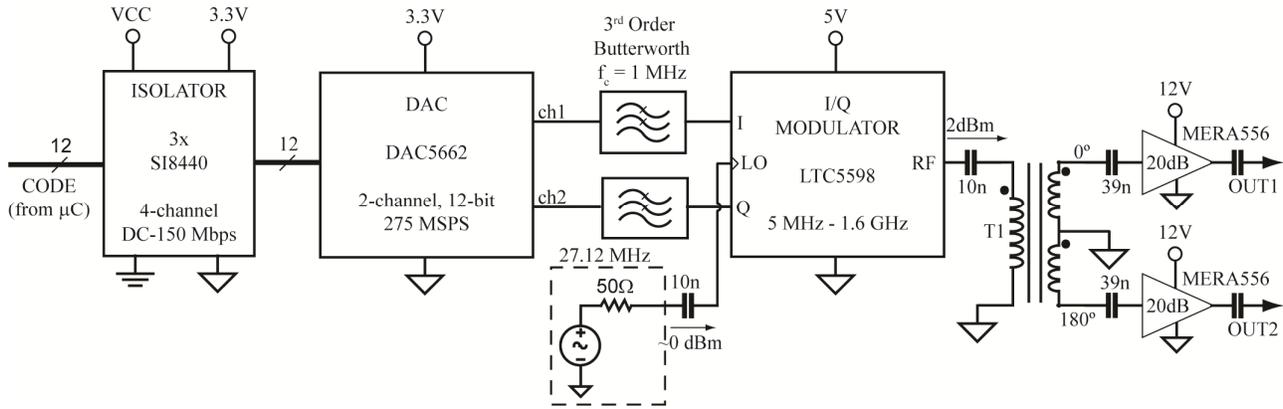


Figure 9. Block diagram of a single outphaser: LO-Local Oscillator input.

Technology Inc.) pre-programmed with a set of outphasing control angles (stored in a look-up table) corresponding to the desired output power levels. The design of the control system, the PAs, and the combiner are treated below.

#### A. Outphasing

The outphaser was originally designed with very wide bandwidth (5 MHz - 200 MHz) in order to facilitate the eventual testing of power combiners operating at various frequencies while alleviating the necessity for significant system modifications and redesign. The outphaser implementation discussed here is capable of providing any desired phase shift from  $-180^\circ$  to  $180^\circ$  with an accuracy of approximately  $\pm 0.1^\circ$  over the entire bandwidth. The proposed design (see Fig. 9) comprises an In-phase/Quadrature (IQ) Modulator (LTC5598, Linear Technology) which outphases a local oscillator (LO) signal by an amount determined by the In-phase (I) and Quadrature (Q) components. Fig. 10 clearly illustrates the phasor relationship between the LO signal the output of the I/Q Modulator (the RF signal); by appropriately adjusting I and Q (within a range of  $-0.5$  V to  $+0.5$  V), the RF signal can be phase-shifted any arbitrary amount with respect to the LO signal, and can also provide variable amplitude drive (though this is not used in the current setup).

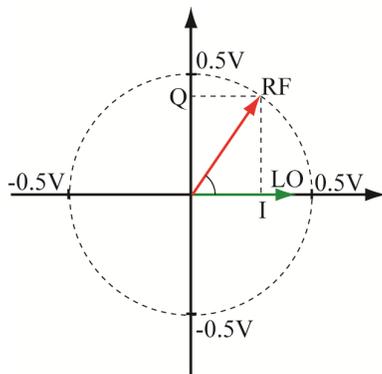


Figure 10. Phasor representation of the I/Q modulator output signal (RF) and its local oscillator input (LO).

Controlled by the PIC32MX460 microcontroller, a 2-channel, 12-bit DAC (DAC5662, Texas Instruments Inc.) is utilized to synthesize the I and Q components. Due to difference in the logic level voltages of the microcontroller and the DAC, three digital four-channel isolators (SI8440, Silicon Labs) are installed on the 12-bit DAC data bus.

The I/Q modulator's RF output signal is coupled to a balun with a 1:2 impedance ratio (T2-1T, Mini-Circuits) thus producing two complementary ( $180^\circ$  apart) versions of the RF signal, each further amplified by a 20 dB gain stage. This allows the outphaser to be used with PAs requiring complementary gate-driving signals (such as a Class-B push-pull stage). Note however that in the present work only one of the outputs is used (OUT1 in Fig. 9) while the other is terminated at  $50\Omega$ . Due to the non-linear mixing process incorporated inside the modulator to introduce the desired phase shift, its output contains significant harmonic content, and so, a 27.12 MHz band-pass filter (part of the PA gate-driving circuit, discussed in Section C) must be used to extract the fundamental component from OUT1. This signal is in turn coupled directly to the PA gate drivers.

Although the present work investigates only the static performance of the combiner, the outphaser of Fig. 9 is designed to provide dynamic phase control with a 1 MHz bandwidth to facilitate future testing of the combiner's dynamic performance.

#### B. The Power Amplifiers

In applications involving frequencies above 10 MHz, single-switch power amplifiers (or resonant inverters) such as the Class-E inverter are often preferred. Fig. 11 depicts the topology of the 27.12 MHz Class-E amplifiers employed for driving the combiner. The input inductor  $L_f$  acts as a choke, while the parallel-tuned output filter network  $L_p$ - $C_p$  improves the output waveform quality by attenuating higher-frequency components. (Note that the combiner is designed to operate at a very narrow bandwidth, with the input-port voltage waveforms ideally being sinusoidal.) In a traditional Class-E inverter [6, 7, 8] the tuned load network comprising  $C_s$ ,  $L_s$ , the total drain-to-source capacitance (the combination of  $C_d$  and the switch output capacitance), and the inverter's loading impedance (in this case, the effective combiner input-port impedance) are

selected to shape the drain-to-source switch voltage  $v_{DS}$  to provide zero-voltage switching (ZVS) and zero  $dv_{DS}/dt$  switch turn-on.

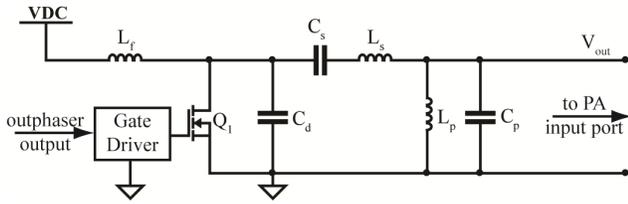


Figure 11. Topology of the implemented Class-E power amplifier.

As a result, the traditional Class-E inverter is highly sensitive to loading variations [7, 9], and considerably deviates from zero-voltage switching for load resistance variations of more than about a factor of two. Since in the present application, the input-port combiner impedance is modulated over a 10:1 range, a recently proposed Class-E design methodology was employed for selecting the inverter components ( $L_s$ ,  $C_s$ ,  $L_p$ ,  $C_p$ , and  $C_d$ ) so as to maintain zero-voltage switching over the entire load-modulation range, without necessarily ensuring a zero  $dv_{DS}/dt$  switch turn-on as loading resistance varies [5]. Table I lists the inverter component values along with their implementation. A gallium-nitride power transistor (EPC1007, Efficient Power Conversion Corp.) was used as a switch with an output capacitance  $C_{oss}$  of approximately 150 pF and channel on-resistance  $R_{on}$  of approximately 30 m $\Omega$ .

TABLE I. COMPONENT VALUES FOR THE IMPLEMENTED CLASS-E PAs

Component	Value	Implementation
$L_f$	35.6 nH	3 parallel 132-09SMJL inductors (Coilcraft Inc.)
$L_s$	380 nH	132-17SMJL inductor (Coilcraft Inc.)
$L_p$	169 nH	132-12SMJL inductor (Coilcraft Inc.)
$C_d$	377 pF	ATC700A Capacitor Series (American Technical Ceramics Corp.)
$C_s$	90 pF	
$C_p$	203 pF	
$Q_1$	$C_{oss} \approx 150$ pF $R_{on} \approx 0.03$ $\Omega$	EPC1007 (Efficient Power Conversion Corp.)

The gate-drive circuit is shown in Fig. 12. As already mentioned, due to its non-linear characteristics, the I/Q modulator introduces significant harmonic content in the phase-shifted signal (see Fig. 9), and so the outphaser output signal is band-pass filtered at 27.12 MHz to isolate only the fundamental and correctly phase-shifted component. The sinusoidal filter output is then "squared up" with a comparator (LT1719, Linear Technology Inc.) and fed to a 3:1 tapered inverter driver (NC7WZ04, Fairchild Semiconductor Inc.), which in turn drives directly the gate of the MOS transistor. Note that the implemented gate-driving circuit conveniently

ensures the same gate signal duty-cycle irrelevant of the amplitude and phase of the outphaser's output signal.

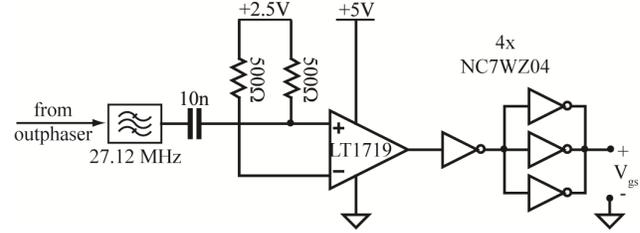


Figure 12. Gate-driving circuit employed in the PA of Fig. 11.

For illustrative purposes, Fig. 13 shows a photograph of the implementation of a single Class-E PA, clearly outlining the gate driver circuit. The outphaser's output (OUT1 in Fig. 9) is fed to the PA's IN port, while its OUT port connects directly to one of the four power combiner input ports.

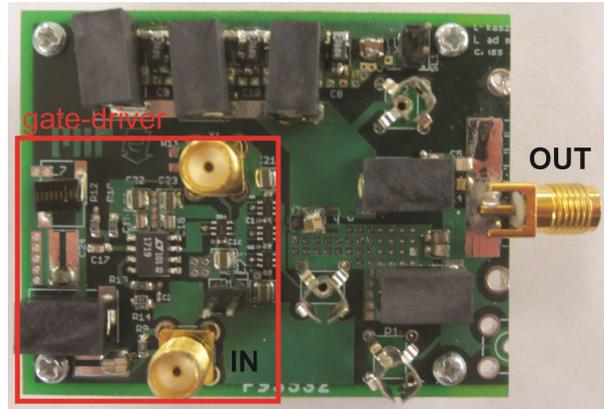


Figure 13. Photograph of a single implemented Class-E PA PCB (5.9 cm x 4.5 cm).

### C. The Power Combiner

Each of the combiner reactances  $X_1$  and  $X_2$  (see Fig. 3) were realized with a series combination of an inductor and a capacitor. This implementation blocks any direct-current (DC) paths from the combiner's input ports to its output port, and suppresses any harmonic content from the PAs. Moreover, it facilitates combiner tuning: any branch reactance can be easily adjusted by simply adding some extra capacitance in parallel with the already-mounted branch capacitor. Fig. 14 and table II depict the actual combiner implementation.

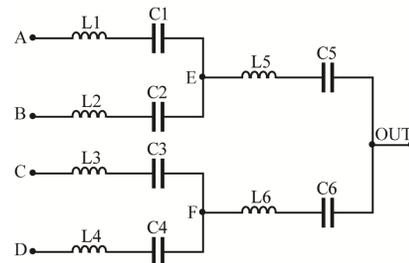


Figure 14. Power combiner implementation.

It is important to properly tune the combiner (adjust the  $X_1$  and  $X_2$  reactances to their intended values), as it has been found that the combiner's performance is very sensitive to variations in the reactance values. Even a 5% deviation in the reactance values may result in considerable degradation of the combiner's input admittance characteristics, including variation in the input admittance phase/susceptance. A simple methodology employed in tuning the combiner is briefly described here.

Starting with an unpopulated combiner printed-circuit board (PCB), C5, C6, L5, and L6 are populated first. Initially, slightly lower values for C5 and C6 are used (for example, 5% less than what is required). Ports E and F are loaded with  $50\Omega$ . A 27.12 MHz sinusoidal signal is injected into the output port (OUT) of the combiner, and the voltage waveforms at ports E and F are monitored. Small capacitance increments are added in parallel with C5 and C6 (for example, increments on the order of 1% of total value) until the waveforms at ports E and F have the same amplitude, and a relative phase shift determined by the desired branch reactance value. An analogous tuning procedure is applied to branches L1/C1 and L2/C2, and branches L3/C3 and L4/C4 with a sinusoidal signal injected respectively into ports E and F. Fig. 15 shows a photograph of the tuned combiner PCB, while Table II lists the utilized component values.

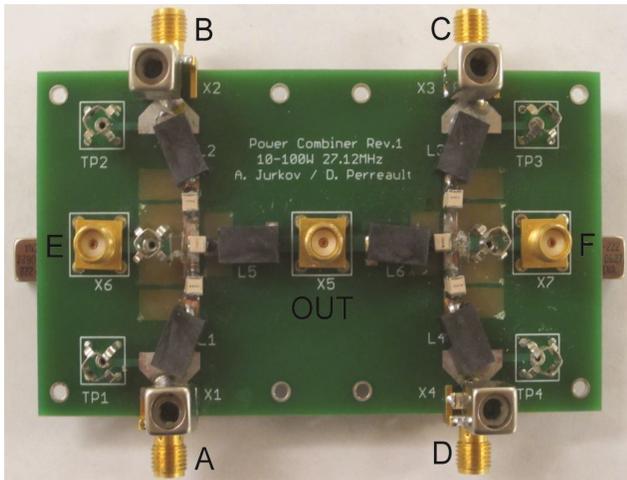


Figure 15. Photograph of the power combiner PCB (9.8 cm x 5.6 cm).

It is of interest to monitor the voltage waveforms at the combiner's input ports, and so, oscilloscope probe connectors (Part #: 131-4244-00, Tektronix Inc.) have been mounted in parallel with the SMA input-port connectors (TP1-TP4 in Fig. 15). However, the resultant parasitic capacitance (approximately 15 pF) at each of the combiner's input and measurement ports (the parallel combination of the SMA connector and the oscilloscope probe capacitance) can considerably affect the performance of the combiner and alter its input impedance characteristics. To address this issue, tunable inductors (7M2-332, Coilcraft Inc.) with a nominal inductance of 3.3  $\mu\text{H}$  are installed in parallel with the probe connectors (X1-X4, Fig. 15) to "resonate-out" the parasitic capacitances at 27.12 MHz. Although there is some small

parasitic capacitance associated with the other nodes of the power combiner circuit, their value has been measured to be no greater than 3 pF, and so their effect on the combiner's characteristics is negligible. Note however that during the combiner tuning procedure described above, oscilloscope probes are temporarily connected to ports E and F to monitor the voltage waveforms. In order to "resonate-out" the probes' parasitic capacitances, similar tuning inductors are temporarily installed in parallel with the probes, and are removed once after the tuning procedure is completed.

TABLE II. POWER COMBINER COMPONENT VALUES

Component	Value	Part #	Manufacturer
L1, L3	222 nH	132-14SMJL	Coilcraft Inc.
L2, L4	422 nH	132-18SMJL	
L5	307 nH	132-16SMJL	
L6	538 nH	132-20SMJL	
C1, C3	78.8 pF	ATC100B Capacitor Series	American Technical Ceramics Corp.
C2, C4	167 pF		
C5	57.9 pF		
C6	137 pF		

Since the proposed power combiner is implemented entirely with reactive components, it is ideally lossless. However, due to the finite Q-factor of the components used, some resistive combiner power loss is expected depending on the combiner's operating point and the respective combiner branch currents. Thus, we briefly examine the effect of the components' finite Q-factor on the combiner's efficiency.

According to the respective manufacturer's component datasheets, at the system operating frequency (27.12 MHz) inductors L1-L6 (see Fig. 14) have an approximate Q-factor of 90, while the tunable shunt inductors X1-X4 have a Q-factor of 25. Capacitors C1-C6 have a much higher Q-factor (nominally greater than 10,000), and so their resistive losses are negligible compared to those of the inductors. Fig. 16 depicts the simulated efficiency of the combiner due solely to resistive power losses associated with the components' finite Q-factors.

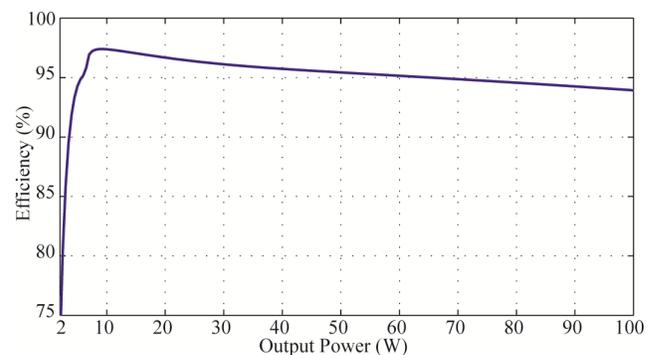


Figure 16. Simulated combiner efficiency including component Q-factor losses.

It can be seen that over an output power range of 10 W to 100 W (the 10 dB range over which the combiner has been

designed to operate), it exhibits a predicted efficiency above 94%. For output power levels below 10 W, the effective input-port impedances of the combiner are significantly dominated by reactive components (as can be also seen from Fig. 6), thus giving rise to considerable circulating currents (and resistive power losses), and hence resulting in a sudden drop in efficiency.

## V. COMBINER PERFORMANCE

In order to evaluate the performance of the power combiner and assess the validity of the proposed outphasing control law, the system is tested at various output power levels over approximately a 10 dB power range ratio. For a given desired output power (termed here "commanded" power) the PAs are outphased according to Fig. 4, with  $\theta$  and  $\phi$  selected for the corresponding power level from Fig. 5. Moreover, the PA's DC supply voltages are appropriately adjusted over the combiner's operating range to ensure that the amplitude of the fundamental component of their output voltage waveforms is always maintained at approximately 25 V for all output power levels (consistent with Fig. 4). Effectively, this results in driving the combiner with zero-output impedance PAs (similar to treating the PAs as ideal voltage sources). It is well recognized that this method for driving the combiner does not accurately reflect the constraints of a "real-life" application; dynamic modulation of the PA's DC supply voltage is not a luxury that one can typically afford in an actual power combining system. Nevertheless, it is important to clarify that the sole purpose of doing so here is to allow for an experimental verification of the power combiner's combining characteristics and evaluation of the effectiveness of the proposed outphasing law to control output power. The performance of an entire power amplifier system using the combiner is the subject of a future work.

### A. Experimental Setup

Four 10 M $\Omega$ , 8 pF oscilloscope probes (P6139A, Tektronix Inc.) were connected respectively to test points TP1-TP4 (see Fig. 15) to monitor the input voltage waveforms at the combiner's input ports and ensure correct inputs signal phases (within  $\pm 1^\circ$ ) and fundamental harmonic amplitudes. As was already mentioned, to mitigate the effect of capacitive probe loading on the combiner, tunable inductors (7M2-332, Coilcraft Inc.) were installed in parallel with the probe connectors to "resonate-out" the probe and connector capacitances at 27.12 MHz.

A 100 W, 30 dB attenuator (Part #: 690-30-1, Meca Electronics Inc.) loaded with the input channel of an oscilloscope (TDS3014B, Tektronix Inc.), set to 50 $\Omega$  input impedance, was employed as a load for the combiner. The VSWR, as seen from the combiner's output port, was determined to be approximately 1.04. The combiner output power was measured using a directional RF power meter (5010B, Bird Electronics Corp.). Fig. 17 shows photograph of the entire experimental setup.

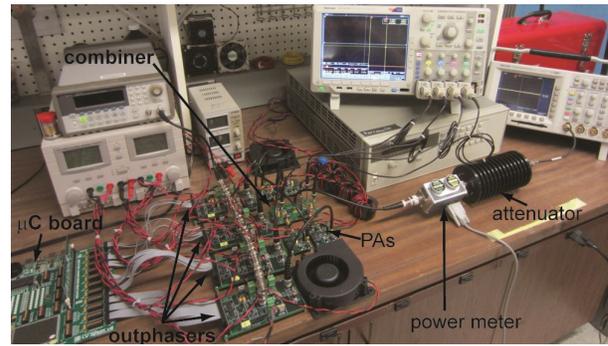


Figure 17. Photograph of the experimental setup.

### B. Combiner Performance Measurements

The relationship between the measured combiner output power and commanded power is plotted in Fig. 18. Ideally the output power should be equivalent to the commanded power (indicated with a dashed line in Fig. 18). The close agreement between the actual output power and ideal output power is evident. This demonstrates that the proposed outphasing control law can be effectively utilized in controlling the output power delivered to a load.

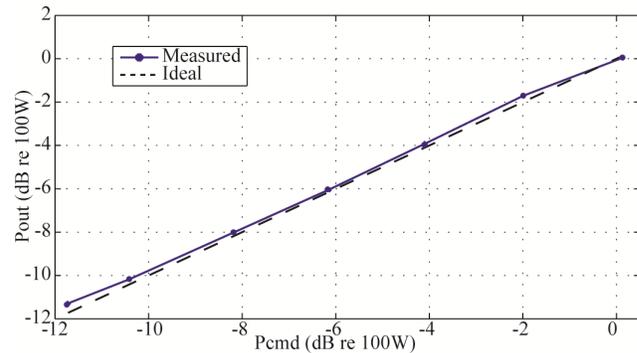


Figure 18. Measured combiner output power versus commanded output power.

It is also of interest to examine the efficiency of the entire combining and outphasing system. Here, system efficiency is determined by the ratio of output power delivered to the load to the total PA DC drain input power (i.e. excluding PA gate-driving power). Fig. 19 shows the measured system efficiency over a 10 dB output power range (plotted in red) with the error bars representing the  $\pm 5\%$  measurement accuracy of the power meter. The measured average PA efficiency curve (shown in blue) was obtained by first measuring independently, and then averaging the efficiencies of each of the four PAs loaded resistively over a range of output power levels, while maintaining a 25 V constant-amplitude fundamental frequency component of the PA output voltages. These efficiency measurements are consistent with the combiner driving methodology described earlier.

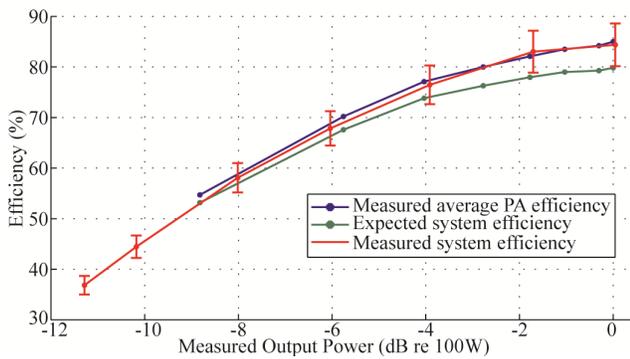


Figure 19. Measured overall system and PA efficiency versus combiner output power.

As can be seen from Fig. 19, the overall system efficiency is dominated by the PA losses. As it was mentioned earlier, variations in susceptive loading of the PAs (due to any susceptive components of the combiner's effective input admittances) can considerably mistune the output resonant tank of the PAs and introduce additional losses (termed here combiner/PA interface losses). Neglecting such interface losses, one would expect the overall system efficiency to be determined by the product of the PA and power combiner efficiencies. Fig. 19 shows the expected system efficiency for the present system (ignoring combiner/PA interface losses) obtained by multiplying the measured average PA efficiency with the combiner efficiency of Fig. 16. As can be seen, the expected system efficiency is within the uncertainty of the overall system efficiency measurements, suggesting that indeed, the combiner does maintain an overall resistive loading of the PAs over most of the operating power range.

Fig. 20 further shows the distribution of total PA input power among the individual PAs. As can be seen, the employed outphasing control law results in a relatively even loading of the PAs over most of the considered operating range.

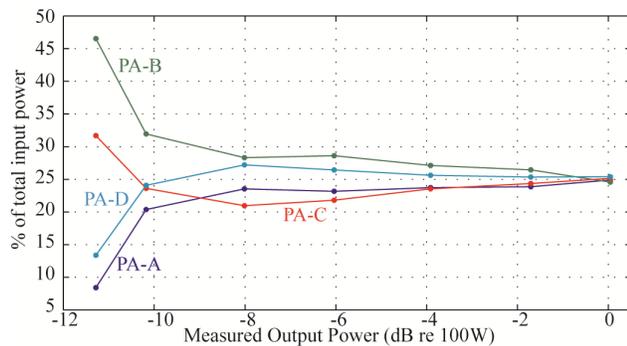


Figure 20. Total input power distribution among PAs versus combiner output power.

## VI. CONCLUSION

This paper presents the design, control and experimental validation of a new lossless multi-way outphasing system that offers major performance advantages over conventional outphasing and combining approaches. A new optimal phase outphasing control strategy is introduced that allows output power control through effective load modulation of the power amplifiers while minimizing admittance phase variations in loading. Moreover, we present the first-ever experimental demonstration of this new power combining and outphasing strategy. We describe a 27.12 MHz combining and outphasing system, and use it to experimentally evaluate its power-combining performance over a 10 dB output power range. It is demonstrated that the proposed outphasing control strategy is effective in controlling the system output power while evenly loading the power amplifiers over most of the operating range.

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