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FITMOS Modeling and Dynamic On-state Characteristic Evaluation

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***Abstract* – This paper presents a study of the detailed characteristics of the new Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS) developed at Toyota. FITMOS has tremendous potential for automotive applications due to its low on-resistance, improved temperature coefficient of resistance and low gate charge. During the study, the key characteristics of this novel FITMOS were investigated; a behavioral model was developed in SPICE for simulation and optimization purposes, and their applications in the design of automotive power electronics was explored. In this study, we also identify a previously unrecognized phenomenon in the FITMOS MOSFET. In particular, we show that the on-state resistance of the device depends on both frequency and peak di/dt at a given frequency[1]. This dynamic on-resistance variation can have a significant application impact.**

***Index Terms*—AC characteristics; capacitance modeling; DC-DC converters; FITMOS; I-V characteristics; optimization; on-resistance; reverse recovery; soft switching.**

I. INTRODUCTION

Power electronics are essential to many automotive applications, and their importance continues to grow as more vehicle functions incorporate electronic controls. MOSFETs are key elements in automotive power electronic circuits. MOSFET characteristics can strongly affect circuit size, cost and performance. Advantages in MOSFET technology are thus of great importance to the advancement of automotive electronics.

The new Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS) developed at Toyota has great potential for applications requiring devices with blocking voltages on the order of 60-100V. As described in [1] [2], the distinctive feature of the FITMOS is the use of floating islands and trench gates with a thick oxide layer at the bottom. This feature extends the breakdown voltage and maintains low on-resistance. In addition, the FITMOS also has low gate capacitance due to its floating island gate structure. As a result, with its low FOM [3], $R_{on}Q_{gd}$, FITMOS is expected to have a very competitive performance with commercial power MOSFETs in the automotive power electronics space.

This paper presents modeling of early generation FITMOS devices, which includes capacitance modeling, I-V characteristic modeling, and body diode reverse recovery modeling. These results were used in the development and experimental evaluation of a FITMOS-based prototype DC-DC converter design to validate the analytical results and provide a concrete demonstration of the impact of FITMOS transistors on power circuit designs. From studying the FITMOS-based converter, we demonstrate that the on-state resistance of the first-generation FITMOS devices shows a dependence on both switching frequency and peak di/dt. The dynamic on-resistance characteristic not only introduces discrepancies between static operation models and experimental results, but also affects the achievable design space and the suitable operating conditions of these new devices.

Section II presents the modeling result of the FITMOS. Section III reveals the AC characteristics of the on-resistance in the FITMOS and section IV concludes the paper.

II. FITMOS MODELING

Understanding the device parameters and their relations to loss mechanisms is important for utilizing the device better. For example, the gate capacitance determines the gating loss in hard switching; the output capacitance affects the switching loss and hence affects the optimum switching frequency; and the on-resistance is the key element for conduction loss. The modeling undertaken for FITMOS devices has three major parts: capacitance modeling; I-V characteristic modeling and body diode reverse recovery characteristic modeling. All the measurement data shown in this paper represent the averaged value among five sample devices.

[1] These characteristics were observed in early-generation FITMOS devices. It is our understanding that these characteristics have been eliminated in the more recent generation of FITMOS devices.

A. *Capacitance Modeling*

C_{OSS}, C_{ISS} and C_C are measured with an Agilent Impedance Analyzer 4395A at 1MHz using 201 points with a frequency range of 100kHz to 10MHz. From C_{OSS}, C_{ISS} and C_C:

$$C_{OSS} = C_{DG} + C_{DS} \tag{1}$$

$$C_{ISS} = C_{GD} + C_{GS} \tag{2}$$

$$C_C = C_{GS} + C_{DS} \tag{3}$$

we can extract out C_{GD}, C_{DS} and C_{GS}:

$$C_{DG} = \frac{C_{OSS}+C_{ISS}-C_C}{2} \tag{4}$$

$$C_{DS} = \frac{C_{OSS}-C_{ISS}+C_C}{2} \tag{5}$$

$$C_{DG} = \frac{-C_{OSS}+C_{ISS}+C_C}{2} \tag{6}$$

Capacitances C_{DG} and C_{DS} are functions of bias voltage. As a result, they need to be modeled as such. We use the junction capacitance equation to capture capacitance variation:

$$C(V) = \frac{C_{jo}}{(1+\frac{V}{\emptyset})^m} \tag{7}$$

in which C_{jo} is the zero-bias junction capacitance, m is known as the grading coefficient, and ø is the built-in junction potential. The values of the parameters in the equation are solved numerically based on least squares fit with the experimental data instead of physical modeling. The selected function models the capacitance accurately; the results are shown in Fig. 1 and Fig. 2.

B. *I-V Characteristic Modeling*

For I-V characteristic modeling, a behavioral model is used instead of physical model of the device since the traditional physical lateral MOSFET model may not model the vertical trench gate FITMOS properly. Moreover, the behavioral model is simpler and suitable for rapid simulation and calculation. There are two major operation regions for the MOSFET: triode region and saturation region.

In the triode region, the drain-source current I_{ds} is inversely proportional to the on-resistance R_{on}, and R_{on} is modeled in a function of gate-source voltage V_{gs} and threshold voltage V_t. For simplicity, and based on empirical observation, we treated the FITMOS device as being in triode region when V_{ds} is less than 0.2V since the current I_{ds} is linearly proportional to $1/R_{on}$ in this region. Fig. 3 shows the extracted 1/ R_{on} plot based on the slope of I_{ds} versus V_{ds} when V_{ds} is less than 0.2V.

When the V_{gs} is only slightly above the threshold voltage, V_{gs}-V_t is small; $1/R_{on}$ strongly depends on V_{gs}-V_t. $1/R_{on}$ will not keep on increasing to a very large number as V_{gs}-V_t continues to increase since R_{on} will saturate to its DC on-state value when V_{gs} is large enough. In order to model this transition accurately, we model the $1/R_{on}$ separately for both small and large values of V_{gs}. The modeling functions are extracted based on the best least square fit with the experimental data. Fig. 4 shows the modeling result of $1/R_{on}$ over a large range of V_{gs}-V_t.

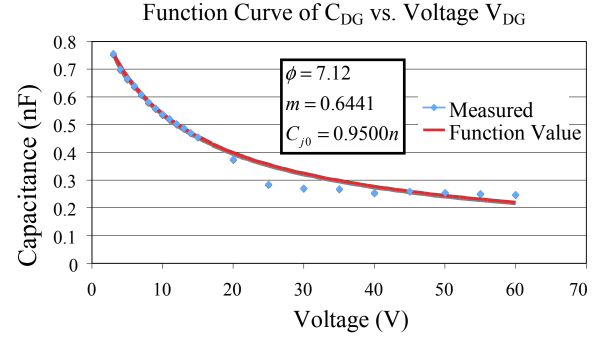


Fig. 1. The plot shows the C_{DG} modeling. Data is collected with bias voltage from 3V to 60V. When the bias voltage is below 3V, the device does not behave capacitively.

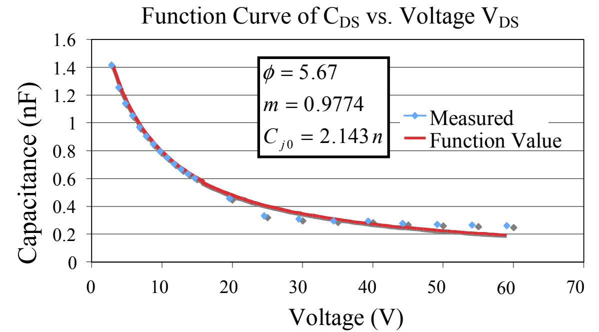


Fig. 2. The plot shows the C_{DS} modeling. Data is collected with bias voltage from 3V to 60V. When the bias voltage is below 3V, the device does not behave capacitively.

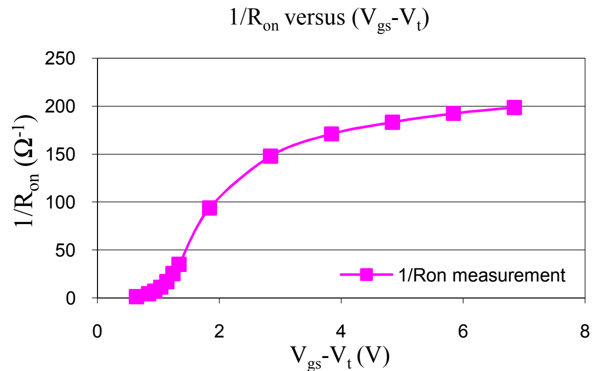


Fig. 3. $1/R_{on}$ versus (V_{gs}-V_t) plot. For large V_{gs}, R_{on} saturates to its DC on-state value: 5mΩ.

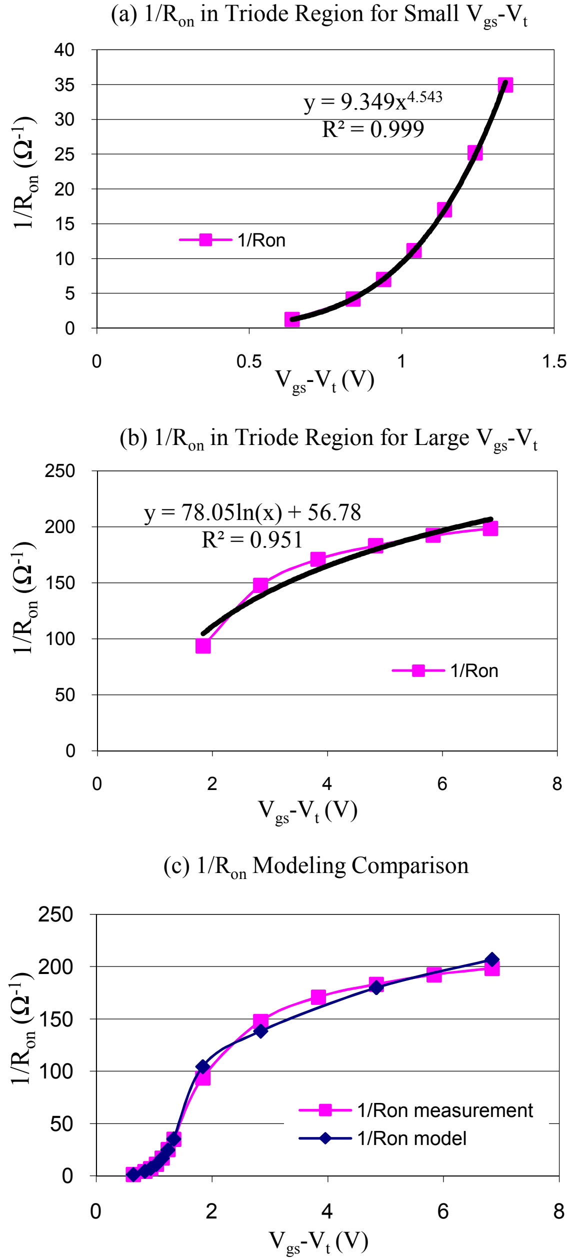


Fig. 4. These plots show the $1/R_{on}$ modeling and result comparison. Plots (a) and (b) show the equation fit for $1/R_{on}$ under small V_{gs}-V_t and large V_{gs}-V_t respectively. Plot (c) shows the overall result of the $1/R_{on}$ model.

The overall $1/R_{on}$ equation is (8)

$$\frac{1}{R_{on}} = \begin{cases} 9.35 \times (V_{gs} - V_t)^{4.54}, \ V_{gs} - V_t < 1.67 \\ 78.05 \times \ln(V_{gs} - V_t) + 56.78, \ V_{gs} - V_t \geq 1.67 \end{cases} \tag{8}$$

From the result shown above in Fig. 4(c), the function models the experimental results very well. As a result, in triode region, the drain-source current I_{ds} is modeled as linearly proportional to the drain-source voltage V_{ds}, with a slope of $1/R_{on}$ that is a function of V_{gs} and V_t:

$$I_{ds} = \frac{V_{ds}}{R_{on}} = \begin{cases} 9.35 \times (V_{gs} - V_t)^{4.54} \times V_{ds}, \ V_{gs} - V_t < 1.67 \\ (78.05 \times \ln(V_{gs} - V_t) + 56.78) \times V_{ds}, \ V_{gs} - V_t \geq 1.67 \end{cases} \tag{9}$$

In the saturation region, the I_{ds} is modeled with (10):

$$K(V_{gs} - V_t)^{\alpha} + \lambda V_{ds} \tag{10}$$

The variables K, α and λ are extracted from the numerical fit from the measured data. The measured I-V curves and their equation fit are shown in Fig. 5.

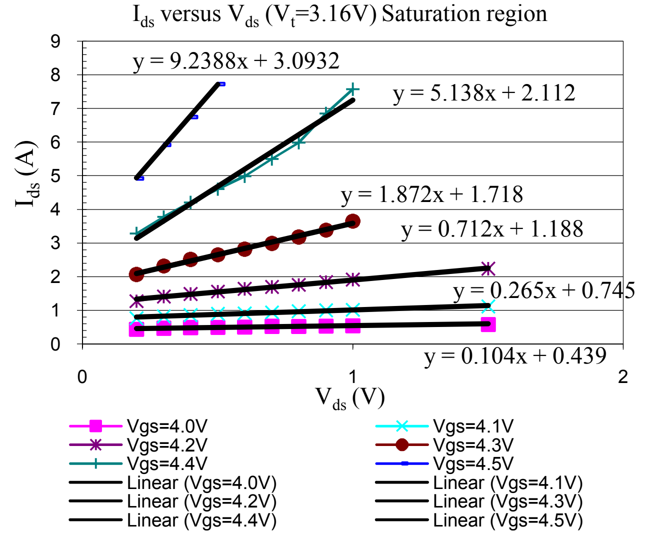


Fig. 5. Figure shows the measured I-V curves and their equation fit for the saturation region only.

$K(V_{gs}-V_t)^{\alpha}$ is the intercept of the extended I-V trendline in saturation with the y-axis, which is $V_{ds}=0$. λ is the slope of the linear trendline fit for the I-V curve in saturation, which is also in a function of V_{gs}-V_t. The values of those variables are extracted as follows:

$K = 0.92$

$\alpha = 4.34$

$\lambda = 0.61(V_{gs}-V_t)^{8.72}$

When the FITMOS operates in the saturation region, the I_{ds} model is:

$$I_{ds} = 0.92 \times (V_{gs} - V_t)^{4.34} + 0.61 \times (V_{gs} - V_t)^{8.72} \times V_{ds} \tag{11}$$

After we combine the two operation regions, linear region and saturation, the complete final equation is shown in (12).

$$I_{ds} = \begin{cases} \begin{cases} 9.35 \times (V_{gs} - V_t)^{4.54} \times V_{ds}, \ V_{gs} - V_t < 1.67 \\ (78.05 \times \ln(V_{gs} - V_t) + 56.78) \times V_{ds}, \ V_{gs} - V_t \geq 1.67 \end{cases}, \ V_{ds} < 0.2 \\ 0.92 \times (V_{gs} - V_t)^{4.34} + 0.61 \times (V_{gs} - V_t)^{8.72} \times V_{ds}, \ V_{ds} \geq 0.2 \end{cases} \tag{12}$$

Fig. 6 shows the comparison between our equation and experimental data. A very good match is observed in the figure, which is accurate enough for our SPICE simulation.

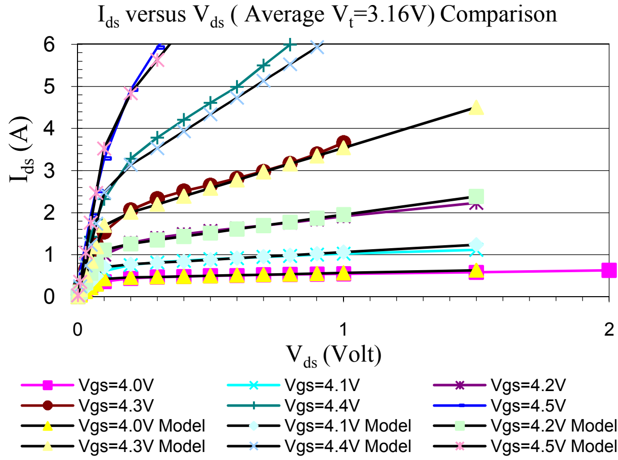


Fig. 6. This shows the measured FITMOS I-V characteristic and our behavioral model. Our model matched with the measurement very well.

C. *Reverse Recovery Modeling*

Reverse recovery of the body diode is a further important loss mechanism in the power MOSFET. This loss is due to the excess minority carrier storage in the body diode junction and is frequency dependent. It happens when the diode is rapidly switched from forward biased to reverse biased. The diode has to sweep out the excessive minority carriers in the junction before it can block a large negative voltage. So this behavior does not only add more loss from discharging the excess minority carriers, but also increases the switching losses. Capturing this power- and frequency-dependent loss can improve the accuracy of our SPICE device model. The reverse recovery measurement setup is shown in Fig. 7.

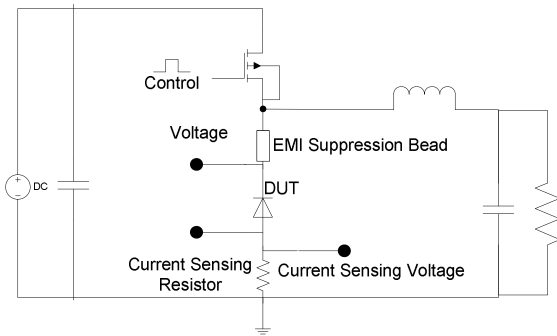


Fig. 7. This is the schematic of the measurement setup for reverse recovery. The body diode current is measured by a ground-referenced sensing resistor.

The measurement setup is a modified buck dc-dc converter. The gate and source of the low side MOSFET is shorted. When the control MOSFET is off, output current goes through the body diode in the low-side MOSFET. Once the high-side control MOSFET is turned on, the current will be drawn by the high-side MOSFET. The body diode in the low-side MOSFET is forced to turn off. During this transition, we can capture the reverse recovery behavior of the body diode. Parasitic ringing in the circuit can significantly affect the measurement result. As a result, this measurement is very sensitive to loop parasitics; extra care is taken to minimize the parasitic inductance in the measurement loop. For the current sensing, four 1.2Ω 0802 surface mount resistors are connected in parallel, which gives a very flat resistive response up to 100MHz. This bandwidth should be sufficient for us to obtain accurate measurement even accounting the high order harmonics in the current waveform. Furthermore, in order to eliminate the high frequency ringing for our measurement, an EMI suppression bead was used in the drain of the testing MOSFET device. For standard comparison, the di/dt of the diode falling current is set to be 100A/us by controlling the gate resistance of the high-side MOSFET. The body diode reverse bias voltage is equal to the input voltage of the testing buck converter, which is 42V. The measurement is repeated for three different current settings by controlling the output power to be 100W, 200W and 400W.

The detailed characteristics are shown in table I:

TABLE I
FITMOS REVERSE RECOVERY CHARACTERISTICS

I_f	I_{rm}	T_a	T_{rr}	Q_a	Q_{rr}
3.4A	-0.9A	22nS	104nS	12.9nC	67.6nC
6.7A	-0.56A	31nS	140nS	12nC	69.5nC
9.1A	-0.53A	34nS	167nS	11.1nC	68.5nC

I_f is the forward diode current; I_{rm} is the reverse peak current; T_a is the time for the diode current to drop from zero to negative maximum; T_{rr} is the reverse recovery time; Q_a is the charge for excessive minority carrier in the Ta period only; Q_{rr} is the total reverse recovery charge.

A sample of reverse recovery behavior from our experimental results is shown in Fig. 8. From the plot, we can see that the diode cannot block reverse voltage until the excessive minority carriers are discharged.

The diode transit time T_t in SPICE is often used to approximate the reverse recovery charge. To model the excessive minority charge in the junction [4] [5] [6], the minority carrier life-time constant is extracted base on our measurement by using (13):

$$T_t = \frac{T_a}{\ln(1-\frac{I_f}{I_{rm}})} \tag{13}$$

I_f is the forward diode current and I_{rm} is the reverse peak current. T_a is the time for the diode current to drop from zero to negative maximum. The average T_t is calculated as 12.4ns

based on the data on Table I. The junction capacitance is modeled with the C_{DS} capacitance.

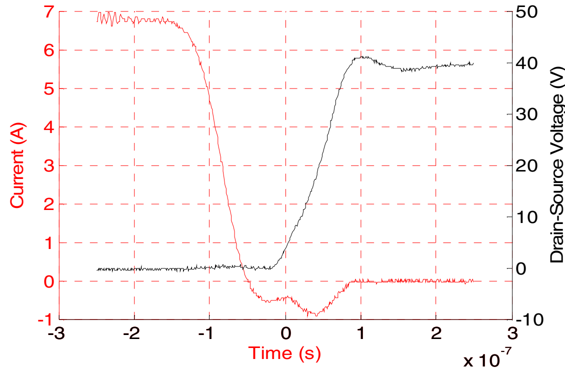


Fig. 8. This shows the measurement result sample for the reserve recovery behavior.

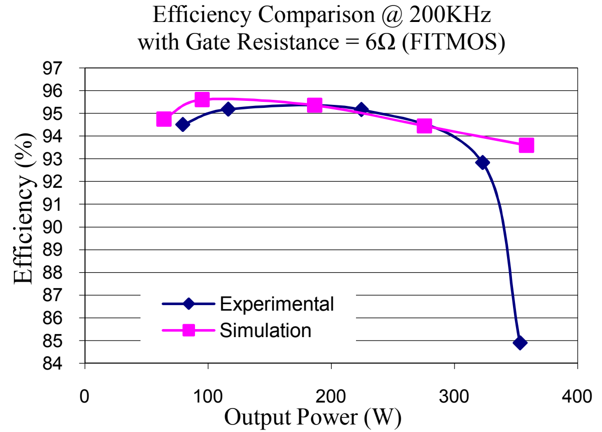
D. Model Validation

A prototype 14V to 42V synchronous boost converter has been developed for use in verifying the modeling results and for exploring the suitable applications of FITMOS devices. The converter operated in hard-switching mode at settable switching frequency. The output power of the converter can be up to 400W. A picture of the prototype converter is shown in Fig. 9

Fig. 9. This is the picture of the prototype converter. The heatsink is oversized for safety experiment purpose.

Overall, the model predicts the performance of the converter reasonable well; Fig. 10 shows the efficiency comparison between our FITMOS model and the experimental data for fixed frequency and various output powers.

From the plot, we can see that the simulation matches the experimental data over a wide output power range, 50W to 300W. Below 300W, our model has no more than 2% error. But at powers approaching 400W, the converter suffers from V_{ds} saturation, and hence the efficiency decreases rapidly. This problem will be discussed in section III.



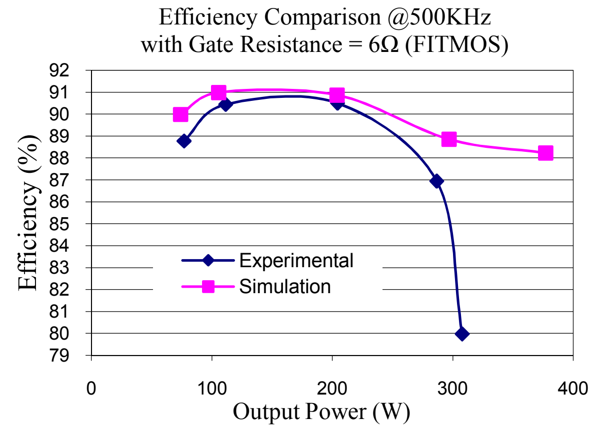


Fig. 10. The top plot shows the efficiency comparison between our FITMOS model with the experimental data at switching frequency of 200kHz; the bottom plot shows the efficiency comparison at switching frequency of 500kHz. An inductor value of 16uH is used.

Besides operating the converter in hard-switching mode, the converter is designed to operate under zero-voltage soft-switching conditions at high di/dt. Under “resonant pole” soft-switching operation (with inductor current ripple ratio exceeding unity to enable ZVS switching), the overlap loss in the device is eliminated. As a result, the simulation predicts that there will be noticeable improvement on the converter performance. The simulation and comparison to experimental results are shown in Fig. 11.

The experiment result shows no performance improvement under soft-switching for FITMOS, which means there is extra loss mechanism under high current ripple conditions that is not captured in the model. These noticeable discrepancies between model and experiment are found at high power and high current ripple conditions. These are explained by the dynamic variation of on-resistance as described in section III.

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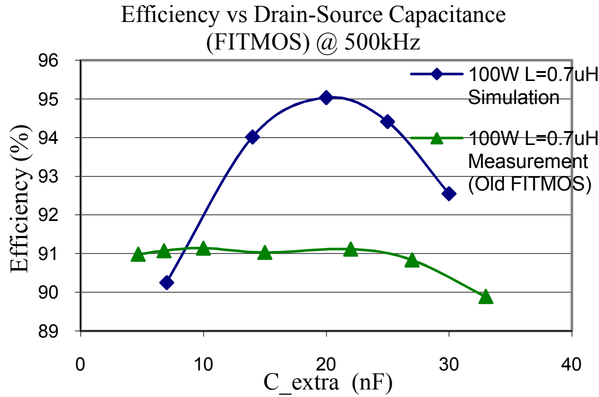
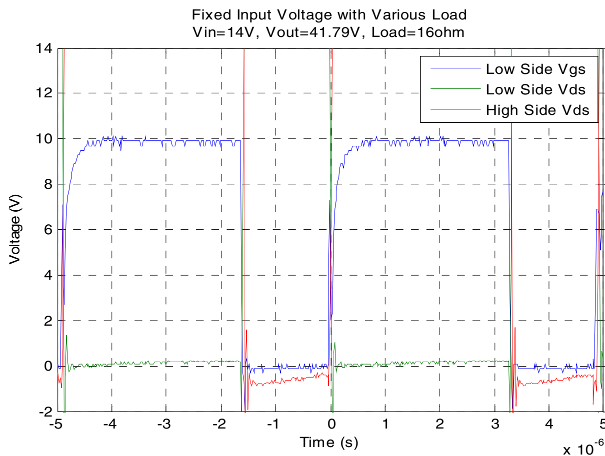
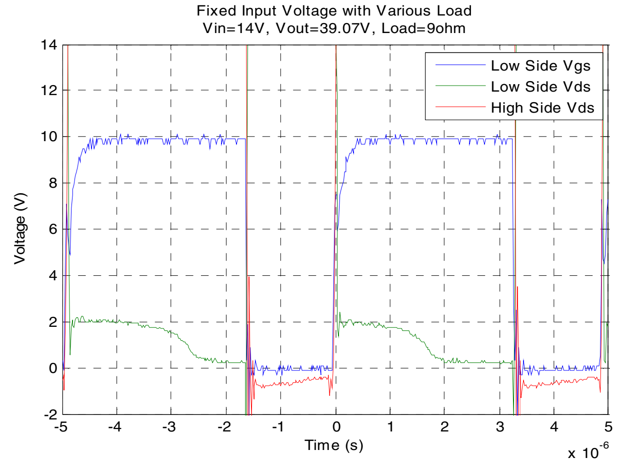


Fig. 11. Figure shows the converter soft-switching performance comparison between simulation and measurement result at 100W output power with an inductor value of 0.7uH. C_extra is the external drain source capacitance added across the lower device to achieve soft-switching.

III. DYNAMIC ON-STATE CHARACTERISTICS

From last section, we have observed that the converter efficiency drops significantly at high output power, over 300W in Fig. 10. After carefully studying the circuit behavior, an unexpected phenomenon is observed in the drain-source voltage V_{ds} of the low-side MOSFET device for a time period after the device is turned on. As the drain-source current I_{ds} that is carried is increased to a certain level (e.g., by adjusting load resistance or input voltage at constant duty ratio), the drain-source voltage of FITMOS does not drop quickly to the normal low level ($R_{ds\text{-}on}$*I_{ds}) that is expected. Instead, it temporarily drops to a 2-3V saturation level (or voltage step level) when the switch is turned on, and only drops to a low level as expected after a long delay time that depends on operating point. When I_{ds} is increased sufficiently, this voltage step can extend across the whole on period for the switch. This situation significantly increases the loss in the device, and hence lowers the efficiency of the converter. Samples of this behavior are captured in Fig. 12.





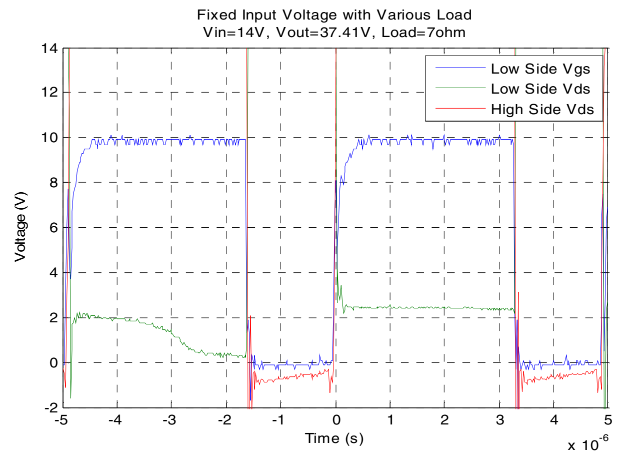


Fig. 12. Samples of the V_{ds} saturation phenomena. The top figure shows no V_{ds} saturation problem at low current. As the current increases, the Vds saturation problem starts to occur and get worse.

This V_{ds} saturation problem was eliminated in a subsequent generation of FITMOS devices.

We also studied the discrepancies between model and experiment under high current ripple (di/dt) condition in soft-switching. During examination, an increased V_{ds} is observed during the on period when the device is experiencing high di/dt in the drain-source current, even with the parasitic inductance effect extracted out. A sample of V_{ds} measurement under high di/dt is shown in Fig. 13.

From Fig. 13, V_{ds} of 0.31V is measured. For 14V input voltage, 42V output voltage and load resistance of 20Ω, the dc input current is about 6.3A. Under the soft-switching condition, the inductor current has 200% peak-to-peak current ripple ratio. As a result, the peak current in the device is 2x6.3=12.6A. Assuming the device temperature is 150°C (the actual device temperature is much less than 150°C) and the on-resistance is about 8.5mΩ, the calculated V_{ds} should be 12.6A x 8.5mΩ = 0.107V, which is much less than the measured value. We can also extract the package parasitic inductance effect on the V_{ds} measurement. From the

measurement, when the FITMOS is turned on, a ringing frequency of 18MHz is observed. Since we have a 10nF external capacitance across the drain and source of the device for soft-switching, which is much larger than the parasitic capacitance on the device, we can extract the parasitic inductance in the package from the ringing frequency:

$$L = \frac{1}{C}\left(\frac{1}{2\pi \times f_{ringing}}\right)^2 \approx 7.94nH \tag{14}$$

The voltage offset caused by the parasitic inductance is

$$V_{offset} = L\frac{di}{dt} \approx 0.083V \tag{15}$$

At 500kHz switching frequency of 60% duty ratio with current ripple of 12.6A, di/dt is calculated to be about 10A/us. With the additional offset voltage from the parasitic inductance, the total calculated V_{ds} is only 0.19V, which is over 30% less than the measured value. From the experimental converter measurements and MOSFET switching waveforms we observed and their comparison to simulation results, we believe that the effective FITMOS on-resistance is dependent on the dynamics of the drain-source current.

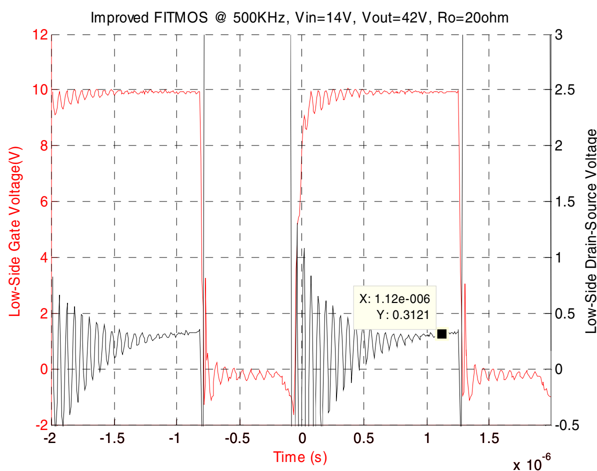


Fig. 13. A sample of the V_{ds} measurement under soft-switching at 500kHz. An inductor value of 16uH was used in the converter.

Two aspects of the dynamic on-resistance behavior are investigated: one is the on-resistance dependence on current frequency (at constant di/dt); the other is the on-resistance dependence on dynamic current change di/dt (at constant drive frequency). The experimental setup is shown in Fig. 14.

A 10V V_{gs} is continuously applied to the device to maintain the MOSFET on during the whole experiment. In this way, we can prevent the parasitic ringing from affecting our measurement during the switching transition of the device. A RF power amplifier is used to provide a sinusoidal current through the device. A 50Ω load is connected in series with the MOSFET to match the output impedance desired by the power amplifier. By measuring the drain-source voltage V_{ds}, drain-source current I_{ds} and the phase θ between V_{ds} and I_{ds}, we can extract the real on-resistance in the MOSFET from $V_{ds}/I_{ds}*\cos(\theta)$, if the voltage and current waveform are purely sinusoidal with negligible distortion. Measurement data is taken 5 minutes after the system is turned on and reaches thermal steady-state. The MOSFET is mounted to a heatsink to reduce the temperature variation effect on the result. Since the testing current is relative low and the power dissipation of the device is small, temperature variation effect on the on-resistance should be negligible.

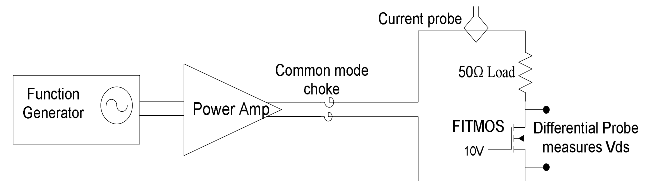


Fig. 14. Equipmental setup for the dynamic on-resistance measurement. A RF power amplifier ENI 3100LA is used to drive the MOSFET.

summary of the experimental results is shown in Fig. 15 and Fig. 16.

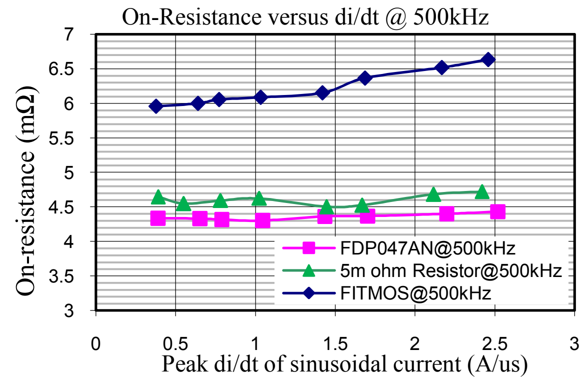


Fig. 15. On resistance variation under different peak di/dt with a given frequency.

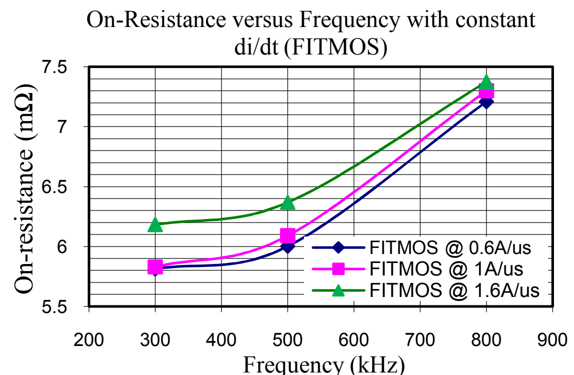


Fig. 16. On resistance versus different drain-source current frequency with constant peak di/dt.

For comparison, we also include test results for a commercial MOSFET FDP047AN and a simple 5mΩ current sensing resistor. Under 500kHz sinusoidal current, regardless the peak di/dt, the on-resistance of the commercial device FDP047AN and the resistance of the current sensing resistor remain constant. As shown in Fig. 15, however, the on-resistance of the FITMOS device increases 10% when the peak di/dt increases from 0.4A/us to 2.5A/us. In addition, the FITMOS on-resistance also increases with higher frequency with constant di/dt as illustrated in Fig. 16. As a result, the conduction loss of the FITMOS increases with higher di/dt and switching frequency. This dynamic on-resistance variation will cause increasing discrepancies between expected performance in simulation and measurement as di/dt and switching frequency increase. Even though the soft-switching technique can eliminate the switching loss for the devices, the extra conduction loss due to the larger on-state resistance in FITMOS under the high di/dt condition in the "resonant pole" soft-switching offsets the gain. FITMOS has a very competitive low DC on-resistance compared to commercial power MOSFETs of similar blocking voltage (R_{on}=5mΩ @ 25ºC, V_{GS}=10V and V_{DSS}=80V). However, in order to maintain FITMOS's competitive performance, its on-resistance AC characteristic has to be considered during the converter design process. The advantage of going for a higher di/dt in some converter topologies has to overcome the loss from the increased on-resistance.

IV. CONCLUSION

This paper presents detailed modeling of novel FITMOS transistors. We modeled device capacitance, on state behavior and diode reverse recovery. The resulting behavioral SPICE model shows accurate device performance prediction with respect to experimental measurements in a prototype 14V-to-42V boost converter. However, discrepancies between the simulation and measurement arise at high operating frequency and ripple current. These discrepancies can be explained by the previously unrecognized dynamic characteristic of the on-state resistance in the FITMOS. With the detailed characterization, we can identify how to best utilize the FITMOS characteristics to benefit power circuit design and quantify the gains that can be achieved through their use.

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