

Two-Stage Power Conversion Architecture for an LED Driver Circuit

Seungbum Lim, John Ranson, David M. Otten, and David J. Perreault

Department of Electrical Engineering and Computer Science

Massachusetts Institute of Technology

Cambridge, Massachusetts 02139-4307

Email: sblim@mit.edu

Abstract—This paper presents a merged-two-stage circuit topology suitable for efficient LED drivers operating from either wide-range dc input voltage or ac line voltage. This two-stage topology is based on a soft-charged switched-capacitor pre-regulator/transformation stage and a high-frequency magnetic regulator stage. Soft charging of the switched capacitor circuit, zero voltage switching of the high-frequency regulator circuit, and time-based indirect scale current control are used to maintain high efficiency, high power density, and high power factor. Two implementations of the proposed architecture are demonstrated: a wide input voltage range dc-dc converter and a line interfaced ac-dc converter. The dc-dc converter shows 85-95% efficiency at 20 W power across 25-200 V input voltage range, and the ac-dc converter achieves 88% efficiency with 0.93 power factor at 8.4 W average power.

I. INTRODUCTION

LED lighting promises unprecedented reductions in energy consumption, but comes with an as-yet unmet demand for high power density, high efficiency, and high-power-factor LED drivers [1]. A survey of commercial LED drivers illustrates this: Considering a group of commercial line-interfaced LED drivers in the 3-30 W output power range, we have found efficiencies in the range of 64-83% and power factors of 0.59-0.96, with no systems achieving both high efficiency and high power factor. The switching frequencies of these drivers were in the range of 57-104 kHz, with correspondingly low power densities below 5 W/in^3 . The size of these drivers was uniformly dominated by magnetic components, and in each case the driver represented a major contribution to overall system size. It may be concluded that power conversion electronics continue to represent a major limitation in solid-state lighting, and that significant improvements in driver efficiency, power density and power factor will be necessary to meet market needs.

This paper introduces a merged two-stage architecture, associated circuit design, and controls to address these challenges. The proposed approach is suitable for conversion from both wide-range dc voltage and ac-line voltage. Section II of the paper presents the overall system requirements we target along with an overview of the design considerations for LED drivers in this space. Section III of the paper presents the proposed architecture, circuit topology, and controls. Section IV of the paper presents experimental results demonstrating the proposed approach, including implementations for both

wide-range dc voltage and ac line voltage. Finally, Section V concludes the paper.

II. SYSTEM REQUIREMENTS AND DESIGN CONSIDERATIONS

The system architecture we adopt targets LED driver circuits operating at low-to-moderate power levels and wide-ranging, grid-scale input voltages. We introduce circuit implementations and controls suitable for power levels of up to a few tens of watts, wide-range input voltages of up to 200 V (e.g., compatible with 120 V_{rms} ac operation), and LED string voltages in the range of 30-40 V. Furthermore, for ac-line applications we seek designs having high power factor (e.g., Power factor > 0.9), while for dc-input applications we seek efficient operation across a wide input voltage range (e.g., 25-200 V input). Lastly, we target substantial miniaturization of the driver through a combination of architecture, circuit topology, and adoption of greatly increased switching frequencies.

We begin with an overview of the design considerations in achieving miniaturization of converters in this application, which operate at high voltages and low powers and across a wide range of input voltage. To attain greater miniaturization, increases in switching frequency are necessary because the values of inductors and capacitors vary inversely with switching frequency. However, the sizes of passive components do not necessarily decrease monotonically with frequency, owing to magnetic-core loss, voltage breakdown, and heat transfer limits [2]–[7]. Consequently, achieving substantial miniaturization through high frequency operation further relies upon appropriate passives design and careful selection of circuit topology to minimize the demands placed upon the passive components, especially the magnetic components.

A further consideration is that while passive component size may be made smaller with increased frequency, size reduces relatively slowly with frequency in practice. Moreover, some parasitic elements, such as semiconductor device parasitic capacitances and inductances, do not scale at all with operating frequency. Consequently, the effects of parasitics become increasingly important as frequency increases. To achieve miniaturization through extreme high-frequency operation, an effective circuit topology should inherently absorb important parasitic components in its operation.

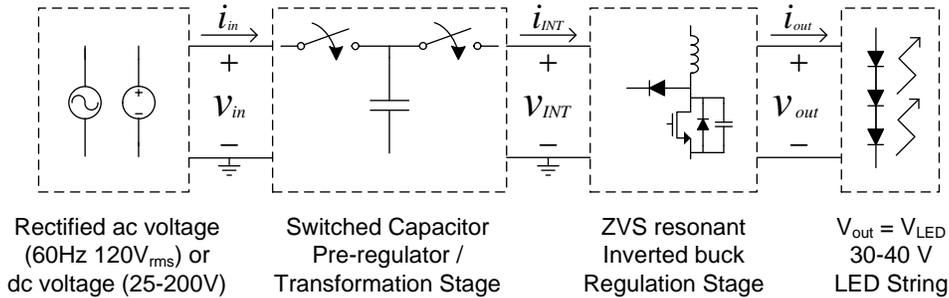


Fig. 1. A merged two-stage conversion architecture having a switched capacitor first stage that provides voltage pre-regulation and transformation, and a high-frequency magnetic stage that provides fine regulation of the output.

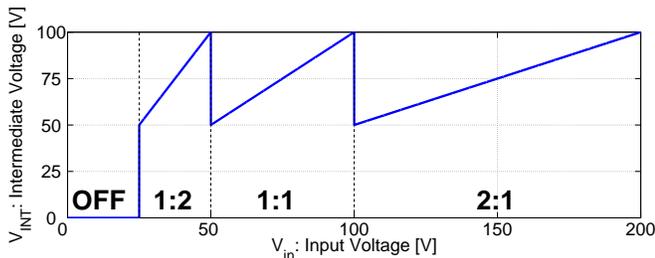


Fig. 2. The voltage transformation characteristic of the first switched capacitor stage in a dc-dc converter.

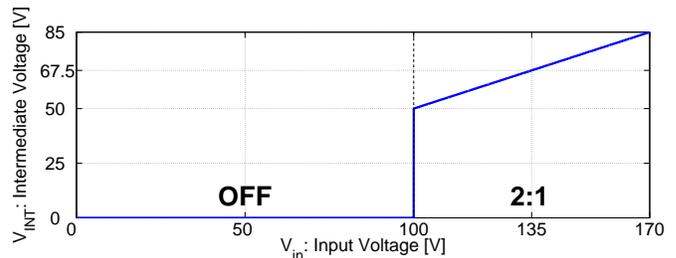


Fig. 3. The voltage transformation characteristic of the first switched capacitor stage in an ac-dc converter.

A third consideration relates specifically to operating characteristics at high voltages and low power levels. Converters operating at high-voltages and low-currents operate at high impedance levels, and consequently utilize relatively large inductors and small capacitors (e.g., characteristic impedance $Z_0 = \sqrt{L/C}$ scales as V/I [2]). Furthermore, inductor and capacitor values scale down with increasing resonant frequency (e.g., $\omega_0 = 2\pi f = 1/\sqrt{LC}$). Thus, for a given topology, increasing frequency beyond a certain point may lead to capacitance values that are too small to be practically achievable (e.g., given parasitics), placing a practical bound on frequency and miniaturization. For miniaturization of converters at high voltage and low-power, it is preferable to select system architectures and circuit topologies that require relatively low characteristic impedance values (i.e., small inductances and large capacitances) to reduce constraints on scaling up in frequency.

Lastly, operating range and control are important architectural considerations. We consider designs operating either from a wide range dc voltage or from an ac line voltage, such that the system sees a wide range of input voltages. At the same time, zero-voltage switching (ZVS) or near-ZVS is necessary to reduce capacitive discharge loss of the switch and to achieve extreme high-frequency operation at high voltages. However, because circuit waveforms change with conversion ratio, soft switching is often difficult to maintain across a very wide voltage range. It is thus important to seek designs that can maintain these desirable operating waveforms across the wide input voltage range.

III. SYSTEM ARCHITECTURE AND CIRCUIT TOPOLOGY

A. System Architecture

To address the above considerations, a merged-two-stage architecture is proposed, as shown in Fig. 1. The first stage is a variable-topology switched-capacitor (SC) circuit operating at moderate switching frequencies (e.g., tens to hundreds of kHz). The SC circuit can achieve high power density and efficiency at these frequencies because it employs only switches and capacitors. However, the SC converter alone cannot efficiently provide the fine voltage regulation capability needed in this application [8]. Instead, this stage serves both to reduce the voltage range over which the second stage needs to operate, and to reduce the maximum voltage level (and hence impedance level) for which the second stage must be designed, in keeping with the design considerations described in the previous section.

The second stage is a magnetic-based stage that provides both additional voltage transformation and fine voltage regulation, and is operated at high frequency (e.g., HF, 3-30 MHz) in order to minimize magnetic component size. High-frequency operation is more readily achieved with high efficiency in the second stage because it operates at lower voltages and (in some cases) a smaller range of conversion ratios than the first stage. Furthermore, as described below, the topology of the second stage is selected such that it requires relatively small inductor values and inherently absorbs parasitic capacitance as part of circuit operation, in keeping with the design considerations described in the previous section. This HF regulation stage is selected to minimize device voltage stress, and to enable

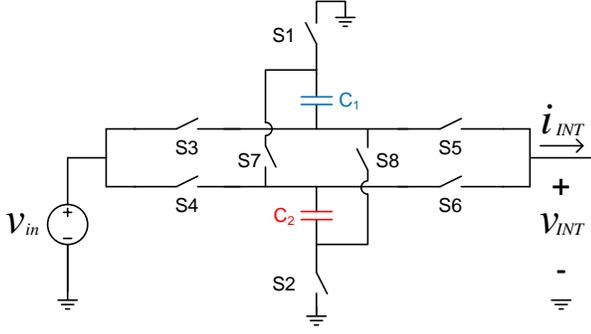


Fig. 4. Schematic of the switched capacitor pre-regulator/transformation stage of the merged two-stage converter.

TABLE I

CONTROL OF ON-STATE SWITCHES OF THE SWITCHED CAPACITOR STAGE.

mode	state 1	state 2
1:2	S1, S3, S6, S8	S2, S4, S5, S7
1:1	S3, S5, S4, S6	
2:1	S1, S4, S5, S8	S2, S3, S6, S7

partitioning of the device requirements into “slow switching and high-voltage first stage” and “fast switching and low-voltage second stage” device categories. Moreover, as detailed below the two-stages are designed to operate together (merged) in a manner that enables higher efficiency and higher power density than could be achieved in a conventional architecture having separate stages [9], [10]. We describe each of these stages in more detail below.

B. First Stage – Switched Capacitor Circuit

1) SC Power Stage:

The first stage is a variable-topology SC circuit that requires only two energy transfer capacitors and provides nearly continuous input and output currents. To create a suitable intermediate voltage over which the second (regulation) stage can run, the SC transformation stage is operated in different conversion modes, depending upon input voltage. It can operate in three different conversion modes (i.e., 1:2, 1:1, and 2:1 conversion modes). For a wide-input-range dc-dc converter system operating from 25-200 V (8:1 conversion ratio), all three of these conversion modes are utilized. For an ac-dc converter system operating from ac line voltage, sufficiently high power factor can be achieved through operation only over a limited voltage range in 2:1 mode, as will be detailed in Section III-D. The relations between input and intermediate voltage at the output of the SC first stage are shown in Fig. 2 and Fig. 3 for wide-range dc-dc conversion and ac-dc conversion respectively. The SC circuit and control are illustrated in Fig. 4, Table I, and Table II. It should be noted that in 1:1 conversion mode the control circuit can be controlled to select S3/S5 current path, S4/S6 current path, or

TABLE II
OPERATING STATES OF THE SWITCHED CAPACITOR STAGE

mode	state 1	state 2
1:2		
1:1		
2:1		

both S3/S5 and S4/S6 current path. Additionally, our system is designed to “merge” operation of the two stages. A benefit of such a “merged two-stage” architecture [9], [11] is that the second high-frequency stage can “soft charge/discharge” the capacitors in the SC stage, reducing loss and/or required capacitor size. Essentially, the HF stage charges and discharges the SC stage as a current source load, enabling the SC circuit to attain the low conduction losses of the SC “fast switching limit” while operating at the low frequencies of the SC “slow switching limit” [8], [12]. The SC circuit thus can provide higher efficiency and higher power density even at relatively low operating frequencies.

The SC circuit serves multiple functions. First, by switching among different conversion modes, it can take a wide-range input voltage (25-200 V) and provide a narrow-range intermediate voltage (50-100 V). That is, an 8:1 input voltage range is reduced to a 2:1 intermediate voltage range. Second, it reduces the peak input voltage for which the HF second stage must operate, lowering device voltage stress and better matching the desired voltage range of the HF regulation stage. Moreover, it improves the impedance levels of the HF stage (i.e., increasing allowable capacitance levels and reducing the required inductance values of the second stage). Lastly, the SC circuit provides a tremendous degree of flexibility to the system, operating either from a very wide 8:1 dc input voltage range (25-200 V) or from a 120 V_{rms} ac-line voltage.

2) SC Stage Control and Driver Circuit:

The SC transformation stage is controlled by the microcontroller, independent of the HF regulation stage operation. The switches of SC stage are controlled with the fixed frequency 50% duty ratio on/off signals from the microcontroller. To decide the frequency of the SC circuit, two specifications should be considered: the dissipation of SC stage and the intermediate voltage ripple over which HF stage can stand to operate. Because of the soft-charging characteristic of the SC stage in our topology, the main dissipation at the SC circuit comes from hard-switching of the switches. The loss of the SC stage is thus proportional to the frequency of the SC circuit. The other consideration is the intermediate voltage

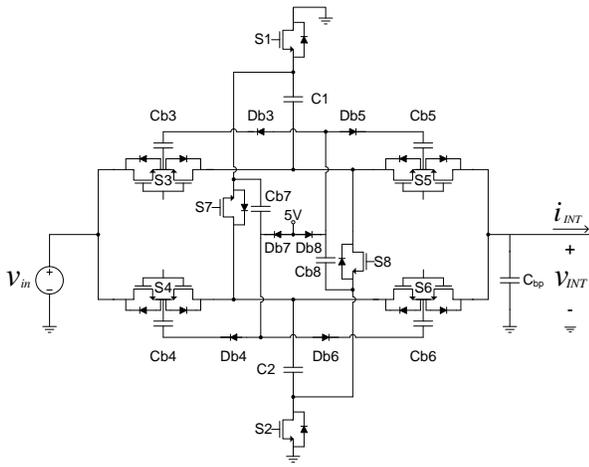


Fig. 5. Schematic of the switched-capacitor pre-regulator/transformation stage with bootstrap diodes.

ripple that the HF regulation stage can tolerate. For a certain energy transfer capacitor value in the SC circuit (i.e., C1, C2 of Fig. 4), the intermediate voltage ripple increases as the frequency is reduced. Therefore, the frequency should be chosen to compromise between dissipation of the SC stage and intermediate voltage ripple. Our current HF regulation stage topology can tolerate substantial voltage ripple in the intermediate voltage; thus, the SC circuit can be operated at frequencies as low as 20-30 kHz with acceptable capacitor size.

Each driver circuit for every switch in the SC circuit was configured with isolating gate driver IC (ADuM5240), low-side gate driver (FAN3111C), and bypass/bootstrap capacitors. The isolating gate driver offers two functions: charging the bootstrap capacitors at start-up and shifting control signals to the flying switch control port. After the circuit is powered up and the bootstrap capacitors are charged, the isolating gate driver IC only operates to shift control signal levels attaining better power efficiency with external bootstrap diodes (i.e., by turning off the internal transformer-based DC-DC power supply capability of the isolating gate driver IC, ADuM5240). The switched capacitor circuit is realized with actual transistors (S1-S8), bootstrap diodes (Db3-Db8), energy transfer capacitors (C1, C2), and bootstrap capacitors (Cb3-Cb8) as shown in Fig. 5. The bootstrap configuration shown in Fig. 5 applies simultaneously for all three conversion modes. It should be noted that even 1:1 conversion mode the bootstrap technique is achieved by alternatively selecting either the S3, S5 current path or the S4, S6 current path with 50% duty cycle instead of keeping all switches S3, S4, S5, and S6 on continuously. It can be seen that, as shown in Fig. 5, the switches S3, S4, S5, and S6 are designed with back-to-back connection of two transistors to block bidirectional voltage.

C. Second Stage – HF Regulation Circuit

1) HF Regulation Power Stage:

The second stage of our converter, shown in Fig. 6, is

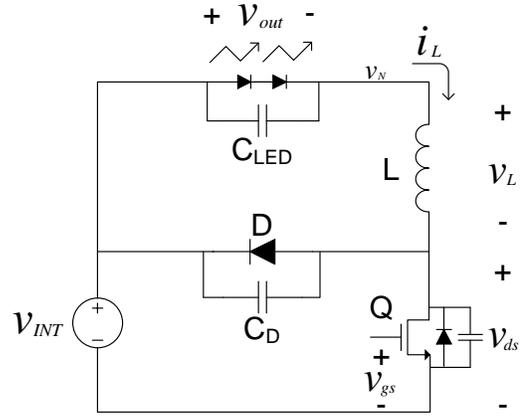


Fig. 6. Schematic of the second magnetic-based regulation stage. This converter stage is designed to operate at high frequency.

a resonant transition discontinuous-mode inverted buck converter operating at frequencies around 10 MHz with ZVS soft-switching over part of its input voltage range, and near-ZVS soft-switching over the rest of the range. Over the portion of its operating range for which it is soft switched, the converter waveforms are similar to those of the “Quasi-Square-Wave” ZVS buck converter [13], though the control techniques are different. The buck converter is “inverted” in the sense that it is designed with “common positives” so that the active switch is referenced to a constant ground potential. Referencing the switch in this way is of great practical importance in achieving extreme high-frequency operation [2].

The buck converter operation cycles through four phases in a HF switching cycle, as illustrated in Fig. 7. During Phase 1, the switch is on, and the inductor current i_L ramps up linearly. In Phase 2, the switch turns off, and the switch drain to source voltage v_{ds} rings up to the intermediate voltage (i.e., V_{INT} , HF regulation stage input voltage). In Phase 3, the diode conducts, and i_L ramps down to zero. In the Phase 4, both diode and switch are off, and the inductor rings with the net capacitance at the switch drain node. Inductor current i_L rings negative and v_{ds} rings down to zero or near zero volts (down to $V_{in} - 2V_{LED}$). At this point, the switch is turned back on, phase 1 is entered and the cycle repeats.

2) HF Regulation Stage Control and Driver Circuit:

The specific characteristic of the LED load is that the LED load voltage is nonlinear with respect to the load current and is almost determined by the pre-defined LED string forward drop voltage. Therefore, to control output power level, the current conducting in the LED string should be adjusted; the fast closed-loop estimated current control circuit introduced here modulates switch on-time of the HF second stage to adjust the power level. The ability of the controller to provide closed-loop control at the high operating frequency of the system is central to the effectiveness of the proposed approach.

The HF stage control circuit is designed to operate at

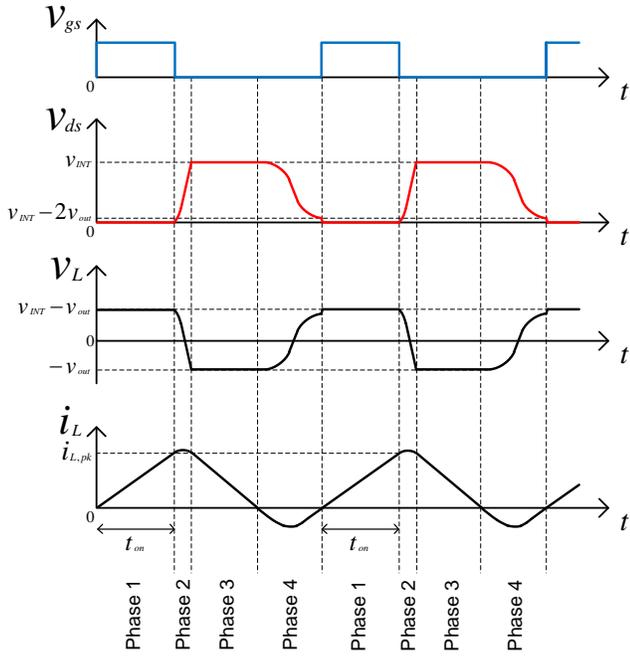


Fig. 7. Operating phases of the high-frequency resonant transition inverted buck converter. The converter achieves zero-voltage switching over most of its range, and low-loss near zero-voltage switching over the remainder of the operating range. Power control is readily achieved by varying the on-state duration of the switch (phase 1).

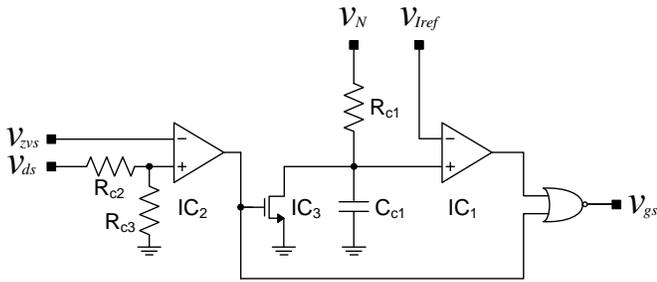


Fig. 8. Schematic of the HF regulation control circuit. This control circuit is designed to regulate the current by changing switch on-time, and to operate at zero-voltage or near zero-voltage switching conditions.

high frequencies (to beyond 10 MHz) using comparators, integrators, and logic circuits. The essence of the control circuit is shown in Fig. 8. The control circuit drives the logic-referenced gate-source voltage v_{gs} of the switch (turning it on and off) as determined by the drain-source voltage v_{ds} , zero-voltage-switching threshold voltage V_{zvs} , cathode node voltage of LED output voltage V_N (e.g., $V_N = V_{INT} - V_{LED}$), and peak-current threshold voltage V_{Iref} ; that is, each voltage signal in Fig. 8 is directly connected to the same voltage node of HF power stage as shown in Fig. 6, with voltages referenced to the switch source voltage.

This HF control circuit regulates switching based on two thresholds using a pair of comparators: a near-ZVS threshold turn-on and (indirect) peak-current threshold turn-off.

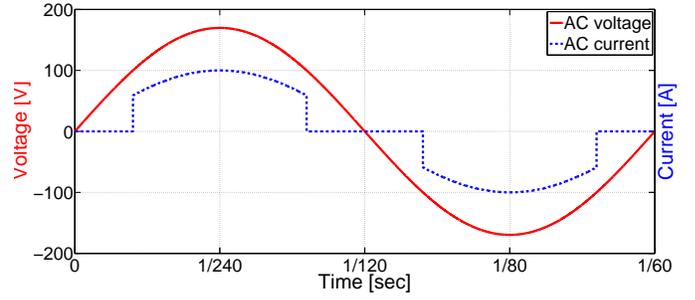


Fig. 9. Waveform of the sinusoidal ac voltage and "clipped sinewave" ac current. The clipped-sinewave current pattern operating over a 108 degree range for each 180 degree half-cycle yields a power factor of 0.95 (this corresponds to a 100 V "cut in" voltage for a 170 V peak sinusoidal voltage). Operating over a 120 degree range per half-cycle yields a power factor of 0.97.

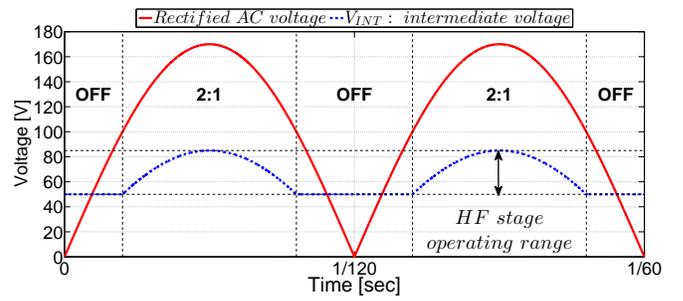


Fig. 10. The voltage transformation characteristic of the first switched capacitor stage over the line cycle in an ac-dc converter.

First, comparator IC_1 determines the on-time duration of the switch by comparing V_{Iref} and the (approximate) integral of voltage V_N . When the transistor begins its phase 1 on-state duration, v_{ds} is low, comparator IC_2 output is low, and transistor IC_3 is off such that the voltage on C_{c1} approximately integrates voltage V_N . After the capacitor C_{c1} is charged for a short duration Δt , $V_{IC1,+} = V_N \Delta t / (C_{c1} R_{c1}) = (V_{INT} - V_{LED}) \Delta t / (C_{c1} R_{c1})$. The output of IC_1 goes high and turns off the switch (v_{gs} low) when $V_{IC1,+}$ becomes larger than V_{Iref} (i.e., $t_{on} = V_{Iref} C_{c1} R_{c1} / V_N = V_{Iref} C_{c1} R_{c1} / (V_{INT} - V_{LED})$). Because the HF stage is always operating at the edge of discontinuous conduction mode, the inductor current i_L during the switch is on-state is as follows:

$$i_L = \frac{V_{INT} - V_{LED}}{L} \Delta t \quad (1)$$

$$i_{L,pk} = \frac{V_{INT} - V_{LED}}{L} t_{on} = \frac{V_{Iref} C_{c1} R_{c1}}{L} \quad (2)$$

Thus, the voltage V_{Iref} directly modulates switch turn-on time to regulate peak current at the inductor, regardless of the HF stage input and output voltage.

Second, the turn on of the switch (ending phase 4 and starting phase 1) is determined by comparator IC_2 . After the switch turns off at the end of phase 1, resistor-divided v_{ds} voltage goes above v_{zvs} , and transistor IC_3 turns on,

TABLE III
COMPONENTS OF THE SC STAGE AND HF STAGE

SC power stage			
C1, C2	energy transfer capacitor	$1\mu F$, Ceramic 100V	
S1 ~ S8	switch	EPC2012, GaN 200V 3A HEMT FET	
Cb3 ~ Cb8	bootstrap capacitor	$1\mu F$, Ceramic 16V	
Db3 ~ Db8	bootstrap diode	DFLS1150, Diodes Inc. 150V 1A Schottky	
C_{bp}	bypass capacitor	$2 \times 10nF$, Ceramic 100V	
SC stage control/driver circuit			
isolator / <i>isoPower</i>		ADum5240, Analog Devices	
low-side gate driver		FAN3111C, Fairchild	
HF power stage			
L	inductor	$2 \times 422nH$, Coilcraft Maxi Spring Air core	
D	diode	STPS10170C, ST 170V 10A Schottky	
Q	switch	EPC2012, EPC GaN 200V 3A HEMT FET	
C_{LED}	output capacitor	DC Configuration	$10\mu F$, Ceramic 50V
		AC Configuration	$10\mu F$, Ceramic 50V $820\mu F$, Aluminum 50V
HF stage control/driver circuit			
IC1, IC2	comparator	LT1711, Linear Technology rail-to-rail comparator	
IC3	inverter	SN74LVC2G06, Texas Instrument Inverter with open-drain outputs	
R_{c1}	resistor	$100k\Omega$	
R_{c2}	resistor	$200k\Omega$	
R_{c3}	resistor	$10.5k\Omega$	
C_{c1}	capacitor	$10pF$, Ceramic 50V	
low-side gate driver		NC7SZ02, Fairchild Tiny Logic Two-input NOR gate	

discharging the voltage on C_{c1} , resetting the past-integrated C_{c1} voltage for the on-time duration in the next cycle. When the inductor current decreases down to zero at the end of phase 3, phase 4 begins and the switch drain-source voltage starts to ring down. When v_{ds} rings down and divided v_{ds} goes below v_{zvs} , the output of IC_2 goes low, the control circuit turns on the switch again, and the cycle repeats. V_{ZVS} is set such that - including logic delays - the switch is turned on at the correct point in the drain-voltage ringdown (ending phase 3).

D. AC configuration

In an ac-dc converter high power factor is desired in addition to high efficiency and high power density. In commercial applications a power factor of at least 0.9 is desired, while in residential applications a power factor of 0.7 is acceptable. To attain high power factor, the input current waveform from the ac-line voltage should be proportional to the sinusoidal voltage waveform. In cases where the voltage waveform is sinusoidal and the current waveform is “clipped” to zero for low voltages (e.g., where the converter drops out of operation near voltage zero crossings), the current waveform providing the highest power factor is a “clipped” sinewave in phase with the voltage, as illustrated in Fig. 9. For a “cut in” voltage of 100 V (for a 170 V peak sinusoid), a power factor of > 0.95 is realized with a clipped sinusoid.

Proposed ac-dc converter is designed to approximate the current draw pattern of Fig. 9, with a “cut in” voltage of 100 V. Both the SC first stage and HF second stage are turned off below 100 V voltage range, and the output load is buffered by

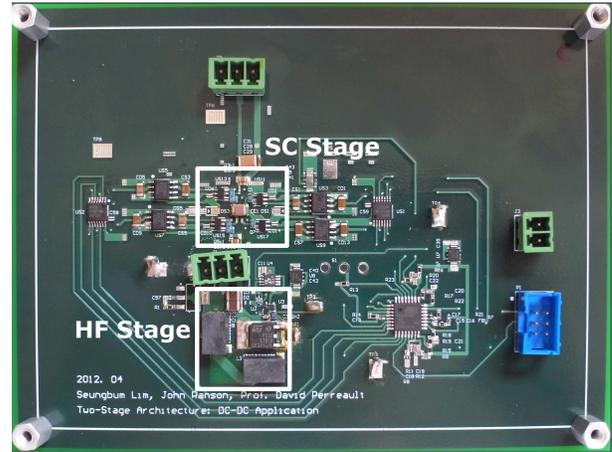


Fig. 11. Photograph of experimental prototype dc-dc converter with switched-capacitor stage and HF regulation stage outlined.

output capacitor during this off period. It should be noted that, as shown in Fig. 10, the SC stage operates in 2:1 conversion mode when the ac input voltage is above 100V and is in the off-state during the rest of the cycle. The intermediate voltage (i.e., the voltage which HF regulation stage operates) remains at 50 V during this off duration because both stages are turned off. The HF regulation stage thus operates with intermediate voltage above 50 V in this case.

When the rectified ac voltage is above 100 V, the merged two-stage circuit is controlled to yield an input current that approximates a clipped-sinusoidal waveform. The filtered in-

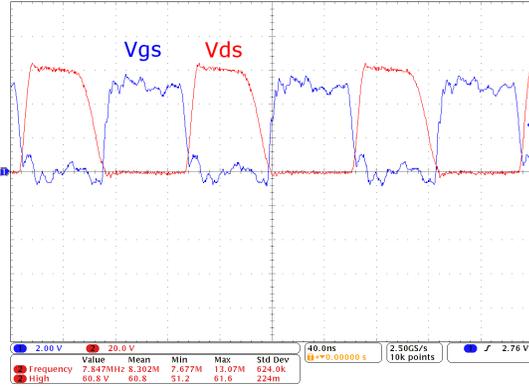


Fig. 12. Experimental v_{gs} and v_{ds} waveforms showing zero-voltage switching (x: 40ns/div, y- v_{gs} : 2V/div, y- v_{ds} : 20V/div). The input voltage is 60 V and the output is a 35 V, 12.15 W load. The converter operates at 7.85 MHz under this condition.

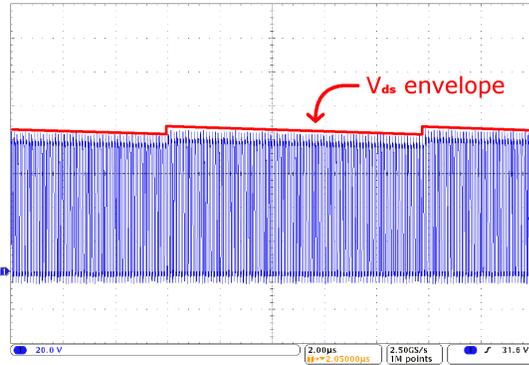


Fig. 13. Experimental measured switch drain-source voltage v_{ds} waveform of the HF regulation stage of the merged two-stage dc-dc converter prototype (x: 2 μ s/div, y: 20V/div). Note that the envelope of the switch voltage v_{ds} shows the soft-charging of the first switched-capacitor stage by the second HF stage (merged two-stage operation). The modulation of the HF stage switch drain voltage is caused by variations in the intermediate voltage between the two stages.

put current is proportional to inductor peak current $i_{L,pk}$ of the HF regulation stage, which is directly changed by V_{Iref} threshold voltage of the HF control circuit as described above. This V_{Iref} threshold voltage is adjusted properly over the low-frequency envelope of the ac line cycle by the microcontroller, and the unfolded approximately clipped-sinusoidal input current flows from the ac line voltage.

IV. EXPERIMENTAL RESULTS

Two implementations of the proposed converter have been developed. One operates from a wide-range dc input voltage (25-200 V dc), while the second operates with a front-end diode rectifier from 120 V_{rms} ac line voltage. The components and parameters chosen for the dc-dc converter and ac-dc converter implementations are listed in Table III. Some additional auxiliary bypass capacitors, resistors, protection diodes are used to connect the converter circuit to the microcontroller. Fig. 11 shows a photograph of the dc-dc converter implementation.

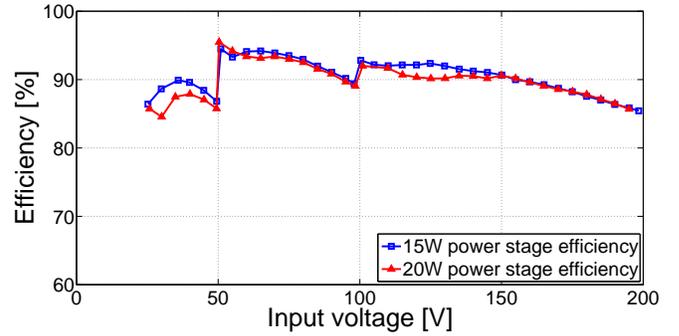


Fig. 14. Power stage efficiency of the merged two-stage converter prototype dc-dc converter configured to operate from a wide-range dc input of 25-200 V. Power stage efficiency is shown for two regulated output power levels (15 W and 20 W) across the input voltage range.

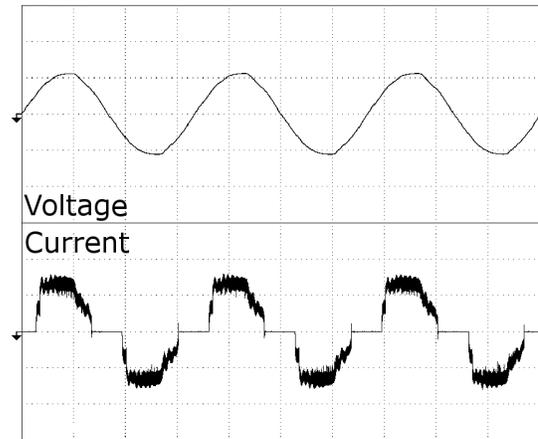


Fig. 15. Experimental input voltage and current of a prototype merged two-stage converter operated from the ac line (x: 5ms/div (top): 150V/div, (bottom): 100mA/div). The prototype achieves a power stage efficiency of 88% and a 0.93 power factor using only commercially-available devices and components. Operation is shown for 35 V at 8.4 W load power.

Shown in Fig. 12 are experimental switch gate voltage v_{gs} and switch drain voltage v_{ds} waveforms of the HF stage in the merged two-stage converter operating at 7.8 MHz for a 60 V dc input voltage and a 35 V output at 12.15 W load; this illustrates the ZVS soft-switching and high-frequency operation of the HF stage. Fig. 13 shows how the envelope of the switch drain voltage v_{ds} is modulated owing to variations in the intermediate voltage at the output of the first stage; this illustrates the soft-charging/discharging of SC circuit energy transfer capacitors by the HF second stage.

Measurement of the dc-dc converter power stage efficiency (i.e., excepting control and driver circuit losses) for various power and input voltage levels is shown in Fig. 14. It can be seen that the converter has a peak power stage efficiency of 95% with $V_{in} = 50$ V, $V_{out} = 35$ V, at an output power of 20 W. The microcontroller, SC stage bootstrap driver, HF stage driver, logic, and linear regulator circuits dissipate 0.6 W regardless of output power level (these loss components were not optimized in this prototype design).

Fig. 15 shows experimental input voltage and current waveforms of the merged two-stage ac-dc converter implementation (including a full-bridge rectifier and EMI filter in front of the SC stage). For an 8.4 W load, the converter operates at 88.3% efficiency, and 0.93 power factor from a 120 V_{rms} 60 Hz ac line.

V. CONCLUSION

A merged two-stage power conversion architecture and associated circuit topology for LED driver applications are demonstrated. This approach is specifically designed to address the challenges of low-power conversion from high and wide-range input voltages. The proposed power converter can be used in both dc-dc and ac-dc applications with low device stress, high efficiency, high power density, and high power factor. The experimental prototypes of dc-dc and ac-dc converter are implemented and presented along with good experimental results. Through appropriate control and merged operation between the SC transformation and HF regulation stages, soft-charging of the SC stage and ZVS switching of the HF stage are achieved. Additionally, this proposed architecture and topological approach are likewise expected to be applied to not only this LED driver circuit but also a variety of electrical applications which have wide-range dc input voltage or ac line input voltage.

REFERENCES

- [1] "Multi-year program plan fy09-fy14: Solid-state lighting research and development," *Office of Energy Efficiency and Renewable Energy, US Dept. of Energy by Navigant Consulting, Radcliffe Advisors, and SLS*, 2008.
- [2] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, Feb. 2009, pp. 1–14.
- [3] A. Rand, "Inductor size vs. q: A dimensional analysis," *Component Parts, IEEE Transactions on*, vol. 10, no. 1, pp. 31–35, Mar 1963.
- [4] W. Odendaal and J. Ferreira, "Effects of scaling high-frequency transformer parameters," *Industry Applications, IEEE Transactions on*, vol. 35, no. 4, pp. 932–940, Jul/Aug 1999.
- [5] W.-J. Gu and R. Liu, "A study of volume and weight vs. frequency for high-frequency transformers," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, Jun 1993, pp. 1123–1129.
- [6] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4 μ a quiescent-current dual-mode digitally controlled buck converter ic for cellular phone applications," *IEEE Journal of Solid State Circuits*, vol. 39, no. 12, pp. 2342–2348, 2004.
- [7] J. Hu, "Design of low-voltage, high-bandwidth radio-frequency power converters," Ph.D. dissertation, Massachusetts Institute of Technology, 2012.
- [8] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841–851, March 2008.
- [9] R. Pilawa-Podgurski, D. Giuliano, and D. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *39th IEEE Power Electronics Specialists Conference*, 2008.
- [10] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. PP, no. 99, pp. 1–11, 2012.
- [11] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," in *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, Sept. 2011, pp. 479–482.
- [12] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," in *IEEE Computers in Power Electronics Workshop*, 16–19 July 2006, pp. 216–224.
- [13] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *Power Electronics, IEEE Transactions on*, vol. 3, no. 2, pp. 183–191, Apr 1988.