

# Integrated CMOS DC-DC Converter with Digital Maximum Power Point Tracking for a Portable Thermophotovoltaic Power Generator

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**Abstract**—This paper presents an integrated maximum power point tracking system for use with a thermophotovoltaic (TPV) portable power generator. The design, implemented in  $0.35\ \mu\text{m}$  CMOS technology, consists of a low-power control stage and a dc-dc boost power stage with soft-switching capability. With a nominal input voltage of 1 V, and an output voltage of 4 V, we demonstrate a nominal peak conversion efficiency over 94% (peak efficiency over 95%), at a power level of 300 mW. The control stage uses lossless current sensing together with a custom low-power time-based ADC to minimize control losses. The converter employs a fully integrated digital implementation of a peak power tracking algorithm, and achieves a measured tracking efficiency above 98%. A detailed study of achievable efficiency versus inductor size is presented, with calculated and measured results.

## I. INTRODUCTION

The static conversion of heat to electricity through thermophotovoltaic (TPV) systems was first proposed in the 1950s [1]. Recently, advances in material science, most notably in low-bandgap semiconductors and photonic crystals, has enabled the development of TPV power generators with significantly higher power density and conversion efficiency than what was previously achievable. Thermophotovoltaics, while similar to photovoltaics (PV), has several key differences. The wavelengths of light captured by TPV systems is mostly in the infrared (IR) region ( $1\text{-}2.5\ \mu\text{m}$ ), compared to light in the visible spectrum that is captured by conventional photovoltaics. For this reason, TPV diodes have considerably lower bandgaps than PV cells ( $0.8\text{-}0.5\ \text{eV}$ ), to enable the conversion of lower-energy photons. Furthermore, TPV power generation is often achieved not directly from sunlight (although it is possible to do so), but from a thermal emitter that is heated up through various means. Because the radiated thermal output power of the emitter can be controlled, and the TPV cell distance from the emitter can be made very small, TPV cells can be made to operate at power densities more than two orders of magnitude higher than solar PV cells [2]. Fig. 1 shows the centimeter-scale TPV power system that is the motivation for this work. The heat source, a silicon micro-fabricated fuel reactor [3] that generates radiant heat, is surrounded by GaInAsSb TPV diodes with bandgap of  $0.54\ \text{eV}$  [4], power electronics, and heatsinks. The system, suitable for centimeter-scale power generation,

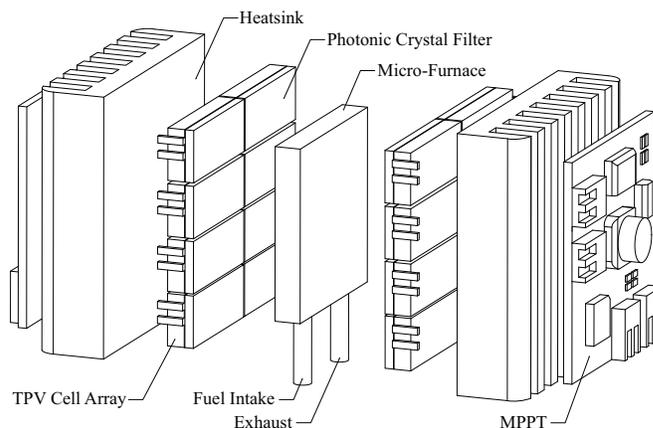


Fig. 1. Illustrative drawing of burner and TPV cells for portable power generation.

allows multiple fuel options, and promises high energy density and high efficiency. Another attractive feature of the system is the lack of any moving parts, which enables long lifetime and robust operation.

Much of the previous work on TPV power generation has focused on device-level performance, with little attention given to the system-level considerations [5], [6]. As described in [7], substantial performance improvements can be realized with the proper integration of power electronics in the system architecture. In this paper, we present an integrated maximum power point tracking system developed in  $0.35\ \mu\text{m}$  CMOS for use in the system depicted in Fig. 1. This MPPT system includes both power point tracking controls and an integrated dc-dc boost converter. Although the application we are describing in this work is a micro-generator TPV system, the approach has applications in other TPV systems such as solar-TPV, radioisotope TPV, as well as for energy harvesting with conventional photovoltaic cells.

Section II of the paper gives an overview of the electrical characteristics of the TPV cells, and the system-level challenges that we seek to address. Section III presents our power management system architecture, and section IV provides a detailed analysis of the fully-integrated control architecture

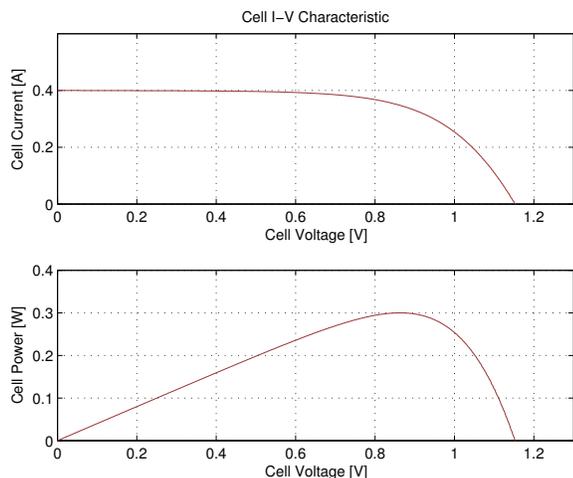


Fig. 2. I-V (top) and P-V (bottom) characteristic of 4 series-connected TPV cells used in this work for a typical operating irradiation.

to achieve maximum power point operation. In section V we show the design and operation of the integrated power stage, together with experimental and model-based design insights into the trade-off between converter efficiency and size, in particular as it pertains to the magnetics design. Experimental results are presented in section VI, and section VII concludes the paper.

## II. TPV CELL CHARACTERISTICS

Shown in Fig. 2 are current and voltage characteristics of four series-connected GaInAsSb TPV cells [4], when operated under typical conditions in the micro-generator. As can be seen in the bottom graph of Fig 2, there is a specific cell voltage ( $V_{mpp}$ ) that corresponds to maximum power output, the *maximum power point* (MPP). The parameter  $V_{mpp}$  changes with cell junction temperature and incident irradiation, making continuous tracking of  $V_{mpp}$  required for maximum power output. A detailed description of the system architecture of the TPV power generator can be found in [2], [7]. Our integrated CMOS maximum power point tracker is designed to improve the power density and conversion efficiency of the overall system through the use of compact, high-efficiency power electronics.

## III. SYSTEM OVERVIEW

The maximum power point tracker we have developed is illustrated in the schematic drawing of Fig. 3, alongside the other system components. The power tracker consists of two primary structures: the control stage and the power stage. The task of the control stage is to provide the duty cycle command to the power devices to ensure that the TPV cell is operating at its most efficient point – the maximum power point. Many different techniques [8] have been proposed to implement the maximum power point tracking functionality. In this work, we use Perturb and Observe (P&O) [9]. Since the duty cycle ( $D$ ) directly affects the input voltage (cell voltage)

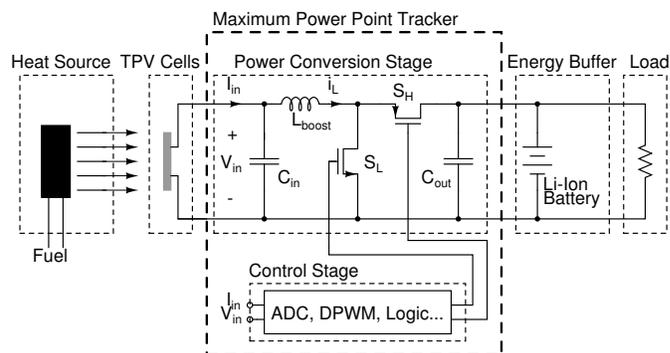


Fig. 3. Schematic drawing of the system architecture. The integrated maximum power point tracker consists of a boost converter power stage and a control stage, all implemented in a 0.35  $\mu\text{m}$  CMOS process.

through the boost converter relationship  $V_{in} = V_{out} * (1 - D)$ , it is sufficient to perturb the duty cycle and observe the change in input power. The P&O technique is well-suited for digital implementation, which we have chosen for our 0.35  $\mu\text{m}$  CMOS design. The details of the control stage are presented in section IV

The power stage comprises a CMOS integrated boost converter with an off-chip inductor and capacitors. The control stage and gate drivers are all powered from the intermediate energy buffer on the output, which is a lithium-ion battery in Fig. 3, but can be any charge storage device with suitable energy density and voltage range. A detailed description of the power stage and its operation is presented in section V.

## IV. CONTROL

Here we introduce how the controls of our system are realized while achieving the goals of very low sensing and control loss and maximum extraction of available energy from the source.

### A. Lossless Current Sensing

While voltage sensing is typically relatively easy to implement, sensing of current in a power converter is often more challenging. The current sensing method used in this work is shown in Fig. 4. It provides lossless sensing of the current by utilizing the parasitic resistance of the power inductor ( $L_{boost}$  of Fig. 3). This method results in overall increased conversion efficiency, since no additional sense resistors are introduced into the circuit, which would add power loss to the system. The average voltage across the inductor,  $\langle v_L \rangle$ , is directly proportional to the average inductor current,  $I_L$ , since in steady-state,  $L \langle \frac{di_L}{dt} \rangle$  is zero by definition. The low-pass filtered differential voltage  $V_{high} - V_{low}$  can thus be used to measure the average input current. This sensing method is well suited to this application as we only need to know *relative* currents (and powers), not absolute values. Variations in inductor ESR are thus not problematic. Furthermore, the time constant of any temperature-induced variation of the ESR value is much larger than the chosen sampling time, so it does not negatively affect tracking performance.

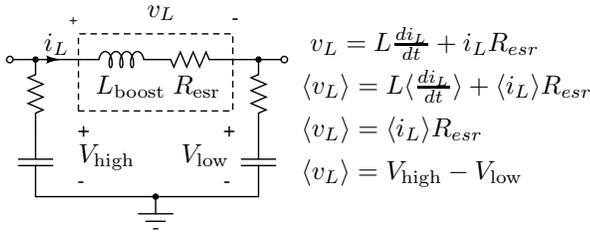


Fig. 4. Schematic drawing of the lossless current sensing implementation. The voltage drop across the inductor parasitic resistance  $R_{esr}$  is extracted through low-pass filtering.

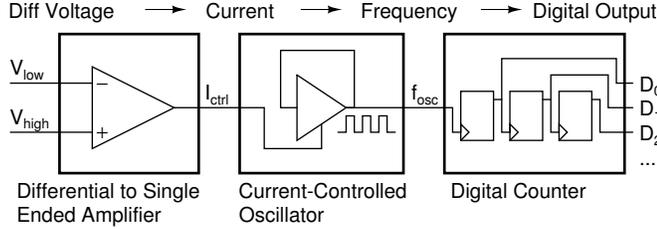


Fig. 5. Block diagram of the differential ADC architecture with inherent low-pass filtering and low power and area requirements.

### B. Analog to Digital Converter

We implemented the ADC architecture of Fig. 5 to convert the analog low-pass filtered differential voltage of Fig. 4 to a digital value. The architecture provides inherent low-pass filtering through the counting stage, which is beneficial since it reduces the analog filtering requirements of the signal. This directly translates to a reduction in silicon area by the integrated filter resistors and capacitors. Other key characteristics of the architecture of Fig. 5 are low power consumption and very small area. The active area occupied by the two ADCs (for current and voltage measurement) is  $0.083 \text{ mm}^2$ , and the power consumption for two ADCs at a sampling rate of 100 Hz (much faster than what is required for the application) is  $48 \mu\text{W}$ . Furthermore, the ADC architecture can be implemented as a single-ended ADC by connecting  $V_{low}$  to a fixed reference voltage. We use this strategy to measure the input voltage of the MPPT, with  $V_{low}$  tied to ground and  $V_{high}$  connected to the input voltage through a resistor divider.

Here we discuss the operation and design of the components of Fig. 5 in more detail:

#### 1) Differential voltage to single-ended current converter:

The conversion from differential voltage to single-ended current is performed by the circuit block shown in Fig. 6, which is a translinear amplifier adapted from [10]. The circuit operation can be analyzed by using the translinear principle [11], [12]:

$$V_{low} - V_{GS1} - V_{GS4} + V_R + V_{GS3} + V_{GS2} = V_{high} \quad (1)$$

Since the current through M2 and M4 is the same, their corresponding  $V_{GS}$  must also be the same. A similar argument holds for M1 and M3, resulting in:

$$V_{GS2} = V_{GS4}, \quad V_{GS1} = V_{GS3} \quad (2)$$

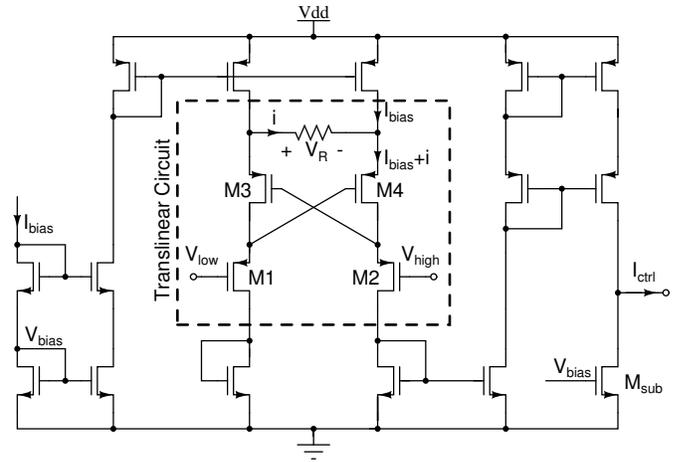


Fig. 6. Schematic diagram of differential voltage to single-ended current converter used as the first stage of the ADC architecture of Fig. 5.

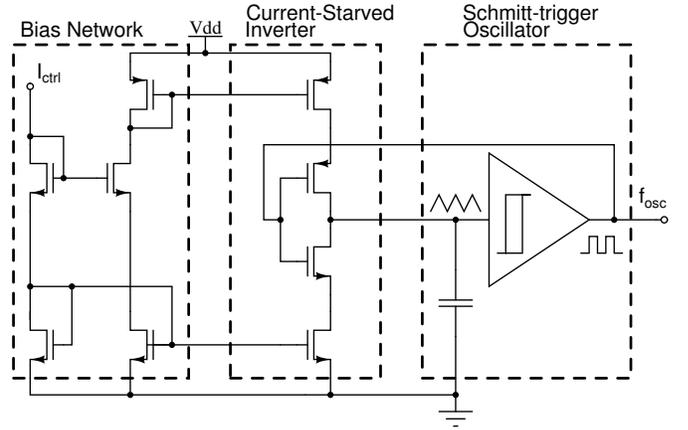


Fig. 7. Schematic diagram of current-controlled oscillator used in ADC architecture of Fig. 5

Using the results of Eq. 2 in Eq. 1 gives the result:

$$V_R = V_{high} - V_{low}$$

$$i = \frac{V_{high} - V_{low}}{R}$$

The current  $I_{bias} + i$  is mirrored to the output, and transistor  $M_{sub}$  is biased to subtract  $I_{bias}$ , leading to:

$$I_{ctrl} = i = \frac{V_{high} - V_{low}}{R}$$

2) *Current-controlled oscillator*: The output current of the converter of Fig. 6 is used to control the frequency of the current-controlled oscillator of Fig. 7. It comprises a bias network, current-starved inverter, an on-chip capacitor, and a Schmitt trigger to produce a square-wave output voltage whose frequency is dependent on the input current.

### C. Digital Logic

The MPPT algorithm was implemented in digital logic, and Fig. 8 shows a block diagram of the key components. The

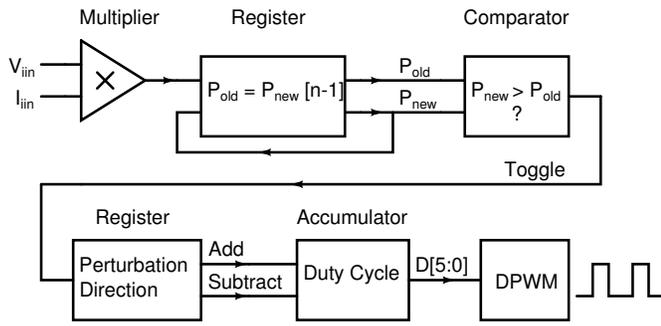


Fig. 8. Block diagram illustrating digital implementation of Perturb and Observe MPPT algorithm.

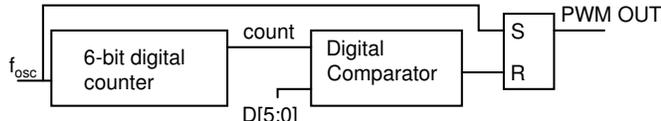


Fig. 9. Schematic drawing of counter-based digital pulse-width modulator implementation.

current and voltage measurements are provided as 9-bit values from the ADC, and the digital multiplier calculates the corresponding input power. This power is then compared to the last power sample, and if it is smaller, the perturbation direction is changed. Depending on the direction, the digitally-stored duty cycle command is either incremented or decremented in the accumulator, and the duty cycle command is translated to a time-domain waveform by the digital pulse-width modulator.

#### D. Digital Pulse Width Modulator

The digital pulse width modulator (DPWM) of Fig. 9 is used to convert the digital code held in the accumulator (of Fig 8) to a series of pulses of the correct width to drive the gates of the power MOSFETs. The design is a counter-based solution, which ensures monotonicity and achieves good linearity, while keeping the implementation area low. Because of the relatively low switching frequency and DPWM resolution (6-bit), the power consumption of the DPWM can be kept low. At a switching frequency of 1 MHz, the estimated (from simulation) power consumption of the DPWM is 0.45 mW.

### V. POWER STAGE

The power stage of the TPV tracking system is an integrated synchronous dc-dc boost converter. In the maximum power operating condition, it converts 0.8-1.3 V from the output of the TPV cell to 3.6-4.2 V for battery charging. A TSMC 0.35  $\mu\text{m}$  thick oxide device process is used to provide 5 V blocking voltage capability. Since the maximum power output of the TPV cells is approximately 300 mW (as seen in Fig. 2), the device sizes and gate driver taper factor are optimized for this power level, to balance the capacitive switching loss and conduction loss [13]. The IC power stage is designed to be flexible, enabling operation at switching frequencies to beyond 1.5 MHz, and with either hard-switching or high-ripple soft-switching operation [14], [15].

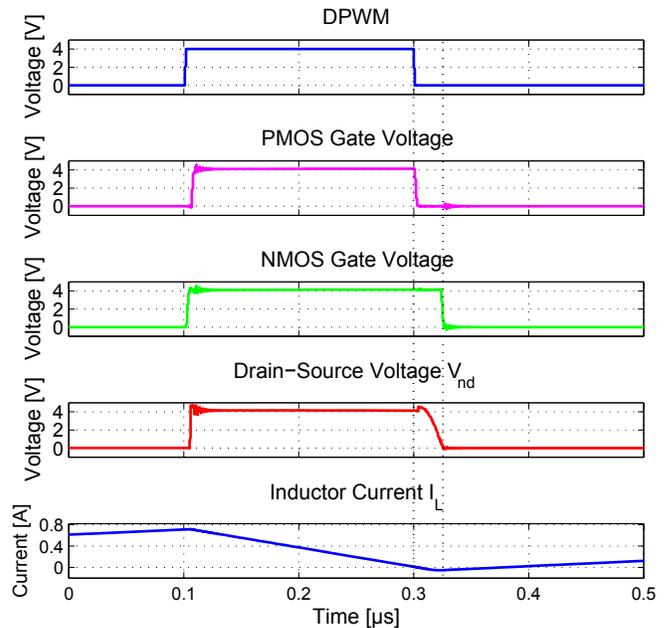


Fig. 10. Simulated waveforms to illustrate soft-switching operation.  $V_{in} = 0.9$  V,  $V_{out} = 4$  V and  $P_{out} = 300$  mW.

Since the converter will operate at the optimal power output condition of the TPV unit most of the time, the system only needs to operate efficiently over a relatively narrow power range. This opens up the possibility of using high-ripple zero-voltage-switching (ZVS) soft-switched operation. Fig. 10 shows sample soft-switching waveforms of this mode of operation.

If the inductor current  $i_L$  has peak-to-peak current ripple over 200% of the average current, soft-switching can be implemented [16]–[18]. After the high-side device is turned off and before the low-side device is turned on, the inductor current will discharge the drain-source capacitance of the low-side device and charge the capacitance of the high-side device. The converse can likewise be made to happen on the other transition. By adjusting the dead-times between the switching of the two devices carefully, ZVS can be achieved at the turn-on transition for both devices.

In this paper, self-adjusted digital dead-time control circuitry is introduced. This self-adjusted dead-time control circuit has several advantages, including simplicity, low power consumption, fast response to changes in operating condition, and the ability to extend the soft-switching operation range as compared to fixed dead-time control. Fig. 11 shows a simplified schematic of the dead-time control circuit. The self-adjusted dead-time circuit controls the dead-time based on the voltage level at the drain of the low-side device,  $V_{nd}$ . The low-side device will only be turned on once voltage  $V_{nd}$  drops below the dead-time logic threshold. Likewise, the high-side device will only be turned on after voltage  $V_{nd}$  rises above the dead-time threshold level for the high-side device turn-on. A Schmitt trigger is used to set the upper and lower switching threshold voltages and also provide stability improvement.

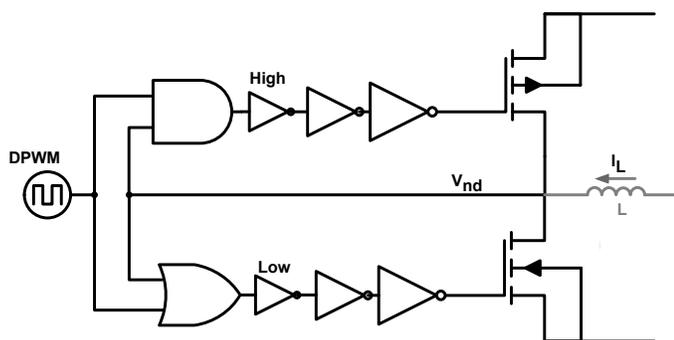


Fig. 11. Simplified schematic drawing of the self-adjusted dead-time control circuit used to achieve ZVS. Additional logic ensures switching even when soft switching is not realized.

TABLE I  
CONVERTER AREA BREAKDOWN

Component	Area [mm <sup>2</sup> ]
ADCs (2)	0.083
Analog Bypass Capacitors (oversized)	0.131
MPPT Logic	0.192
DPWM	0.031
Digital Decoupling Capacitors (oversized)	0.134
Power Devices	0.752
Gate Drives	0.061
Dead-time Control	0.040
Output Capacitor	1.21
Total Active Area	1.159
Total Capacitor Area (oversized)	1.475

To address operating conditions when ZVS switching will not occur, an additional 28 ns dead-time limit is set. This enables hard-switching operation to be employed if desired, and also ensures correct operation under conditions (such as transients) that disrupts soft-switching operation. (This window size is determined by the longest required dead-time for ZVS with minimum inductor current ripple.)

The power stage design is compatible with both soft and hard switching operation. The final optimized size (device width) for the NMOS transistors is 118000  $\mu\text{m}$ , and for the PMOS transistor is 121000  $\mu\text{m}$ . A taper factor of 11 is chosen for the gate drivers to balance the gate drive loss and switching loss of the power devices. The dead-time control logic and gate drivers are powered by the output of the converter.

## VI. EXPERIMENTAL RESULTS

The TPV tracking system was fabricated in a TSMC 0.35  $\mu\text{m}$  CMOS process and mounted in a QFN40 package. An annotated die photo of the converter is shown in Fig. 12, and approximate silicon area breakdown is presented in Table I. The converter specifications are shown in Table II.

### A. Power Stage Characterization

Shown in Fig. 13 are experimental waveforms of the converter which illustrate soft-switching operation using a 0.9  $\mu\text{H}$

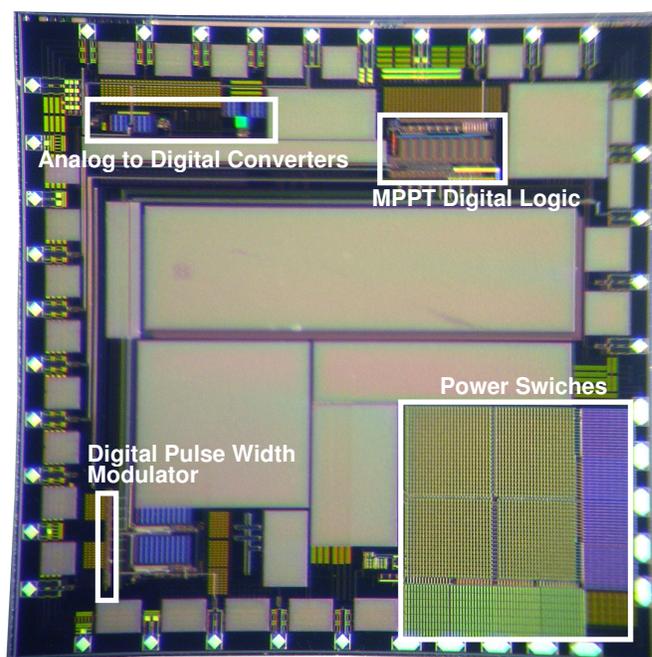


Fig. 12. Annotated die photo of the maximum power point tracker implemented in a 0.35  $\mu\text{m}$  CMOS process. Total die area is 4x4 mm, with approximately 1.16 mm<sup>2</sup> of active area (see Table I for more details regarding area breakdown).

TABLE II  
CONVERTER SPECIFICATIONS

Input Voltage Range	0.8-1.3 V (1 V Nominal)
Output Voltage Range	3.6-4.2 V (4 V Nominal)
Nominal Output Power	300 mW
Switching Frequency	500 kHz
Converter Peak Efficiency	95.4%
Tracking Efficiency	>98%

inductor with 11-120-P material, and operating at an input voltage of 0.9 V, an output voltage of 4 V, and an output power of 300 mW. Hard-switching waveforms are also as would be expected. Measured converter efficiencies for various power and voltage levels are shown in Fig. 14 for one power-stage implementation under hard-switched conditions. It can be seen that the converter has a peak efficiency of 95.4% with  $V_{in} = 1.3$  V,  $V_{out} = 4$  V and output power of 300 mW.

With the low output power and requirements of small size and high efficiency in this work, inductor size and converter performance trade-offs become important, especially as inductor size dominates the overall size of the converter (for most design conditions). Fig. 15 shows the measured converter performance for different frequencies, inductor designs and operating modes with a nominal input voltage of 1 V, output voltage of 4 V and output power of 300 mW. A picture of some of the inductors used in the experimental measurements is shown in Fig. 16. For reference, the TPV converter chip and a US penny are also shown in the picture, as well as a

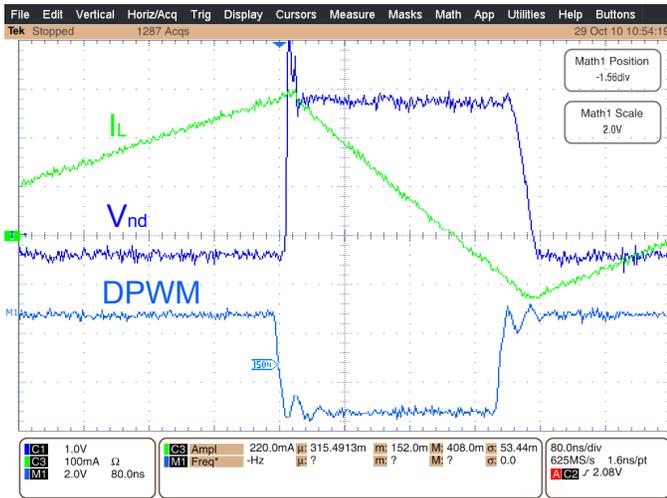


Fig. 13. Experimental waveforms of the power stage drain voltage and inductor current, as well as the DPWM signal. The dead-time control circuitry adjusts the timing of the gate signals to achieve ZVS. In this example, the input voltage is 0.9 V, the output voltage is 4 V, the inductor value is 0.9  $\mu\text{H}$ , and the output power is 300 mW.

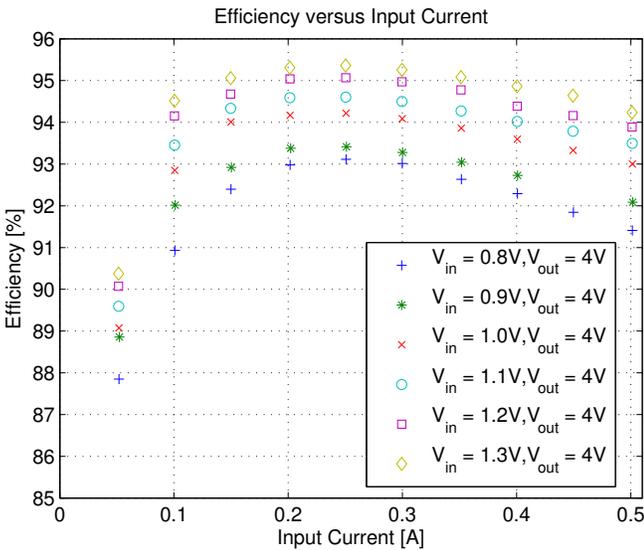


Fig. 14. Plot of measured power stage efficiency in hard-switching operation at  $f_{sw} = 500$  kHz. Input capacitance is 4  $\mu\text{F}$ , output capacitance is 4.8  $\mu\text{F}$ , and the power inductor is 8  $\mu\text{H}$  wound on a P9/5 3F3 core with  $3 \times 28$  AWG.

cm-scaled ruler.

As part of evaluating our system, we undertook a detailed study of achievable efficiency as a function of inductor size, switching frequency and operating mode (hard switching vs. soft switching). This included modeling of system losses for numerous designs (using loss models of commercial inductors along with detailed models of our own converter IC) and experimental validation of a subset of designs. We considered operation at frequencies from 500 kHz to 1.5 MHz, with inductance values selected for both soft- and hard-switching operation.

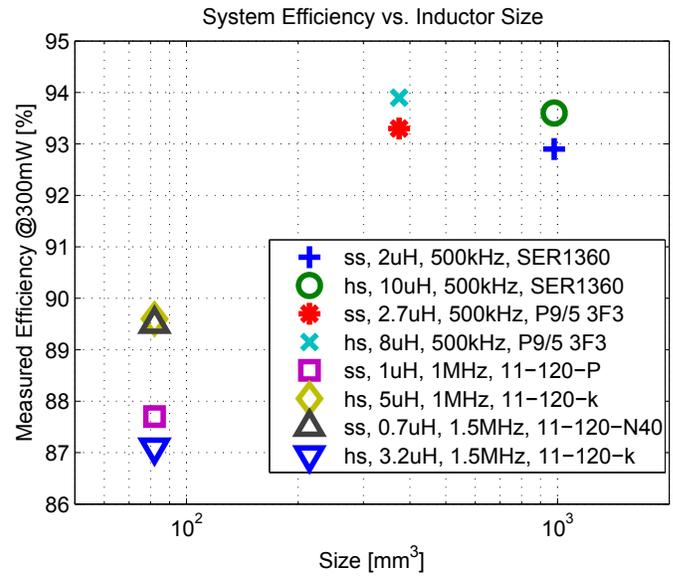


Fig. 15. Measured converter efficiency for various inductor sizes and values. Inductors are wound on selected available cores. “hs” stands for hard-switching and “ss” stands for soft-switching. Operation is for  $V_{in} = 1$  V,  $V_{out} = 4$  V, and  $P_{out} = 300$  mW.

At higher operating frequencies, designs can effectively use either high-permeability core materials or low-permeability core materials. An advantage of some low-permeability materials (e.g., NiZn ferrites) is that the effect of core loss can be reduced to an extent, benefiting the use of high-ripple soft switching. As illustrated in Fig. 15, at the lowest inductor volumes tested ( $\approx 80$   $\text{mm}^3$ ), the achieved experimental efficiencies with soft switching and hard switching were very close. (The soft-switched design operated at 1.5 MHz, while the hard switching design of comparable efficiency operated at a reduced frequency of 1 MHz; considering only 1.5 MHz operation, soft switching was superior by more than 2% in efficiency.) However, our models suggest that with an appropriate customized low permeability core material (relative permeability of 20-30), a soft-switched implementation could perform significantly better than a hard-switched implementation at frequencies above 1 MHz. (Our experimental results were limited to available commercial cores, and did not include an appropriate custom core material.)

Figure 17 shows calculated converter efficiency as a function of inductor size for a wide variety of commercial cores and inductance values, for both hard and soft switching. Figure 18 overlays these calculated results with the experimental results from Fig. 15. It can be seen that the measured experimental results all fall in to the range expected from model calculations. Consequently, Figs. 15, 17, and 18 show the frontier of inductor size vs. conversion efficiency, at least for the types of core materials and inductor designs evaluated.

### B. Tracking Performance

To evaluate the performance of the peak power tracker under repeatable conditions, the converter was attached to

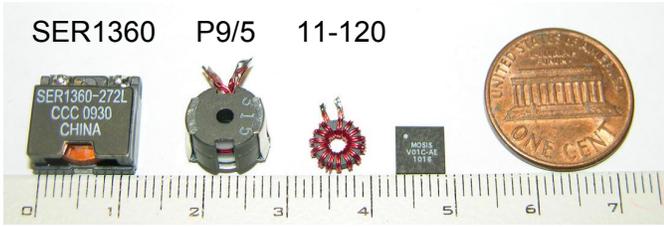


Fig. 16. Picture of some inductors used for the experiment. The packaged TPV converter chip and a US penny are shown for size reference, together with a cm-scale ruler.

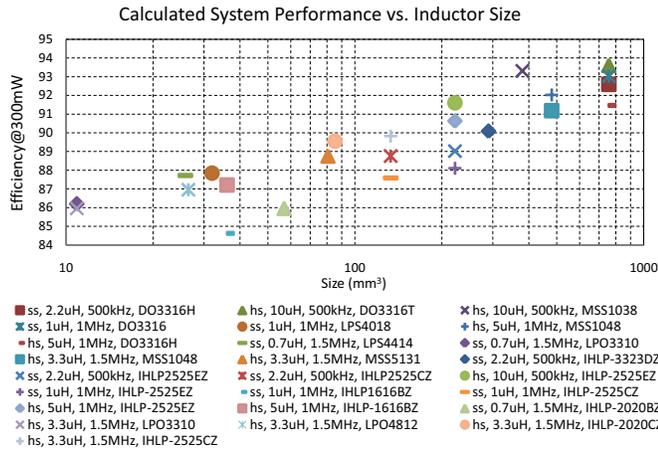


Fig. 17. Calculated converter efficiency versus inductor sizes. All inductors are commercially available from Coilcraft and Vishay. “hs” stands for hard-switching and “ss” stands for soft-switching.

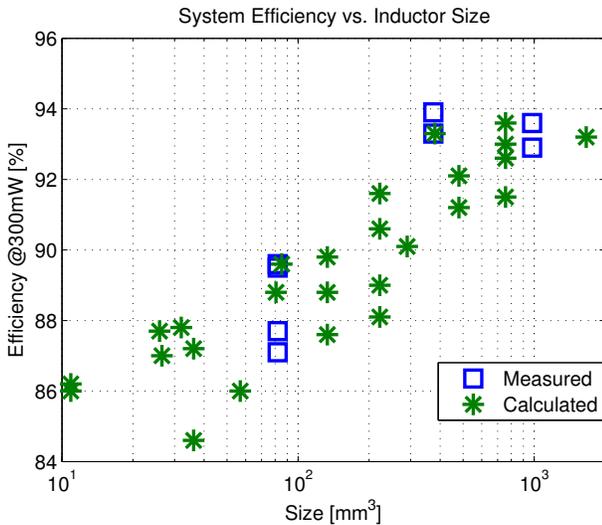


Fig. 18. Measured and calculated converter efficiency versus inductor sizes. The measured results agree well with calculated values. Operation is for  $V_{in} = 1$  V,  $V_{out} = 4$  V, and  $P_{out} = 300$  mW.

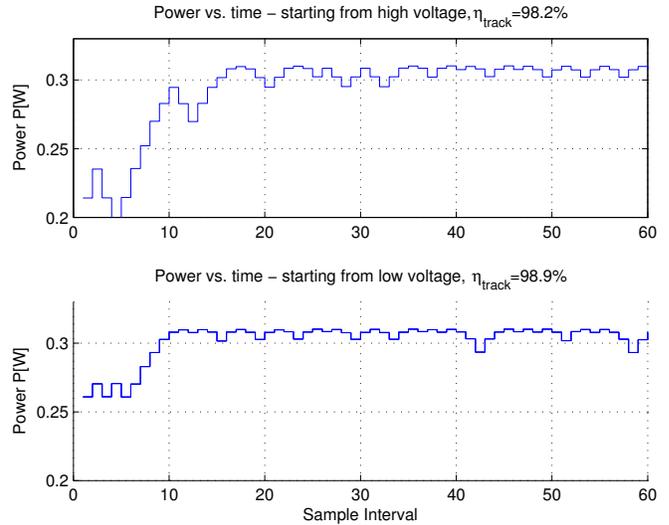


Fig. 19. Time-domain plot of the converter input power, showing maximum power point tracking.

two crystalline Silicon series-connected solar cells illuminated by a halogen lamp to produce I-V characteristics similar to that produced by the micro-burner. This enabled initial characterization of the converter without the added complexity of the micro-reactor dynamics.

Shown in Fig. 19 are plots of power versus time, illustrating the peak power tracker performance. In the top plot, the tracker is started with a duty cycle set to operate at a voltage that is higher than  $V_{mpp}$ . The bottom plot shows the corresponding data when the starting voltage is set below  $V_{mpp}$ . In both cases, the converter correctly finds the maximum power point and tracks it to within the resolution of the duty cycle command and the noise in the power measurement. The tracking efficiency,  $\eta_{track}$ , is a measure of how precisely the MPP is tracked, and is given by:  $\eta_{track} = \frac{\langle P_{in} \rangle}{P_{MPP}}$ , and is above 98% in both cases in Fig. 19.

Fig. 20 shows a plot of converter input power versus input voltage, which illustrates the I-V characteristics of the source, which is similar to the plot shown in Fig. 2. In addition, the discretization of the input voltage illustrates the finite achievable voltage step-size. The minimum step-size is limited by the resolution of the digital pulse-width modulator.

## VII. CONCLUSION

A fully integrated maximum power point tracking system developed in  $0.35 \mu\text{m}$  CMOS is presented. A low power custom-designed ADC suitable for lossless current sensing is utilized to achieve very low control losses, together with a digital implementation of a peak power tracking algorithm. The integrated boost power stage can be configured to employ either soft-switching techniques to achieve high efficiency operation while operating at high switching frequencies, or hard-switching operation for efficient operation at lower switching frequencies. Achievable efficiency versus passive component

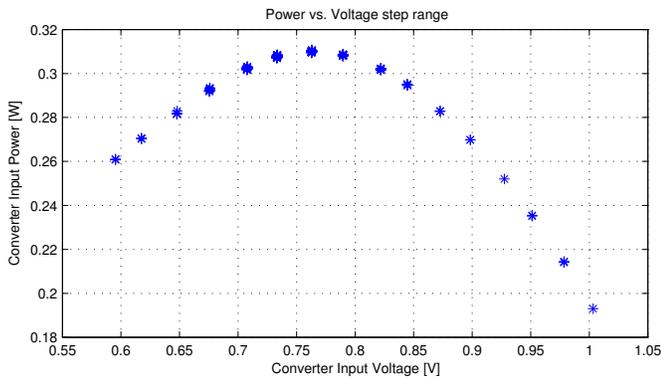


Fig. 20. Plot showing the power and voltage dependence of the experimental power source, using the same data as that which generated Fig. 19. The voltage step-size is limited by the resolution of the digital pulse-width modulator.

size is explored; power stage efficiencies above 95% are demonstrated, and MPP tracking efficiency of above 98% is demonstrated.

#### ACKNOWLEDGMENTS

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