

# Design of Variable-Resistance Class E Inverters for Load Modulation

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**Abstract**—Single-switch inverters such as the conventional class E inverter are often highly load sensitive, and maintain zero-voltage switching over only a narrow range of load resistances. This paper introduces a design methodology that enables rapid synthesis of class E inverters that maintain ZVS operation over a wide range of resistive loads. We also show how the proposed methodology relates to circuit transformations on traditional class E designs. The proposed methodology is demonstrated and experimentally validated on a design at 27.12 MHz that operates efficiently over an 8:1 load resistance range.

## I. INTRODUCTION

For frequencies above about 10 MHz, single-switch inverters such as the Class E inverter are often preferred. Figure 1 shows the topology of the conventional Class E inverter, with the addition of a parallel-tuned output filter network  $L_P-C_P$  to improve output waveform quality. In the traditional Class E inverter [1, 2, 3], the input inductor  $L_F$  acts as a choke, while the tuned load network ( $C_F, L_S, C_S, R$ ) is selected to both deliver power to the load resistor  $R$  and shape the switch voltage  $v_{DS}$  to provide zero-voltage switching (ZVS) and zero  $dv/dt$  turn on of the switch. Operation in this way – under ZVS with a single ground-referenced switch – facilitates switching at very high frequencies.

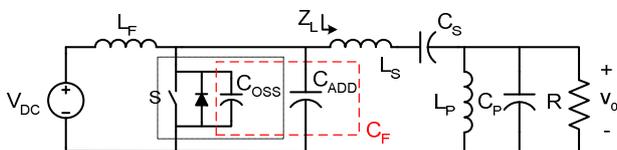


Fig. 1. Class E inverter topology, including parallel-tuned output filter. The capacitor  $C_F$  comprises the device output capacitance  $C_{oss}$  and additional capacitance  $C_{ADD}$ . It is also assumed that the switch has an antiparallel diode.

Because the load network is used to shape the switch voltage trajectory, the traditional Class E inverter is highly sensitive to variations in load resistance [2, 4], and tends to deviate substantially from zero-voltage switching for load variations of more than about a factor of two or three in resistance. In many applications – such as when the load resistance is well known, or the inverter is coupled to the load via an isolator – this load sensitivity is not problematic. In other applications,

however, it would be desirable to be able to operate efficiently over a wide range of resistive loads.

One application in which the effective load resistance can vary significantly is in dc-dc converters. In this case, the equivalent resistance provided by the rectifier can vary significantly with output voltage, instantaneous power, and input voltage [4-6]. While load variations in these applications can be compensated for with techniques such as resistance compression networks [4], these techniques increase component count and loss.

Another application in which the effective load resistance seen by the inverter varies over a wide range is in *outphasing* inverter systems. In outphasing, output power is controlled by phase-shifting the switching times of multiple inverters (i.e., phase-shift control of two or more inverters). When designed with an appropriate lossless power combiner – such as a Chireix combiner or multi-way lossless combiner – the real component of the effective load impedance seen by each inverter varies with control angle (thus controlling power), while the reactive component remains small [7-18]. For this reason, systems controlled in this manner are said to use *load modulation* to vary their output power. These systems must typically operate over a load resistance ratio that is equal or greater than the desired output power ratio obtained through load modulation.

While Class E and related inverters have been employed in applications with variable effective load resistance (e.g., [15, 16, 19]), a simple and effective methodology for designing inverters for such conditions is lacking. There has been some theoretical work on design of Class E inverters that are insensitive to load variations (e.g., [20-22]). However, the results are complex, making design insight difficult, and tend to lead to designs that have very high circulating currents, which hurts efficiency. (With sufficiently high circulating currents, operation can be made insensitive to the load resistance, but the achievable practical efficiency of such designs is relatively poor.)

In this paper, we present a methodology for rapidly synthesizing single-switch resonant inverters for operation at fixed frequency with variable load resistance (i.e., with load modulation). To provide greater flexibility of operation, we allow for waveforms that ideally maintain ZVS switching and constant switch duty ratio, but do not necessarily maintain zero  $dv/dt$  turn-on of the transistor as load resistance varies. We focus on identifying the resonant frequencies and

characteristic impedances of the key resonant networks in the circuit, and provide guidance of how circuit performance is modified by adjusting these parameters. In section II of the paper, we introduce the design methodology as applied the Class E inverter of Fig. 1. The methodology is demonstrated in Section III and experimentally validated in Section IV. Section V shows how this design methodology relates to circuit transformations on classical Class E designs [1-3], and Section VI concludes the paper.

## II. DESIGN METHODOLOGY

To design the inverter for load modulation, one starts with a set of output specifications: output frequency  $f_j$ , rated output power  $P_{or}$ , and a load resistance range (from minimum rated load resistance  $R_{min}$  to a maximum load resistance  $R_{max}$ ). Output power  $P_o$ , load resistance  $R$ , and dc input voltage  $V_{DC}$  are approximately related as follows:

$$\frac{P_o R}{V_{dc}^2} = 1.32 \quad (1)$$

The rms output voltage amplitude,  $V_{o,rms}$ , is approximately 1.15 times the dc input voltage, and is approximately invariant to load resistance, so  $R_{min}$  sets the rated output power and  $R_{max}$  sets the minimum output power.

For the design procedure, it is assumed that transistors of appropriate characteristics (on-state resistance, voltage and current ratings, and capacitances) can be obtained. The design goals are to select input network component parameters  $L_F$  and  $C_F$ , and output network component parameters ( $L_S$ ,  $C_S$ ,  $L_P$  and  $C_P$ ). It is assumed that the total capacitance  $C_F$  includes transistor output capacitance  $C_{oss}$ . Moreover, we assume that the all components are linear (neglecting variations of  $C_{oss}$  with voltage on circuit operation, as treated in [23-26].) It is also assumed that the transistor is operated at 50% duty ratio.

*A key observation we have made is that to achieve good performance under load modulation, the load network impedance  $Z_L$  should remain substantially resistive as load resistance  $R$  varies.* Consequently, we tune both the  $L_S$ ,  $C_S$  network and the  $L_P$ ,  $C_P$  network to be resonant at the switching frequency:

$$\frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_S C_S}} = 2\pi f_j \quad (2)$$

Note that this design selection is significantly different than those proposed previously for operation under varying load [19-21].

The characteristic impedances of the  $L_S$ ,  $C_S$  and  $L_P$ ,  $C_P$  networks of are selected such that adequate filtering of the output voltage is achieved across the intended load modulation range. While this selection is highly application dependent, one possible selection method is to choose the parallel network to provide high filtering for the lightest load (largest resistance), and the series network to provide high filtering at the heaviest load (smallest / rated resistance), and to rely on a combination of series and parallel filtering in the mid range (e.g., near the geometric mean of minimum and maximum resistances). Thus, one might choose:

$$\frac{\sqrt{L_S/C_S}}{R_{min}} = \frac{R_{max}}{\sqrt{L_P/C_P}} = Q_{fil} \quad (3)$$

where  $Q_{fil} \sim 5$  might be selected for adequate filtering over a 12:1 load resistance range.

It should be noted that other filter structures may be selected, but should be chosen with the goal that the input impedance of the load network ( $Z_L$  in Fig. 1) remain resistive at the switching frequency as the load resistance changes. Likewise, to provide impedance transformation between the inverter and the load, one should utilize a method that maintains resistive input impedance of the load at  $f_j$  as the load varies, such as a tuned transformer, an immittance conversion network, or a quarter-wave line.

To achieve the desired soft-switching performance across load, the input-side network  $L_F$ ,  $C_F$  is tuned at or just slightly below 1.5 times the switching frequency. In practice, one starts by tuning this input network at 1.5 times the switching frequency:

$$1/\sqrt{L_F C_F} = 3\pi f_j \quad (4)$$

If needed to realize good switching conditions across the load range, the resonant frequency can be reduced, typically by increasing capacitance  $C_F$  slightly (e.g., between 0 and 20%).

The characteristic impedance of the  $L_F$ ,  $C_F$  network is selected based on the rated (minimum) load resistance:

$$\sqrt{L_F/C_F} = k_f R_{min} \quad (5)$$

where  $k_f$  is a design value typically selected between 0.5 and 1.5. To the extent that soft switching can be maintained, higher values of  $k_f$  are preferable because they increase characteristic impedance and reduce the resonating losses associated with the  $L_F$ ,  $C_F$  network, which do not reduce significantly as load resistance increases (and operating power reduces). However, lower values of  $k_f$  yield higher values of  $C_F$ , and hence higher allowable values of transistor output capacitance, which forms part or all of  $C_F$ . Lower values of  $k_f$  also reduce  $L_F$ , enabling faster dynamic response of the inverter to changes in operating condition. In practice, one starts with a low value of  $k_f$ , and increases it as much as possible within the constraints of maintaining ZVS (or close to it) across the load range, providing at least the minimum amount of capacitance associated with the transistor, and achieving the needed response speed.

We have found that the above methodology, used in conjunction with a circuit simulator such as SPICE, allows rapid design of inverters that operate well over a wide range of load resistances.

## III. EXAMPLE AND DEMONSTRATION

This section illustrates how the proposed design methodology can be applied, and presents simulation results that demonstrate its efficacy. (Experimental results are presented in the following section.) The design procedure begins with a rated load resistance, rated output power and switching frequency. Table I summarizes parameters chosen for the example we carry out here.

Based on these values, we can calculate the rms value of output voltage  $V_{or}$ , rated output rms current  $I_{or}$ , and DC supply voltage  $V_{DC}$ :

rms output voltage:

TABLE I. DESIGN PROCEDURE EXAMPLE INPUT DATA.

Parameter	Value
Rated load resistance $R_{or}=R_{min}$	12.5 $\Omega$
Rated output power $P_{or}$	25 W
Switching frequency $f_1$	27.12 MHz

$$V_{or}=\sqrt{P_{or}R_{or}}=\sqrt{25W \cdot 12.5 \Omega}=17.68 V \quad (6)$$

Rated rms output current:

$$I_{or}=\frac{P_{or}}{R_{or}}=1.41 A \quad (7)$$

dc input voltage:

$$V_{DCr}=\frac{V_{or}}{1.15}=15.37 V \quad (8)$$

The next step is to choose the parameters  $L_S$  and  $C_S$ . As per (2), these are chosen to resonate at the switching frequency. In addition, we select a Q factor of the circuit at rated load as per (3). Here we select  $Q_{fil} = Q_s = 5$ :

$$\frac{\sqrt{L_S/C_S}}{R_{min}}=5 \quad (9)$$

This leads to the following results:

$$C_s=\frac{1}{2\pi f_1 Q_s R_{or}}=93.9 pF \quad (10)$$

$$L_s=Q_s^2 R_{or}^2 C_s=367 nH. \quad (11)$$

A similar approach is applied to design the parallel resonant output filter. In this example, its quality factor is chosen to  $Q_{fil} = Q_p = 4.5$  when the load resistance is ten times higher than the rated resistance (the highest considered resistance):

$$\frac{R_{max}}{\sqrt{L_p/C_p}}=\frac{10 \cdot R_{or}}{\sqrt{L_p/C_p}}=4.5 \quad (12)$$

This leads to results:

$$L_p=\frac{10R_{or}}{2\pi f_1 Q_p}=147 nH, \quad (13)$$

$$C_p=\frac{Q_p^2 L_p}{R_{or}^2}=293 pF. \quad (14)$$

Calculations of the  $L_F-C_F$  resonant circuit parameters begins with the determination of the resonant frequency  $f_f$  as dictated by (3):

$$f_f=1.5 \cdot f_1=40.68 MHz. \quad (15)$$

Next, we determine the characteristic impedance  $Z_{charF}$  of the input network  $L_F-C_F$ . SPICE simulations of the circuit model indicate that in order to maintain soft switching, the factor  $k_f$  in (5) should be set to approximately 0.7:

$$Z_{charf}=0.7 \cdot R_{or}=8.75 \Omega \quad (16)$$

$L_F-C_F$  are determined from circuit resonant frequency and characteristic impedance as follows:

$$C_F=\frac{1}{2\pi f_f Z_{charf}}=447 pF, \quad (17)$$

$$L_F=C_F \cdot Z_{charf}^2=34.2 nH. \quad (18)$$

For the given parameters, the EPC 1007 transistor has been chosen. Its internal capacitance is simply approximated as a linear capacitance  $C_{oss} = 100 pF$ . To provide the desired operation, we augment  $C_{oss}$  with an additional capacitance  $C_{ADD}$ :

$$C_{ADD}=C_F-C_{oss}=337 pF \quad (19)$$

Calculated parameters may have to be slightly adjusted using simulation. The nominal circuit parameters for the design (including both from the initial design pass and with adjustments based on simulation) are shown in Table II.

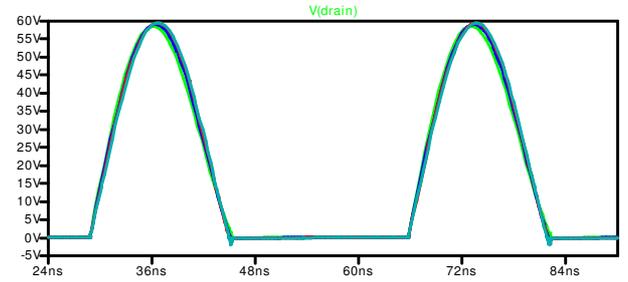


Fig. 2.  $v_{DS}$  waveforms of the proposed Class E inverter of Table III (for 1, 2, 5 and 10 times rated resistance of 12.5  $\Omega$ ).

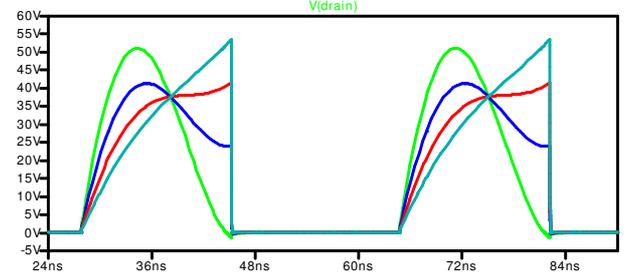


Fig. 3.  $v_{DS}$  waveforms of the classical Class E inverter (Q=10 Design, [3], components in Table III) (for 1, 2, 5 and 10 times rated resistance).

Fig. 2 shows simulated drain-source voltage waveforms for an inverter based on our proposed design methodology, while Fig. 3 shows results from a conventional class-E design (a design at  $Q=10$  [3]). The simulations utilize a simple switch model with an on-resistance  $R_{ds} = 0.3$  and a linear output capacitance  $C_{oss} = 100 pF$  for the switch. Components used in the proposed design are presented in Table II, while components for the conventional design are presented in Table III.

It can be seen that a class-E inverter based on the methodology proposed here achieves much better switching waveforms across load resistance (i.e., at or near ZVS) than a traditional class E design.

#### IV. EXPERIMENTAL RESULTS

To further validate the proposed approach, an experimental prototype has been developed and evaluated. Fig. 4 shows the prototype, which approximately realizes the example design of the last

section (components listed in Table IV.) In addition to using paralleled off-the-shelf inductors to construct  $L_F$ , a version of the converter with a custom single-turn foil inductor having a higher  $Q$  was also tested. The gate driver comprised a parallel connection of six inverters (three NC7WZ04 integrated circuits). The inverters were controlled by a function generator. The gate driver circuit supply power never exceeded 100 mW. The inverter was constructed on a four layer PCB with 2 oz outer and 1 oz inner copper layers. The load for the inverter comprised paralleled resistors soldered directly to the PCB. The load resistors were cooled through the PCB by mounting the back of that portion of the PCB to a Dynatron P199 CPU cooler.

TABLE. II. COMPONENT AND PARAMETER VALUES FOR DESIGNED CLASS E INVERTER.

Component	Values from design procedure	Adjusted values after SPICE simulation
$L_F$	34.2 nH	34.2 nH
$C_F$	447 pF	516 pF
$C_{ADD}$	347 pF	366 pF
$L_S$	367 nH	367 nH
$C_S$	93.9 pF	93.9 pF
$L_P$	147 nH	147 nH
$C_P$	293 pF	293 pF
$v_{DC}$	15.37 V	16 V
$f_l$	27.12 MHz	27.12 MHz
$D$	50%	50%

TABLE. III. COMPONENT VALUES FOR CLASSICAL CLASS E INVERTER.

Component	Values from Spice simulation
$L_F$	100 $\mu$ H
$C_F$	199 pF
$C_{ADD}$	99 pF
$L_S$	734 nH
$C_S$	47 pF
$L_P$	-
$C_P$	-
$v_{DC}$	16 V
$f_l$	27.12 MHz
$D$	50%
$R_{or}=R_{min}$	12.5 $\Omega$

Fig. 5 shows the experimental test setup. The prototype class E circuit validates the proposed design approach. Input power measurements were based on dc input current and voltage measurements using multimeters. Output power was measured by means of oscilloscope-based rms voltage and dc resistance (and thus includes the modest harmonic contributions to output power). Efficiency results across load are shown in Fig. 6. Experimental waveforms at rated load resistance, 2X rated resistance and 12X rated load resistance are shown in Figs. 7, 8 and 9, respectively.

TABLE. IV. COMPONENT VALUES FOR THE PROTOTYPE CLASS E INVERTER.

Component	Value	Implementation
$L_F$	35.6 nH	3 parallel maxi-spring 132-09 inductors
$C_{ADD}$	377 pF	ATC 700A
$L_S$	380 nH	maxi-spring 132-17
$C_S$	90 pF	ATC 700A
$L_P$	169 nH	maxi-spring 132-12
$C_P$	203 pF	ATC 700A
$R_{or}$	12.5 $\Omega$	4 parallel Bourns CHF1206CNT500LW resistors
$R_{max}$	150 $\Omega$	Series connection of Bourns CHF2010CNP101RX and CHF1206CNT500LW resistors
Switch	$C_{oss} \sim 100$ pF $R_{on} \sim 0.03$ $\Omega$	EPC 1007
$v_{DC}$	16 V	-
$f_l$	27.12 MHz	-
$D$	50%	-

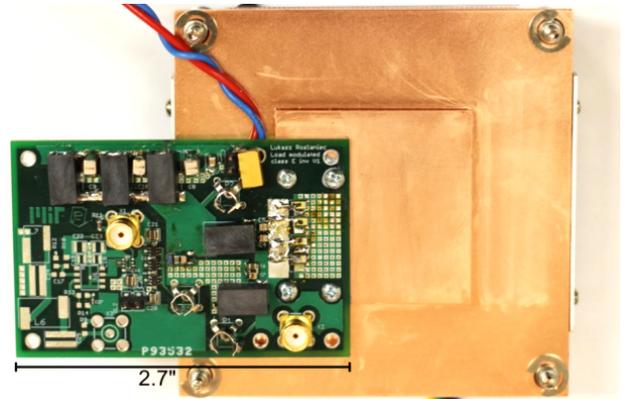


Fig. 4. Photograph of the prototype inverter with resistive load and load heat sink. This version of the inverter utilizes coilcraft maxi-spring inductors to form  $L_F$ . The design was also tested with a large single-turn foil inductor that provided higher  $Q$ .

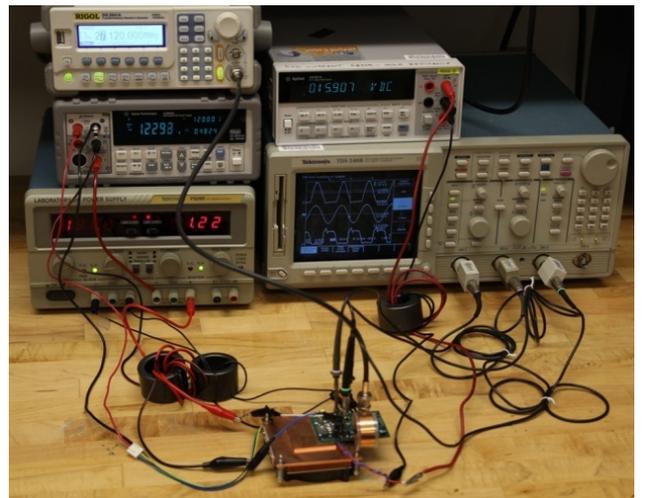


Fig. 5. Photograph of the experimental setup. This version of the circuit incorporates the custom foil inductor.

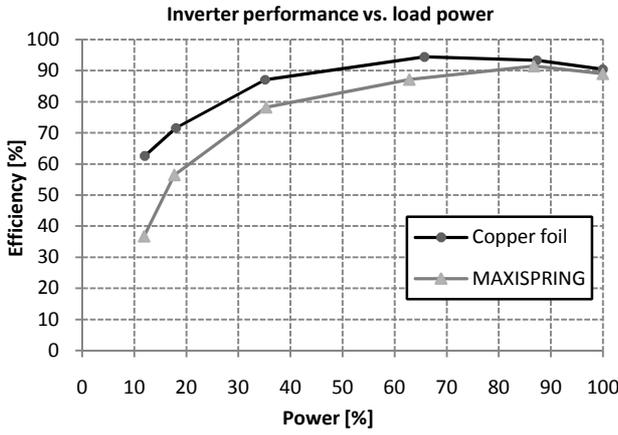


Fig. 6. Inverter drain efficiency as a function of output power (adjusted by resistive load modulation). The efficiency is found at the following load resistances:  $R = 12.53 \Omega$ ,  $16.47 \Omega$ ,  $24.61 \Omega$ ,  $49.3 \Omega$ ,  $99.3 \Omega$  and  $149.1 \Omega$ . Efficiency is shown for both the baseline design (with  $L_F$  formed from paralleled Maxi-spring inductors) and with a custom foil inductor for  $L_F$ .

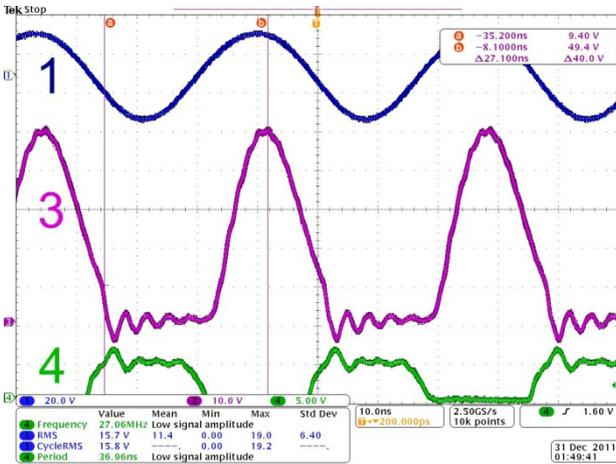


Fig. 7. Waveforms of the prototype class E inverter at rated load ( $R_o = 12.53 \Omega$ ) ( $1 - v_o$ ,  $3 - v_{ds}$ ,  $4 - v_g$ ).

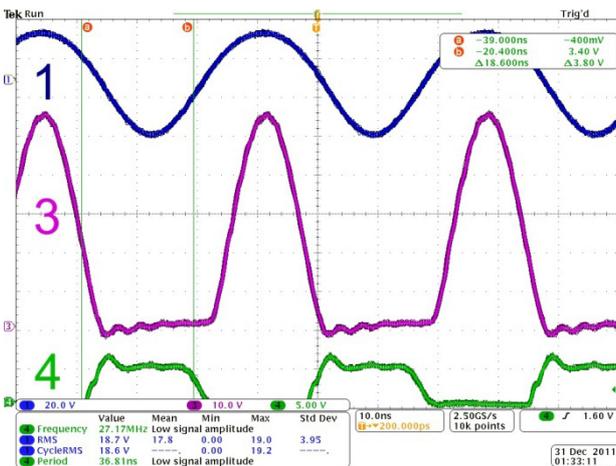


Fig. 8. Waveforms at 66% of rated load ( $R_o = 24.61 \Omega$ ) ( $1 - v_o$ ,  $3 - v_{ds}$ ,  $4 - v_g$ ).

It can be seen that near-zero-voltage switching is maintained over the 12:1 load resistance range. Unlike the simulation, however, the experimental inverter begins to lose soft switching at one end of the operating range. (It is believed this results partly from the nonlinearity of the device capacitance, which was not modeled in the

simulation.) A 12:1 variation in load resistance results in an 8.3:1 variation of output power. This indicates that the system provides an rms output voltage that is nearly (but not perfectly) invariant to the value of load resistance. Fig. 6 shows efficiency vs. output power, with power varied by adjusting the load resistance. It can be seen that efficiency remains high over a very wide power (and load resistance) range. At very low output power levels, losses due to circulating currents in the  $L_F$ - $C_F$  input network become increasingly important and degrade system efficiency.

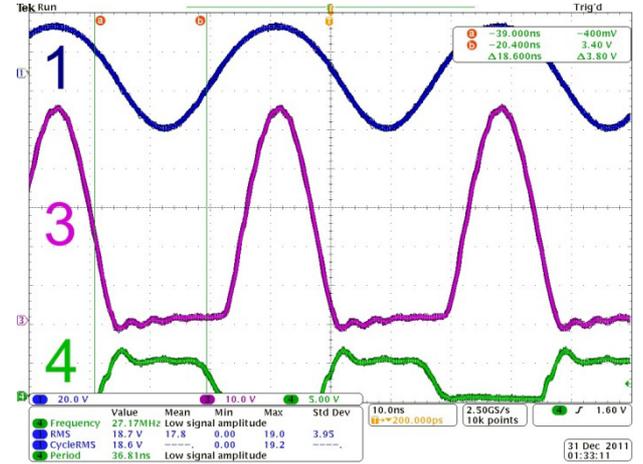


Fig. 9. Waveforms at 12% of rated load ( $R_o = 149.1 \Omega$ ) ( $1 - v_o$ ,  $3 - v_{ds}$ ,  $4 - v_g$ ).

## V. CIRCUIT TRANSFORMATION VIEW

In this section, we show how circuit transformations can be applied to existing inverter designs (such as the conventional class E inverters of [2,3]) to realize inverters having similar circuit values and properties to those developed with the methodology of Section II. The circuit transformation technique we introduce can be used to retune existing designs to better accommodate load resistance variation, and combined with other design techniques (e.g., [25]) to better account for factors such as device capacitance nonlinearity.

Consider the transformation steps in Fig. 10 (a)-(d). The circuit of Figure 10(a) can represent a conventional class E design, such as a design from [3] with a high loaded Q and a large-valued dc choke inductor  $L_{DC}$ . In such a design, the resonant network impedance  $Z_L$  is inductive at the switching frequency. Consequently, as shown in Fig 10(b), one can split the  $LC$  tank into two portions – a series resonant network  $L_T$ ,  $C_T$  tuned to the switching frequency and an additional inductor  $L_{NET}$ . If the output tank is of sufficiently high quality factor, it carries a nearly sinusoidal current at the switching frequency. In this case, as illustrated in Fig. 10(c), series-connected components  $L_{NET}$  and  $R$  can be replaced with a parallel network ( $L_K$  and  $R_K$ ) having the same impedance at the switching frequency. The values of the transformed components may be found as [28]:

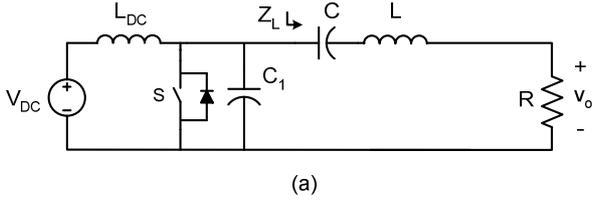
$$L_K = L_{NET} \cdot ((Q_T + 1) / Q_T) \quad (20)$$

and

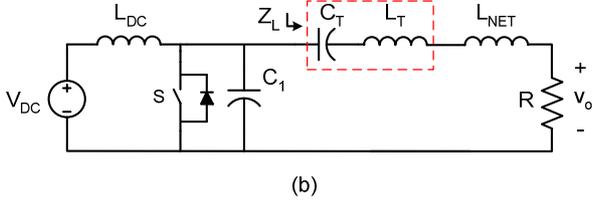
$$R_K = R \cdot (Q_T + 1) \quad (21)$$

where

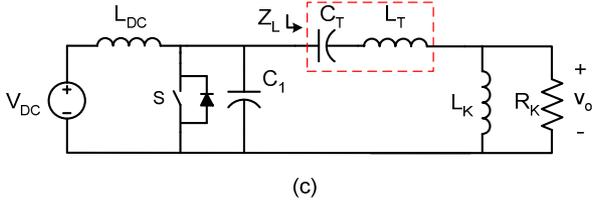
$$Q_T = \omega L_{NET}/R \quad (22)$$



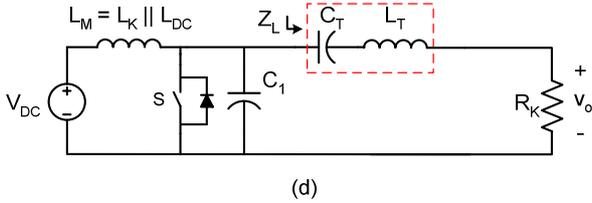
(a)



(b)



(c)



(d)

Fig. 10. Steps for transforming a class E inverter for variable-resistance operation.

Considering the network of Fig. 10(c), the tank network  $L_T C_T$  is a short circuit (due to resonance) at the switching frequency. At this frequency (only), inductor  $L_K$  is effectively in parallel with the input choke inductor  $L_{DC}$  (from an ac perspective). As our last transformation step, illustrated in Fig. 10(d), we thus eliminate  $L_K$ , and replace  $L_{DC}$  with a new inductor  $L_M$  having a value of  $L_K \parallel L_{DC}$ .

The result of the transformation illustrated in Fig. 10 yields a circuit in Fig. 10(d) that has the output network tuned on resonance at the switching frequency, which we have found to be a desirable characteristic to achieve good operation over a wide load resistance range. Moreover, the input inductor in the transformed circuit is a resonant inductor rather than a simple dc choke. The behavior of the circuit of Fig. 10(d) will not necessarily be the same as that of Fig. 10(a), since two of the transformation steps employed preserve impedance characteristics only at the switching frequency, but not at dc or harmonic frequencies. Nonetheless, this transformation yields designs that are quite close to those produced by the methodology of Section II, and which maintain desirable operation over a wide load resistance range.

As an example of this transformation approach, we start with a conventional class E inverter design from [3] with  $Q = 100$  and a 50% switch duty ratio. From [3], the components for the circuit of Fig. 10(b) are defined by:

$$\omega R C_1 = 0.1851; \quad (22)$$

$$\omega R C_T = 0.01006; \quad (23)$$

$$\omega L_T/R = 99.4036; \quad (24)$$

and

$$\omega L_{NET}/R = 1.1764 \quad (25)$$

Transforming to the circuit of Fig. 10(c), we get

$$R_K = 2.3839 \cdot R \quad (26)$$

and

$$\omega L_K = 2.027 \cdot \omega L_{NET} = 2.3846 \cdot R \quad (27)$$

Finally the circuit of Fig. 10(d) results in the same values for  $C_1$ ,  $C_T$ ,  $L_T$  and  $R_K$ , with

$$\omega L_M = 2.027 \cdot \omega L_{NET} = 2.3846 \cdot R. \quad (28)$$

Examining this design, we find that:

$$\frac{I}{\sqrt{L_M \cdot C_1}} = 1.5052 \cdot \omega \quad (29)$$

such that the input network is tuned almost exactly to 1.5 times the switching frequency, and the output network is tuned to the switching frequency, just as in the design methodology of Section II. With addition of a tuned parallel resonant tank in parallel with the load resistor for filtering (and with appropriate renaming of components) we obtain a design very close to that provided by the direct design method of Section II.

The transformation technique of Fig. 10 is thus useful for converting existing class E inverter designs into alternative designs that are suitable for load modulation. While we do not detail it here, we have also found this approach to be effective with Phi-2 inverter designs [28]. Moreover, this transformation provides an approximate way to relate conventional class E designs to those generated by the methodology developed in Section II.

## VI. CONCLUSION

This paper presents a methodology for rapidly synthesizing single-switch resonant inverters such as Class E inverters for operation at fixed frequency with variable load resistance (i.e., with load modulation). We present a design methodology yielding class E inverter designs that are effective across a wide load resistance range. We focus on identifying the resonant frequencies and characteristic impedances of the key resonant networks in the circuit, and provide guidance of how circuit performance is modified by adjusting these parameters. The efficacy of this approach is demonstrated in both simulation and in an experimental prototype inverter at 27.12 MHz. We also show how this design methodology relates to circuit transformations on classical class E designs, and demonstrate how the transformation-based approach can be employed to reconfigure designs with higher-order tunings for variable-resistance operation. It is expected that the presented work be valuable in applications where single-switch inverters are operated under variable-resistance-load operation, such as in dc-dc converters and outphasing power amplifiers.

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