There are at least four ways to control the amount of power that is delivered in this circuit. They are now introduced individually, followed by the stategy which results in the most efficient operation of the inverter.

1) Full-bridge phase shift: Taking the fundamental of v_{FB} as the phase reference for all waveforms of interest, the Fourier series coefficients of v_{FB} are given by (4), where $\delta = \frac{2\tau}{T}$. The phase of each component is therefore either 0 or π radians. Each leg of the full-bridge operates at 50% duty ratio. Changing phase shift of the full-bridge can be defined as changing the amount of time between the rise of the voltages of high sides of leading and lagging legs. This directly corresponds to changing τ, the overall 'width' of the positive and negative voltage pulses of v_{FB}, while also affecting θ (however, that relationship also depends on frequency). According to (4), changing phase shift changes the magnitude of each harmonic component of the voltage, which in turn changes the resonant current and the overall power transfer.

$$V_{FB,n} = \begin{cases} 0, & n = 0,2,4,\ldots \\ \frac{4V_{IN}}{n\pi} \sin\frac{n\delta\pi}{2}, & n = 1,3,5,\ldots \end{cases} \quad (4)$$

2) Cycloconverter phase modulation: According to (3c), for a given resonant current amplitude of the fundamental and output voltage, increasing the cycloconverter phase shift ϕ decreases the instantaneous output power. This also means that for a given output power, operating at larger phase angle ϕ means having larger peak (and *rms*) resonant current.

3) Switching frequency: The impedance presented by the series resonant LC network is a function of frequency. Starting just above resonance (as a minimal ZVS requirement), the magnitude of the impedance increases as the frequency increases, which in turns causes the resonant current magnitude to decrease. Thus, fixing everything else constant, the power transfer to the load decreases with increased frequency.

4) Burst mode (ON-OFF) control: One can control average power by bursting the entire converter on and off at a modulation frequency that is far below the switching frequency. While this technique is *not* presently utilized in the prototype, it is anticipated that it could be very useful for maintaining efficiency at light loads.

D. Control for high efficiency

Efficient control of the converter is realized as a combination of the above techniques [14]. Without further details, the sum of all loss estimates may be lumped into one equation, (5), referenced as 'the loss function'. The loss function has some direct dependence on the switching frequency and the resonant *rms* current value. The goal of an efficient control law is to minimize the loss function while satisfying the power delivery requirement given by equation (3) and the appropriate ZVS constraints (otherwise the loss function is invalid).

$$Loss = A\left(f_{SW}, i_x\right) f_{SW}^{\alpha} + B\left(f_{SW}, i_x\right) {i_x}^{\beta} \quad (5)$$

The maximum amount of power which the inverter can deliver (ignoring ZVS requirements) occurs when it is operated at $f_{SW} = f_{res}$, $\delta = 1$, and $\phi = 0$. Decreasing power delivery can be done by increasing f_{SW} or ϕ, or by decreasing δ. An operating point determines the minimum required resonant current and the corresponding minimum cycloconverter phase shift $\phi = \phi_{critical}$. Any extra cycloconverter phase shift will result in extra loss as a consequence of higher current. For the components chosen for the prototype, the loss function is more sensitive to current than it is to frequency for most of the operating region. The nominal control strategy which minimizes losses looks to operate at the lowest possible cycloconverter phase shift ϕ, as this results in the lowest *rms* current, while also switching at the lowest allowed frequency and consequently the narrowest pulse width τ on the full-bridge. The cycloconverter is thus not utilized as a control handle beyond modulating it to resemble a diode rectifier. Essentially the combination of frequency/phase shift is more favorable in terms of loss than cycloconverter modulation, with further preference going to lower frequency. The equivalent circuit model for the converter under this control scheme is shown on Fig. 3. It emphasizes that the most efficient way to control the cycloconverter is by operating it as close to a diode rectifier as possible, with the only deviation being due to the parasitic (output) capacitance of the cycloconverter MOSFETs.

A restriction of how low the frequency can be comes from the ZVS requirements: the resonant current has to completely charge or discharge C_{par} before v_{cc} can change between 0 and V_{out} or vice versa. This gives rise to the angle $\phi_{critical}$ as the angle (in the switching period) during which the required amount of charge is delivered to or from this capacitance. Note that C_{par} is placed across only one of the diodes but its value absorbs the capacitance across the other diode as the two are in effectively in parallel. The effective value of C_{par} is given by (6), considering the nonlinear characteristics of the device capacitances. This value was empirically found to have worked best in predicting the behavior of the MOSFETs. In general, this is a function of the output (line) voltage: $V_{ds} = V_{out}$. The value of $C_{oss}\left(V_{ds}\right)$ is obtained from the manufacturer datasheet.

Under this scheme, the switching frequency is high at low output powers while the resonant *rms* current is low. There exists a boundary in switching frequency and current level above which it becomes more efficient to operate with non-minimal current but in turn to switch at a lower frequency. This is achieved by increasing ϕ above $\phi_{critical}$ for a certain output requirement. Since extra resonant current results (i.e. the resonant current is determined by ZVS and not power delivery), this will be referenced as the 'sloshing boundary'. It may refer to the maximum allowed frequency at a nominal current level or vice versa, and is dependent on the component selection and the loss. Note that the analytical models may not be accurate enough to exactly predict which direction is best and experimental verification will often be needed. The discussion presented in the rest of this paper comes as a result of experimentally determining that most of the operating points of CEC interest occur in the minimal current mode of operation, with the current sloshing technique mostly relevant for the very low output powers, which have small CEC weighting coefficients. Additionally, the gain in efficiency due

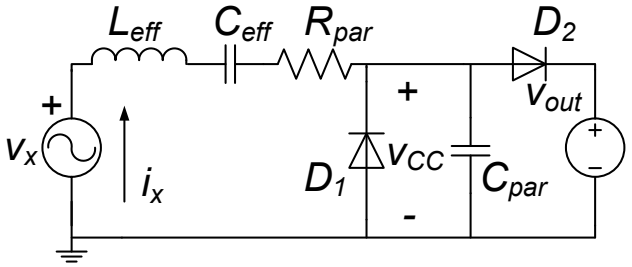

Fig. 3. Equivalent circuit model in the most efficient control mode for positive output polarity. The two connections to the diode rectifier are swapped for negative output polarity.

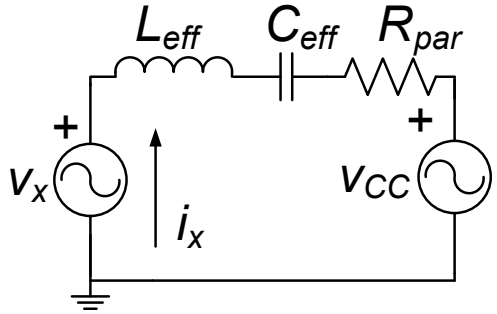

Fig. 4. Basic inverter model for control timing calculations.

to sloshing is typically very small for the chosen components, so the minimal current mode is often very close to the most efficient control law.

$$C_{par}\left(V_{ds}\right) = \frac{2}{V_{ds}} \int_0^{V_{ds}} C_{oss}\left(\nu\right) d\nu \tag{6}$$

E. Inverter analysis and timing calculations

Having presented the optimal control stategy, it is still a challenge to calculate the proper MOSFET timing, such that testing may be conducted. Apart from switching frequency, full-bridge phase shift, and cycloconverter phase shift (w.r.t. full-bridge timing), deadtimes need to be calculated for each half-bridge leg. Having a deadtime that is too small might lead to hard switching (and thus extra losses) and even failure due to voltage spikes. Having too much deadtime results in higher losses as the parasitic body diode conduction of each MOSFET is generally more lossy than conduction through the device. It is typically better to overestimate deadtime (rather than underestimate) as that is much less likely to result in failure of the components. It is also undesirable to operate at angles θ and ϕ that are much greater than minimal possible values as that results in higher *rms* current and thus greater loss. However, underestimating these leads to hard switching, which may compromise robust operation of the converter, and overestimation is also favored here.

A simplification of model of Fig. 3 replaces the cycloconverter with an AC voltage source equal to v_{cc}, as shown on Fig. 4. This model reflects all circuit elements to the secondary side of the transformer, and the voltage source v_x is thus equal to $N\times\ v_{FB}$. The model describes the time domain relations but it may also represent the converter at each switching harmonic if the two voltage sources and the resonant current are taken as phasor quantities (with $f_n = n \times f_{SW}$ for the n$^{\text{th}}$ switching harmonic). The parasitic resistance ('R_{par}') arises from modeling all loss in the converter as some equivalent resistor. One way to calculate control inputs under minimum current control law is by determining the minimum allowed cycloconverter phase shift given a switching frequency and the full-bridge pulse width[3]. These inputs fix the magnitude and phase of all harmonics of v_x, consistent with (4). To solve for resonant current i_x, and thus the output power, v_{cc} needs to be determined. However, v_{cc} depends on i_x. In setting up the equations to arrive at the solution, we assume that:

1) v_{cc} is a square waveform of values 0 and V_{out}, and of duty ratio 0.5.
2) v_{cc} has an instantaneous rising edge transitions, occurring when a charge of $Q_{par} = \frac{C_{par}V_{out}}{2}$ is delivered by i_x, after it crosses zero while rising. A similar calculation is used for the falling edge.
3) For a given V_{out}, C_{par} is a linear capacitance.

Furthermore, γ_0 is defined as the angle, along the switching cycle, at which i_x crosses zero while rising. Angle γ_Q is defined as the angle at which charge Q_{par} is delivered by i_x. Equation (7) shows the relationship between these angles and $\phi_{critical}$. Following the above assumptions, the Fourier series decomposition of v_{cc} is approximated by that of a square wave, as given by (8). This allow us to define a relationship between resonant current and the two voltage waveforms for the n$^{\text{th}}$ switching harmonic by writing the current-impedance equation for the standard series RLC circuit (excited by the difference of the two voltage sources), as given by (9a). Equation (9b) enforces that γ_0 is indeed a zero crossing angle of i_x and (9c) specifies that the right amount of charge is delivered in the time $\frac{\phi_{critical}}{\omega_{sw}}$. Solving (9) yields a consistent current and a set of angles, which can be used to set the final control input (cycloconverter phase shift) in order to achieve ZVS with minimal current sloshing for a given full-bridge phase shift and switching frequency.

$$\phi_{critical} = \gamma_Q - \gamma_0 \tag{7}$$

$$V_{cc,n} = \begin{cases} \frac{V_{out}}{2}, & n = 0 \\ 0, & n = 2,4\ldots \\ \frac{-2V_{out}}{n\pi}\left(\sin n\gamma_Q + j\cos n\gamma_Q\right), & n = 1,3,\ldots \end{cases} \tag{8}$$

$$I_{x,n} = \frac{N\frac{4V_{IN}}{n\pi}\sin\frac{n\delta\pi}{2} + \frac{2V_{out}}{n\pi}\left(\sin n\gamma_Q + j\cos n\gamma_Q\right)}{\frac{1}{jn\omega_{sw}C_{res}} + jn\omega_{sw}L_{res} + R_{par}} \tag{9a}$$

$$\sum_n \|I_{x,n}\|\cos\left(n\gamma_0 + \angle I_{x,n}\right) = 0 \tag{9b}$$

$$\frac{1}{\omega_{SW}}\int_{\gamma_0}^{\gamma_Q}\left(\sum_n \|I_{x,n}\|\cos\left(n\tau + \angle I_{x,n}\right)\right)d\tau = Q_{par} \tag{9c}$$

[3]Although this is possible with SPICE, having a semi-analytical model is useful for generating and testing large sets of operating points.

Equation (9a) needs to be solved for each harmonic used in the analysis. Equations (9a) and (9c) provide the time domain constraints. To arrive at solution, a numerical iteration was performed over γ_Q with the zero crossing of the time domain waveform reconstructed using (9a), evaluated with the concurrent value of γ_Q. By comparing this model to LTspice IV simulations, it has been determined that adding more harmonics to the analysis increases the accuracy in predicting power delivery through the effect that including more harmonics has on shifting the angles γ_0 and γ_Q, and not through the actual power transfer through the harmonics. Since it is often impractical to model the resonant components at a frequency beyond the 5^{th} switching harmonic, this was taken as the number considered for this analysis. Comparing results of this method with LTSpice IV simulations, we find that the error in power delivery is less than 7% for powers of up to 400 W with C_{par} in the range of values of the actual components (up to 1.5 nF). Some error is to be expected given the assumptions that went into this model (specifically, ignoring the waveform curvature that is due to charging of a linear capacitor, in favor of a much analytically simpler square wave).

An almost identical procedure is performed for the full-bridge MOSFETs. The different value of C_{par} needs to be taken (per the datasheet and any additional capacitance used) and the fact that the primary-side resonant current is N times greater than the secondary-side current often results in $\theta_{critical}$ being close to zero. Equation (10) gives an expression for $\theta_{critical}$ in terms of $\gamma_{Q,FB}$, which is defined as the angle at which the current completely commutates between the low and the high side of one leg of the full-bridge. The two legs are not symmetric in this regard: typically the lagging leg switches near the peak of i_x, which requires a smaller critical angle for that half-bridge. It is also possible that the MOSFET is unable to change its state before the current fully commutates. In that case, extra drain to source capacitance may be placed on the lagging leg MOSFETs to ensure no overlap loss, even near peaks of resonant current.

$$\theta_{critical} = \gamma_{Q,FB} - \gamma_0 \tag{10}$$

Having arrived at a consistent solution (to within some tolerance), the deadtimes for full-bridge and cycloconverter switching are computed as given by (11). The two safety factors (SF) are some values between one and two. They are included to compensate for the assumptions made about v_{cc} and v_{FB}. Physically, the aforementioned procedure calculates the time to deliver approximately half of the required charge. Since the resonant current is typically rising at that point (and definitely not falling), the time to deliver the full charge is at most twice of the calculated value and is at least the same. Selecting these factors refers to the tradeoff between more robust and more efficient operation of the inverter. The final control input is the cycloconverter phase that is given by (12a) for the high side of the positive-output-polarity cycloconverter half-bridge and by (12b) for the negative polarity half-bridge. Since the operation is identical for the two halves, a simple change of phase is required when switching polarity. The safety factor $SF_{CC,on}$ is generally smaller than SF_{cc} of (11b) and is also meant to absorb any shortcomings in the model and guarantee that the devices never turn on too early.

$$deadtime_{FB} = SF_{FB} \times \frac{\gamma_{Q,FB}}{\omega_{sw}} \tag{11a}$$

$$deadtime_{cc} = SF_{cc} \times \frac{\gamma_Q}{\omega_{sw}} \tag{11b}$$

$$\gamma_{on,HS,pos} = \gamma_0 + SF_{cc,on} \times deadtime_{cc} \tag{12a}$$

$$\gamma_{on,HS,neg} = \gamma_{on,HS,pos} + \pi \tag{12b}$$

The presented model may be extended to the non-minimal ϕ mode of operation, for example, by adding an extra angle ϕ_s to both limits of integration in (9c). This would mean that each of the cycloconverter MOSFETs starts conduction ϕ_s radians after the earliest that it can do so. Finally, the assumption of a fixed parasitic resistance may be inaccurate across a wide frequency range. It is possible to use different values in different frequency bands or to provide an analytical estimate instead.

F. Resonant component sizing

Specifying an operating point determines the minimum ϕ and the corresponding minimum $i_{x,rms}$. The values of the resonant components determine the switching frequency. Reducing resonant frequency reduces loss in all circuit elements. This may be achieved by reducing the resonant frequency through selection of larger values for L_{res} and C_{res}, which may require physically larger circuit components. Selecting frequency range is thus a balance between size and efficiency.

The lowest allowed switching frequency is determined by the natural frequency of the resonant tank: $\frac{1}{2\pi\sqrt{L_{res}C_{res}}}$. The switching frequency range beyond resonance is determined by the tank's characteristic impedance: $\sqrt{\frac{L_{res}}{C_{res}}}$. Using a computer script[4] to sweep through a range of inductor and capacitor values, it was determined that a characteristic impedance of 50-60 Ω (as seen on the secondary side) provided an optimal balance between efficiency and component values. In addition, a resonant frequency of about 40 kHz gave an acceptable balance between efficiency and passive component size. The final component values used in the prototype are given in Table III. Using a similar procedure to compare current sloshing to the presented control scheme, it was determined that for our component values, operating with current sloshing is not needed[5].

[4]A script was set up to implement the described control method for the fundamental frequency analysis only given a set of resonant component values. For each case, a CEC efficiency was estimated using loss models instead of a single parasitic resistor. Using the fundamental-only analysis was necessary to speed up the computation time to allow to sweep through a large (100s of μH and 10s of nF inductance and capacitance, respectively) range of resonant component values. This script is shown in appendix C of [14].

[5]In general, current sloshing is less efficient unless the natural frequency of the resonant tank is selected greater than approximately 200 kHz. However, the efficiency at those frequencies is at least one percent lower than in the selected range.

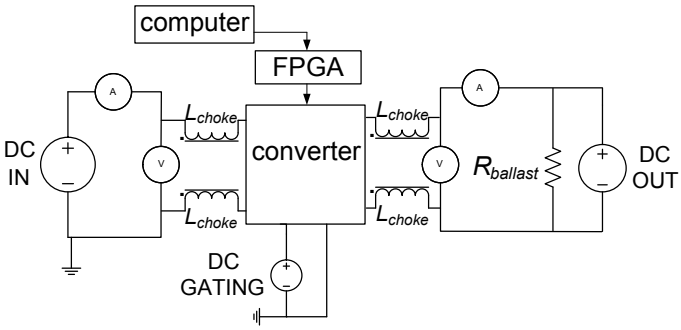

Fig. 5. Experimental setup diagram for testing with positive output voltage polarity. The 'DC OUT' supply connection is reversed for negative polarity.

The frequency consideration gives preference to a lower turns ratio of the transformer. Higher N gives higher voltage amplification and requires switching at a higher frequency to achieve the same power transfer as a lower turns ratio at a lower frequency. The minimum turns ratio, as dictated by the fundamental components of the full-bridge and the cycloconverter waveforms at the minimum input and the maximum output voltages, with $\delta = 1$, is given by (13). A turns ratio of 7.5 is chosen for the prototype.

$$N_{min} = \frac{V_{cc,1,max}}{V_{FB,1,min}} = \frac{\frac{2}{\pi}240\sqrt{2}}{\frac{4}{\pi}25} \approx 6.8 \qquad (13)$$

III. Experimental verification

A. Testing setup

A prototype has been built and tested. Fig. 6 shows the populated prototype board. Table III specifies the circuit components of the tested design. Testing was performed using static DC voltages at the output. To approximate the line cycle, 8 or 9 output voltages were tested for each average power level. Due to symmetry, only one quarter of the line cycle is unique in its operation. Fig. 5 shows the experimental setup. The output voltage was controlled by a DC power supply connected to a ballast resistor. The common mode chokes were important at the output as that power supply was not grounded. Two 20 mH chokes were used in series. The input and output power were monitored by two meters per port. The auxiliary DC power supply labeled 'DC gating' provided the power to gate all eight MOSFETs. The front panel of that supply was used to monitor this component of loss. At each DC operating point, the inverter was controlled in an open loop manner, with static gating waveforms being supplied by an FPGA development board (the power for which is not considered in the efficiency summary).

B. Results

The converter was tested with output voltages ranging from 20 to 90 degrees along the AC line cycle, spaced by 10 degrees (this is a range of 115 to 339 V). For average power levels of 50% and higher, the 10 degree measurement was also taken (58 V). The safety factors (of (11), (12)) used for the model were as follows: full-bridge - 1, cycloconverter deadtime - 2, cycloconverter turn on - 1.5. A table of control inputs and

TABLE III
Prototype parameters

C_{res}	4.4 μF, 20×.22 μF Ceramic C0G
C_{block}	2 μF, 2× 1.0 μF Capstick 105K400CS6G
L_{res}	3.9 μH ETD-54 core, 3C90 4 turns of 8400×AWG44
Transformer	N = 7.5, RM14-3C95 Primary: 4 turns of 600×AWG40 Secondary: 32 turns of 80×AWG40
Full Bridge FETs	ST STB160N75F3
Cycloconverter FETs	Infineon IPP60R250CP
Switching frequency	45-350 kHz

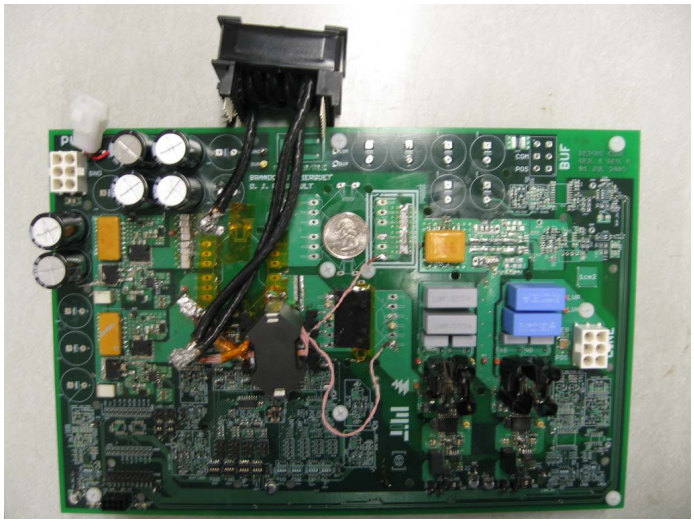

Fig. 6. Photograph of the prototype converter with a U.S. quarter-dollar coin. This circuit board is designed to be configurable for multiple different topologies and control options, so is considerably larger than strictly necessary.

the resulting converter outputs was generated by sweeping the switching frequency from resonance to about 400 kHz and the full-bridge pulse width from 0.35 to 0.99 in steps of 0.01, for each output voltage. The input voltage was fixed at 32.5 V. To provide accuracy in power delivery (to properly simulate an AC line cycle), a computer script adjusted the control inputs until the power delivery was within 3% of what is desired. In general this was achieved in 2 steps or less.

Fig. 7 shows the measured efficiency as a function of instantaneous power delivered over a quarter line cycle for 32.5 V at the input. Assuming that the efficiency is 0 when 0 W is delivered and assigning a CEC weight of 0.09 to the 20% average power case (the 10% case was skipped) the overall CEC efficiency of the prototype is approximately 95.9%. Fig. 8 shows typical waveforms of converter operation.

Results for a single (negative) polarity of the output voltage are presented. However, both halves of the cycloconverter were tested with their respective output polarities. Additionally, the output voltage and the operating point were adjustable (across the operating range) while the converter was running. This gives confidence in the design being suitable for true DC/AC conversion.

An immediate area of revision is an improved layout. It was determined that layout contributes to the ringing on the full-bridge and higher than expected parasitic impedance. In fact, measurements have shown that between 6 and 12% of

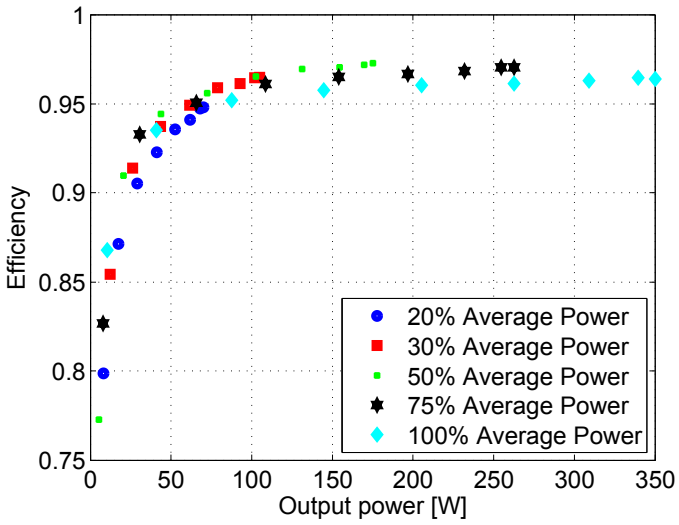

Fig. 7. Efficiency vs. instantaneous delivered power. For each average power level, different points correspond to different output voltages.

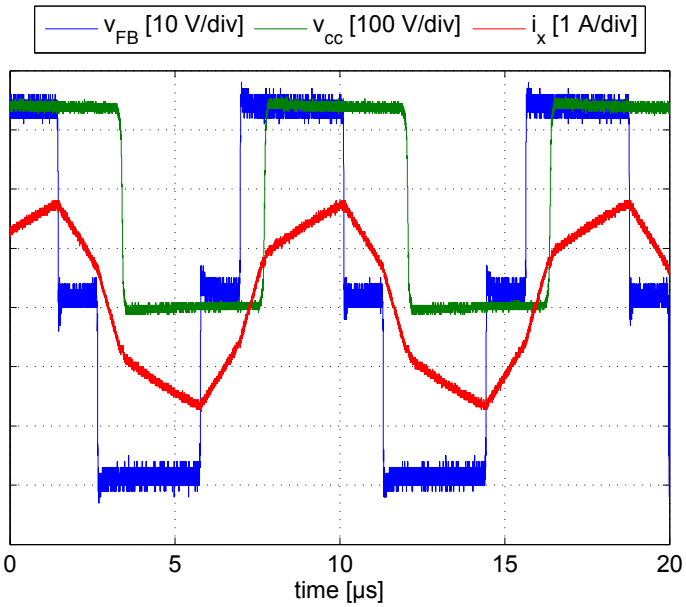

Fig. 8. Experimental waveforms taken with the prototype converter. V_{IN}: 32.5 V, V_{out}=338.9 V, output power: 175.1 W, input power: 179.3 W, DC gating power: 0.7 W, Net efficiency: 97.3%. Switching frequency: 115 kHz, resonant current: 1.19 A cycle *rms*, 3.56 A peak to peak.

loss comes from the high frequency ESR of the primary-side current loop. Additionally, utilizing a different MOSFET package would allow for devices which are projected to yield higher efficiency.

IV. Conclusion

This paper introduces a microinverter for single-phase PV applications that is suitable for conversion from low-voltage (25-40 V) DC to high voltage AC (e.g. 240 V_{rms} AC). The topology is based on a full-bridge series resonant inverter, a high-frequency transformer, and a novel half-wave cyclo-converter. The operational characteristics are analyzed, and a multidimensional control technique is utilized to achieve high efficiency, encompassing frequency control, inverter phase shift control and cycloconverter phase control. An experimental prototype is demonstrated which achieves 95.9% CEC efficiency and higher efficiencies appear to be attainable. Further details about this work may be found in [14].

Acknowledgments

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References

[1] Xiaoming Yuan; Yingqi Zhang, "Status and Opportunities of Photovoltaic Inverters in Grid-Tied and Micro-Grid Systems," Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International , vol.1, no., pp.1-4, 14-16 Aug. 2006

[2] Kjaer, S.B.; Pedersen, J.K.; Blaabjerg, F., "A review of single-phase grid-connected inverters for photovoltaic modules," Industry Applications, IEEE Transactions on , vol.41, no.5, pp. 1292- 1306, Sept.-Oct. 2005

[3] Amirabadi, M.; Balakrishnan, A.; Toliyat, H.A.; Alexander, W., "Soft switched ac-link direct-connect photovoltaic inverter," Sustainable Energy Technologies, 2008. ICSET 2008. IEEE International Conference on , vol., no., pp.116-120, 24-27 Nov. 2008

[4] Lohner, A.; Meyer, T.; Nagel, A., "A new panel-integratable inverter concept for grid-connected photovoltaic systems," Industrial Electronics, 1996. ISIE '96., Proceedings of the IEEE International Symposium on , vol.2, no., pp.827-831 vol.2, 17-20 June 1996

[5] Quaschning, V.; Hanitsch, R., "Influence of shading on electrical parameters of solar cells," Photovoltaic Specialists Conference, 1996., Conference Record of the Twenty Fifth IEEE , vol., no., pp.1287-1290, 13-17 May 1996

[6] Quan Li; Wolfs, P., "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," Power Electronics, IEEE Transactions on , vol.23, no.3, pp.1320-1333, May 2008

[7] Bhat, A.K.S.; Dewan, S.D., "Resonant inverters for photovoltaic array to utility interface," Aerospace and Electronic Systems, IEEE Transactions on , vol.24, no.4, pp.377-386, Jul 1988

[8] Yaosuo Xue; Liuchen Chang; Sren Baekhj Kjaer; Bordonau, J.; Shimizu, T., "Topologies of single-phase inverters for small distributed power generators: an overview," Power Electronics, IEEE Transactions on , vol.19, no.5, pp. 1305- 1314, Sept. 2004

[9] Henze, C.P.; Martin, H.C.; Parsley, D.W., "Zero-voltage switching in high frequency power converters using pulse width modulation," Applied Power Electronics Conference and Exposition, 1988. APEC '88. Conference Proceedings 1988., Third Annual IEEE , vol., no., pp.33-40, 1-5 Feb 1988

[10] Ho, B.M.T.; Henry Shu-Hung Chung, "An integrated inverter with maximum power tracking for grid-connected PV systems," Power Electronics, IEEE Transactions on , vol.20, no.4, pp. 953- 962, July 2005

[11] Kawabata, T.; Honjo, K.; Sashida, N.; Sanada, K.; Koyama, M., "High frequency link DC/AC converter with PWM cycloconverter," Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE , vol., no., pp.1119-1124 vol.2, 7-12 Oct 1990

[12] Jih-Sheng Lai, "Power conditioning circuit topologies," Industrial Electronics Magazine, IEEE , vol.3, no.2, pp.24-34, June 2009

[13] Bower, W.; Whitaker, C.; Erdman, W.; Behnke, M.; Fitzgerald, M., "Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems," Prepared for the California Energy Commission, Oct 2004.

[14] A.Trubitsyn, "High Efficiency DC/AC Power Converter for Photovoltaic Applications," S.M. thesis, Department of Electriacal Engineering, Massachusetts Institute of Technology, MA, 2010.