TABLE IV
PERFORMANCE COMPARISON

Reference	[25]	[26]	[27]	[28]	[29]	**This work**
Year	2011	2004	2004	1997	2012	
Topology	Buck	Cascaded Buck	Buck	Cascaded buck	Cascaded buck	Merged two-stage
Technology	0.35 μm	0.25 μm	0.6 μm	0.15 μm	0.35 μm	0.18 μm
Input Voltage	2.7-4.2 V	2.8-5.5 V	3-5.2 V	3.3 V	2.5-5 V	4.0-5.5 V
Output Voltage	2.4 V	1.0-1.8	V_{in} - 0.2 V	1.65 V	1.0-1.8 V	0.8-1.3 V
Switching Frequency	5 MHz	0.5-1.5 MHz	300 kHz-1 MHz	12.8 MHz	1.3 MHz	10 MHz
Efficiency (η_{peak})	91 %	92%	89.5%	75%	94%	81%
Voltage step-down at η_{peak}	3.3 V to 2.4 V	4 V to 1.5 V	3.6 V to 2.0 V	3.3 V to 1.65 V	2.5 V to 1.8 V	5.0 V to 1.3 V
Output power	0.12 W to 1.2 W	0.15 mW to 0.6 W	0.1 W to 0.8 W	8.25 mW to 82.5 mW	18 mW to 0.675 W	0.3W to 0.8 W

IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers (ISSCC), pp. 210–211, 2010.

[23] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Kluwer Academics, 2000.

[24] P.-L. Wong, F. Lee, X. Peng, and K. Yao, "Critical inductance in voltage regulator modules," *IEEE Transactions on Power Electronics*, vol. 17, no. 4, pp. 485–492, 2002.

[25] M. Du, H. Lee, and J. Liu, "A 5-MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1928–1938, 2011.

[26] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4μA quiescent-current dual-mode digitally controlled buck converter ic for cellular phone applications," *IEEE Journal of Solid State Circuits*, vol. 39, no. 12, pp. 2342–2348, 2004.

[27] F. Lee and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, 2004.

[28] S. Reynolds, "A DC–DC converter for short-channel CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 111–113, 1997.

[29] H. Nam, Y. Ahn, and J. Roh, "5-V buck converter using 3.3-V standard CMOS process with adaptive power transistor driver increasing efficiency and maximum load capacity," *IEEE Transactions on Power Electronics*, vol. 27, pp. 463–471, 2012.

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