

# An Electrolytic-Free Offline LED Driver with a Ceramic-Capacitor-Based Compact SSC Energy Buffer

Minjie Chen<sup>†</sup>, Yu Ni<sup>‡</sup>, Curtis Serrano<sup>†</sup>, Benjamin Montgomery<sup>†</sup>, David Perreault<sup>†</sup>, Khurram Afridi<sup>‡</sup>

<sup>†</sup>Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

<sup>‡</sup>University of Colorado at Boulder, Colorado 80309, USA

Email: minjie@mit.edu

**Abstract**—This paper presents the design and implementation of a compact ceramic-capacitor-based stacked switched capacitor (SSC) energy buffer for a single-stage offline 8-W 21-V output electrolytic-free LED driver. The elimination of the electrolytic capacitors can lead to a longer lifetime for the LED driver. Compared to earlier works, this design of the SSC energy buffer has a simpler ground-referenced gate drive circuit and eliminates the need for a separate precharge circuit. The prototype LED driver presented here uses a ceramic-capacitor-based SSC energy buffer with optimized capacitor sizing that provides substantially higher effective energy density than electrolytic capacitors. The improvement in energy density is achieved in part by a design approach which optimizes the ratio of the capacitance values of the capacitors in the SSC energy buffer. The prototyped SSC energy buffer achieves a round-trip efficiency of above 98%. The total passive volume of the ceramic capacitors in the prototype is less than half the volume of the electrolytic capacitors it replaces.

## I. INTRODUCTION

Single-phase high-power-factor ac/dc converters require twice-line-frequency energy storage to buffer the difference between the dc and ac side instantaneous power. The size of this energy buffer is proportional to the converters power rating and the line period and cannot be reduced by simply increasing the switching frequency of the converter. Generally, electrolytic capacitors are used for energy buffering owing to their relatively high energy density. However, due to their lifetime and temperature constraints there is a desire to eliminate electrolytic capacitors in applications which require long lifetime, such as LED drivers and solar micro-inverters [1]–[3]. Film and ceramic capacitors have much longer lifetime. However, their energy densities are an order of magnitude lower than that of electrolytic capacitors. Since film and ceramic capacitors can be efficiently charged and discharged over a wide voltage range at fairly high frequencies, a larger fraction of their energy storage capacity can be utilized compared to electrolytics. Hence, film and ceramic based energy buffers can be designed with effective energy densities comparable to that of electrolytic capacitors. A number of approaches to effectively utilize film or ceramic capacitors while maintaining a narrow range dc bus voltage have been proposed, including using bi-directional converters [4], energy buffers incorporated into the operation of the power stage [5]–[7], and

energy buffers that utilize switched capacitor circuits [8]–[12]. However, these approaches suffer from efficiency, flexibility or complexity limitations.

A stacked switched capacitor (SSC) energy buffer approach has recently been presented that overcomes some of these limitations [13]–[15]. This paper introduces an improved SSC energy buffer design that has very high effective energy density, and is suitable for single-phase single-stage ac/dc converters, such as offline LED drivers. Compared to earlier SSC implementations, this design also has much simpler ground-referenced gate drives and eliminates the need for a separate precharge circuit. It is also the first prototype with a ceramic-capacitor-based SSC energy buffer. The improvement in energy density is achieved in part by a new design approach which optimizes the ratio of the capacitance values of the capacitors in the SSC energy buffer. This SSC energy buffer has been prototyped for an offline single-phase 8 W 21 V output LED driver. The prototype SSC energy buffer achieves a round-trip efficiency of above 98%, and the total passive volume of the ceramic capacitors in the prototype is less than half the volume of the electrolytic capacitors it replaces.

The remainder of this paper is organized as follows: Section II introduces the operational principles of the SSC energy buffer used in the offline LED driver. Design optimization of the SSC energy buffer is presented in section III. Section IV provides the implementation details of the ceramic-capacitor-based SSC energy buffer for the single-stage offline 8 W 21 V output LED driver. The experimental results are presented in section V. Finally, section VI concludes the paper.

## II. SSC ENERGY BUFFER FOR AN LED DRIVER

An SSC energy buffer comprises two series-connected blocks of switches and capacitors: backbone block and supporting block, as shown in Fig. 1. It works on the principle that while the voltages across the individual blocks (and individual capacitors) vary over a wide range, these voltage variations of the two blocks tend to cancel each other. Therefore, the dc bus voltage is maintained within a desired narrow range. By allowing large variations in individual capacitor voltages, the SSC energy buffer significantly improves the utilization

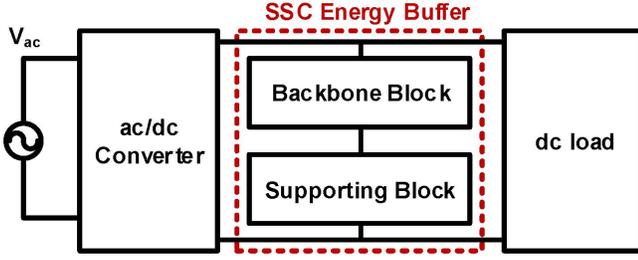


Fig. 1. Stacked Switched Capacitor (SSC) energy buffer architecture.

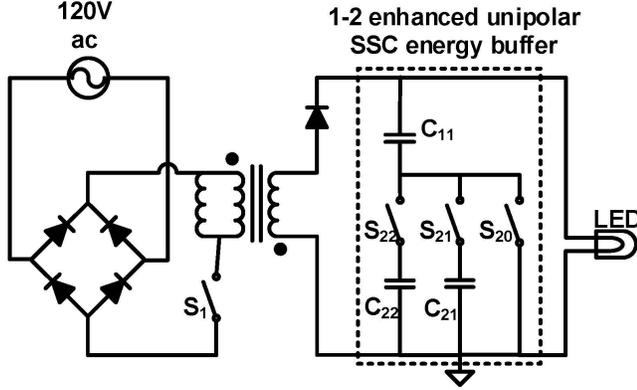


Fig. 2. A 1-2 enhanced unipolar SSC energy buffer as part of an offline single-stage LED driver.

of the energy stored in the capacitors. This increases the effective energy density of the energy buffer. Furthermore, the switches in the SSC energy buffer switch at low multiples of the line frequency, minimizing switching losses. This allows the energy buffer to have a high round-trip efficiency.

The SSC energy buffer has many embodiments, allowing tradeoffs to be made between performance and complexity [13], [14]. Among these embodiments is the  $1 - m$  enhanced unipolar SSC energy buffer. It has one backbone capacitor,  $m$  supporting capacitors and  $(m + 1)$  supporting block switches. Because of its relatively low complexity and reasonably high energy utilization, it is suitable for offline single-stage LED drivers, and is the SSC architecture that is optimized and implemented in this work. Figure 2 shows the schematic of a 1-2 enhanced unipolar SSC energy buffer as part of an offline single-stage LED driver. The LED driver shown in Fig. 2 is a flyback converter (similar to the one used for prototype development and testing in this paper), and the SSC energy buffer replaces the electrolytic capacitors that were at the output of this converter. The LED driver used in this paper has a nominal output voltage of 21 V and a peak-to-peak ripple of 2 V.

Before the buffer starts normal operation, the capacitors are precharged to appropriate voltage levels through a specific precharge switching sequence. In the 1-2 enhanced unipolar SSC energy buffer investigated in this paper, the voltage of  $C_{11}$ ,  $V_{C11}$ , is precharged to 18 V, the voltage of  $C_{21}$ ,  $V_{C21}$ , is precharged to 1 V, and the voltage of  $C_{22}$ ,  $V_{C22}$ , is precharged

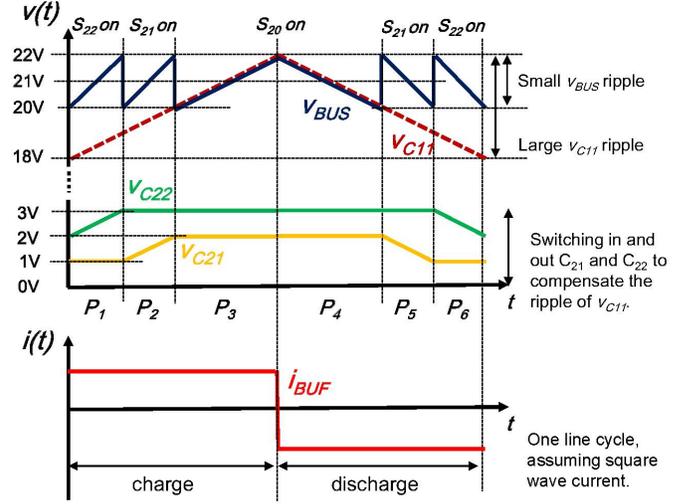


Fig. 3. Operation waveforms of a 1-2 enhanced unipolar SSC energy buffer.

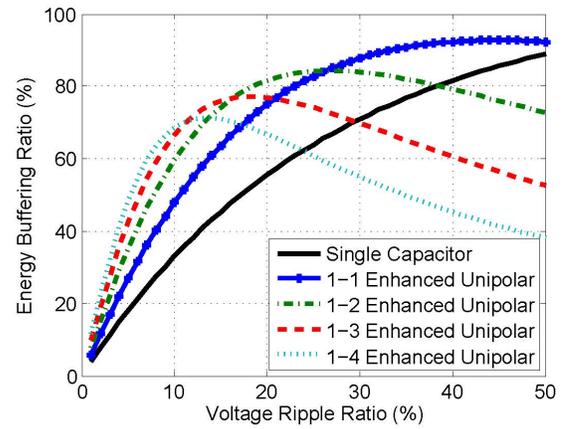


Fig. 4. Energy buffering ratio of the  $1 - m$  enhanced unipolar SSC energy buffer as a function of ripple ratio with different number of supporting capacitors ( $m$ ). The energy buffering ratio for a single capacitor is also shown for comparison.

to 2 V. When precharging starts,  $S_{21}$  and  $S_{22}$  are both turned on to charge  $C_{21}$  and  $C_{22}$  to 1 V. After this,  $S_{21}$  is turned off, and  $S_{22}$  is kept on to continue charging  $C_{22}$ . When  $V_{C22}$  reaches 2 V,  $S_{22}$  is turned off and  $S_{20}$  is turned on to charge  $C_{11}$ . Once  $V_{C11}$  reaches 18 V, the precharge stage is completed and the SSC energy buffer enters normal operation.

Figure 3 shows the main waveforms of the 1-2 enhanced unipolar SSC energy buffer during normal operation. In each switching cycle, there is a symmetrical charging and discharging process. The charging process of the SSC buffer can be divided into the following three intervals:

- 1) P1 - charging  $C_{11}$  and  $C_{22}$ : when the energy buffer is to be charged,  $S_{22}$  is turned on (and all the other switches are off).  $C_{11}$  and  $C_{22}$  are charged during this period, and  $C_{21}$  is not connected. When the dc bus voltage,  $V_{BUS}$ , reaches 22 V,  $V_{C11}$  becomes 19V. Then  $S_{22}$  is turned off and  $S_{21}$  is turned on.  $V_{C21}$  (1 V) adds to  $V_{C11}$  (19

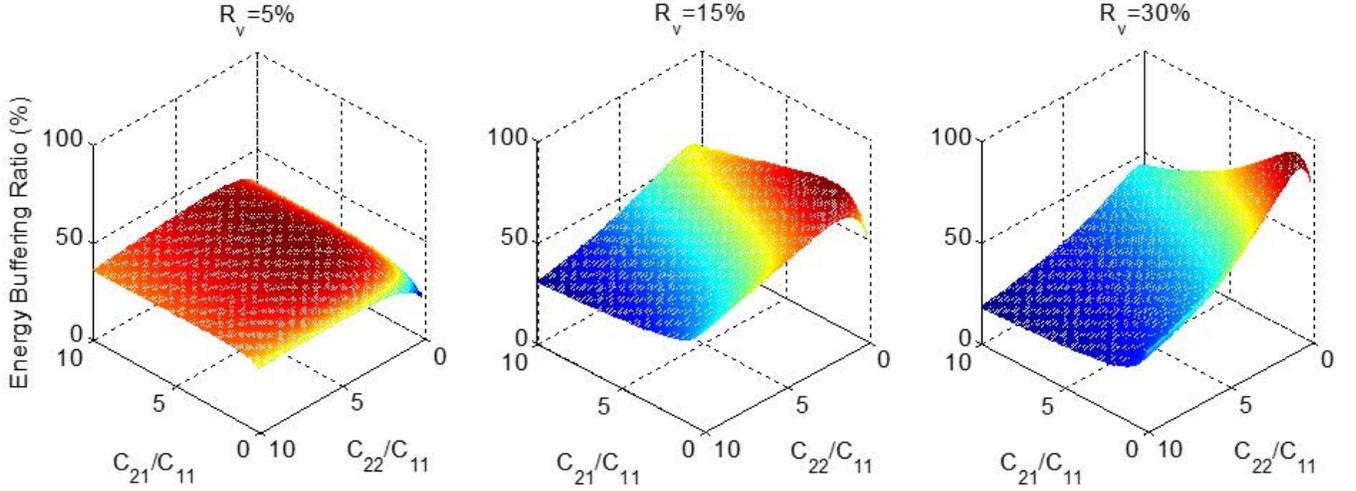


Fig. 5. Energy buffering ratio of a 1-2 enhanced unipolar SSC energy buffer as a function of the ratio of its capacitances ( $\frac{C_{21}}{C_{11}}$  and  $\frac{C_{22}}{C_{11}}$ ) for different ripple ratios ( $R_v$ ): (a)  $R_v = 5\%$ , (b)  $R_v = 15\%$ , and (c)  $R_v = 30\%$ .

V) and elevates  $V_{BUS}$  back to 20 V.

- 2) P2 - charging  $C_{11}$  and  $C_{21}$ : During this period,  $S_{21}$  is on.  $C_{11}$  and  $C_{21}$  are charged in series until  $V_{BUS}$  reaches 22 V again. This time  $V_{C11}$  becomes 20 V, and  $V_{C21}$  increases to 2 V. Then  $S_{21}$  is turned off, and  $S_{20}$  is turned on. The dc bus voltage equals the voltage of  $C_{11}$  (20 V).
- 3) P3 - charging  $C_{11}$  only: During this period, only  $S_{20}$  is on.  $C_{11}$  is charged until  $V_{BUS}$  reaches 22 V.

At this time, all capacitors have reached their maximum voltage ( $V_{C11} = 22$  V,  $V_{C21} = 2$  V and  $V_{C22} = 3$  V). The SSC energy buffer cannot be further charged. As a result, for a given maximum power of the ac-dc converter, the size of the capacitors needs to be large enough to ensure this charging limit is never exceeded.

The discharging process (P4 to P6) is simply the reverse of the charging process.

### III. DESIGN OPTIMIZATION

Important design parameters for an SSC energy buffer are the voltage ripple ratio ( $R_v$ ) and the energy buffering ratio ( $\Gamma_b$ ). The voltage ripple ratio is defined as the ratio of the peak voltage ripple amplitude (half of peak-to-peak ripple) to the nominal value of the dc bus voltage. The energy buffering ratio is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer. Maximizing the energy buffering ratio for a given voltage ripple ratio ensures better usage of a given amount of capacitor energy storage capacity. The energy buffering ratio for a 1- $m$  enhanced unipolar SSC energy buffer (with all capacitors having equal capacitance) as a function of voltage ripple ratio ( $R_v$ ) and number of supporting capacitors ( $m$ ) is given by [14]:

$$\Gamma_b = 1 - \frac{(1 + 2^2 + 3^2 + \dots + m^2)R_v^2 + (1 - (m + 1)R_v)^2}{(2^2 + 3^2 + \dots + (m + 1)^2)R_v^2 + (1 + R_v)^2}. \quad (1)$$

This expression for energy buffering ratio is plotted as a function of ripple ratio in Fig. 4 for four different values of the number of supporting capacitors ( $m$ ). From Fig. 4 it can be seen that the 1-2 enhanced unipolar SSC energy buffer provides a good tradeoff between energy density and circuit complexity (which increases with increasing  $m$ ). Therefore, it is selected as the topology of choice for the prototype developed in this paper.

The conventional SSC designs [13], [14] uses capacitors of equal capacitance value. However, further improvements in energy buffering ratio are possible if the capacitance ratios of these capacitors are optimized [15]. The energy buffering ratio for a 1-2 enhanced unipolar SSC energy buffer with arbitrary capacitance values for the three capacitors ( $C_{11}$ ,  $C_{21}$  and  $C_{22}$ ) is given by:

$$\Gamma_b = 1 - \frac{[1 - R_v - 2R_v(\frac{\alpha_{21}}{1+\alpha_{21}} + \frac{\alpha_{22}}{1+\alpha_{22}})]^2}{(1 + R_v)^2 + 4\alpha_{22}R_v^2[1 + \frac{\alpha_{21}}{1+\alpha_{21}}]^2 + 4\alpha_{21}R_v^2} - \frac{4\alpha_{22}R_v^2[\frac{\alpha_{21}}{1+\alpha_{21}} + \frac{\alpha_{22}}{1+\alpha_{22}}]^2}{(1 + R_v)^2 + 4\alpha_{22}R_v^2[1 + \frac{\alpha_{21}}{1+\alpha_{21}}]^2 + 4\alpha_{21}R_v^2} - \frac{4\alpha_{21}R_v^2[\frac{\alpha_{21}}{1+\alpha_{21}}]^2}{(1 + R_v)^2 + 4\alpha_{22}R_v^2[1 + \frac{\alpha_{21}}{1+\alpha_{21}}]^2 + 4\alpha_{21}R_v^2}. \quad (2)$$

Here  $\alpha_{21} = \frac{C_{21}}{C_{11}}$  and  $\alpha_{22} = \frac{C_{22}}{C_{11}}$  are the ratios of the capacitances of the two supporting capacitors to the capacitance of the backbone capacitor. When the three capacitors have equal capacitances (i.e.,  $\alpha_{21} = \alpha_{22} = 1$ ), this expression reduces to the expression given in (1) with  $m$  equals to 2.

Figure 5 plots the energy buffering ratio of the 1-2 enhanced unipolar SSC energy buffer as a function of  $\alpha_{21}$  and  $\alpha_{22}$  for three different values of ripple ratio ( $R_v = 5\%$ ,  $R_v = 15\%$ ,  $R_v = 30\%$ ). As can be seen from Fig. 5, the optimal capacitance ratios (i.e.  $\frac{C_{21}}{C_{11}}$  and  $\frac{C_{22}}{C_{11}}$ ) depends on the ripple ratio. The optimal values of  $\frac{C_{21}}{C_{11}}$  and  $\frac{C_{22}}{C_{11}}$  which maximize the energy buffering ratio are plotted as a function of ripple

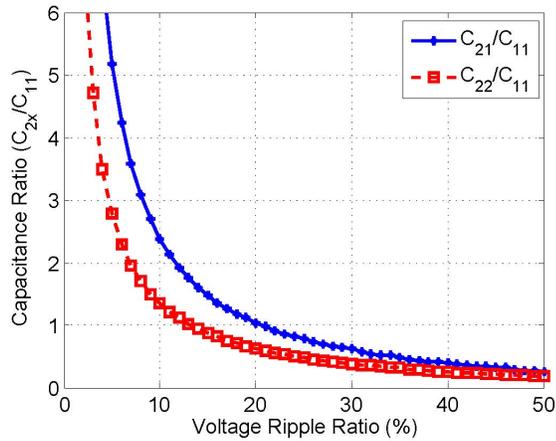


Fig. 6. Optimal capacitance ratios as a function of ripple ratio for the 1-2 enhanced unipolar SSC energy buffer.

ratio in Fig. 6. Note that across the full range of ripple ratios considered, an optimal design uses a larger capacitance value for  $C_{21}$  (the supporting capacitor with the lower voltage) than  $C_{22}$ . Also, as the voltage ripple ratio increases, the capacitance values for both  $C_{21}$  and  $C_{22}$  decrease relative to  $C_{11}$ . The improvement in energy buffering ratio because of this optimization (relative to using capacitors of equal capacitance) are plotted in Fig. 7. The optimization is most beneficial at low and high ripple ratios. This is because if the ripple ratio is in the 15-20% range, the optimal capacitance ratios are quite close to unity.

#### IV. PROTOTYPE DESIGN

A prototype ceramic-capacitor-based 1-2 enhanced unipolar SSC energy buffer has been designed and built as part of an offline LED driver. Compared to previous implementations, this design places specific emphasis on demonstrating the reduced size of the energy buffer. An LM3444 120-V<sub>ac</sub> 8-W LED driver evaluation board is used as the design platform for this prototype. The evaluation board has a flyback converter functioning as the grid-tied power factor correction circuit (PFC), and uses two 330  $\mu\text{F}/35\text{ V}$  electrolytic capacitors for twice-line-frequency energy buffering. In this paper, these capacitors are replaced by a 1-2 enhanced SSC energy buffer. Figure 8 shows the full schematic of the prototype comprising the flyback converter and the SSC energy buffer.

The nominal output voltage of the LED driver is 21 V with 2 V peak-to-peak voltage ripple (i.e.,  $R_v = 5\%$ ) when the output power is 8 W. From Fig. 6, the optimized capacitance ratios for a ripple ratio ( $R_v$ ) of 5% are:  $\alpha_{21} = 5.18$  and  $\alpha_{22} = 2.78$ . Table I lists the required optimized capacitance values and voltage ratings for the three capacitors ( $C_{11}$ ,  $C_{21}$  and  $C_{22}$ ) of the SSC energy buffer. Also listed in Table I are the design values for the SSC energy buffer when equal capacitances are used, and the design values for a single capacitor solution. The total energy storage capacities of these three alternative designs are also given in Table I. The SSC energy buffer with optimized capacitance ratios requires the least energy storage

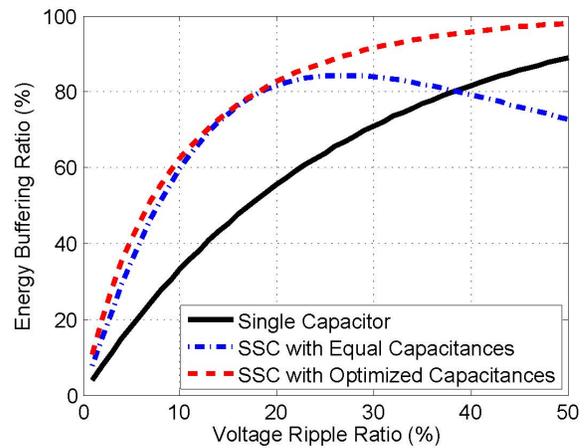


Fig. 7. Improvements of energy buffering ratio due to capacitance ratio optimization in a 1-2 enhanced unipolar SSC energy buffer.

TABLE I  
CAPACITANCE VALUES AND VOLTAGE RATING OF THE CAPACITORS NEEDED IN AN 8-W 21-V OUTPUT OFFLINE LED DRIVER WITH THREE DIFFERENT TYPES OF ENERGY BUFFERS: AN SSC ENERGY BUFFER WITH OPTIMAL CAPACITANCE RATIOS, AN SSC ENERGY BUFFER WITH EQUAL CAPACITANCES, AND A SINGLE-CAPACITOR ENERGY BUFFER. THE TOTAL ENERGY STORED IN THE ENERGY BUFFERS IS ALSO INDICATED.

|             | SSC Energy Buffer         |                         | Single Capacitor       |
|-------------|---------------------------|-------------------------|------------------------|
|             | Optimal Capacitance Ratio | Equal Capacitance       | Single Capacitance     |
| $C_{11}$    | 22 V, 195 $\mu\text{F}$   | 22 V, 253 $\mu\text{F}$ |                        |
| $C_{21}$    | 2.0 V, 1100 $\mu\text{F}$ | 2 V, 253 $\mu\text{F}$  | 22V, 505 $\mu\text{F}$ |
| $C_{22}$    | 3.7 V, 573 $\mu\text{F}$  | 3 V, 253 $\mu\text{F}$  |                        |
| $E_{total}$ | 0.0532 J                  | 0.0628 J                | 0.1223 J               |

capacity, reflecting its high energy buffering ratio compared to the alternative designs. The values in Table I assume linear capacitors. In practice, the capacitance of ceramic capacitors has a nonlinear dependence on voltage. For this reason the actual capacitance values used are somewhat higher.

The maximum drain-to-source voltages of switches  $S_{21}$ ,  $S_{22}$  and  $S_{20}$  (in Fig. 2) are 1.00 V, 3.72 V and 3.72 V, respectively.  $S_{21}$  needs to block bidirectional voltage, and is implemented with two reverse connected MOSFETs ( $S_{21a}$  and  $S_{21b}$ ), as shown in Fig. 8. All switches need to carry bidirectional current. The rms currents of  $S_{21a}$ ,  $S_{21b}$ ,  $S_{22}$ ,  $S_{20}$  at full load are: 0.17 A, 0.17 A, 0.13 A, 0.16 A, respectively. In the prototype, all switches are implemented with CSD17313Q2 MOSFETs. The four switches are driven by two TC4427 two-channel gate drives. Since the supporting block voltage ( $v_s$ ) never exceeds 3 V, no floating gate drive is required for  $S_{21a}$  and  $S_{22}$ . The grid-tied flyback converter is controlled by a LM3444 controller, and the SSC energy buffer is controlled by a MSP430 microcontroller. The microcontroller senses the dc bus voltage through a resistive voltage divider and produces the four required gate signals. Figure 9 shows a photograph of the SSC energy buffer compared to the electrolytic capacitor that has been replaced, as well as a photograph of the

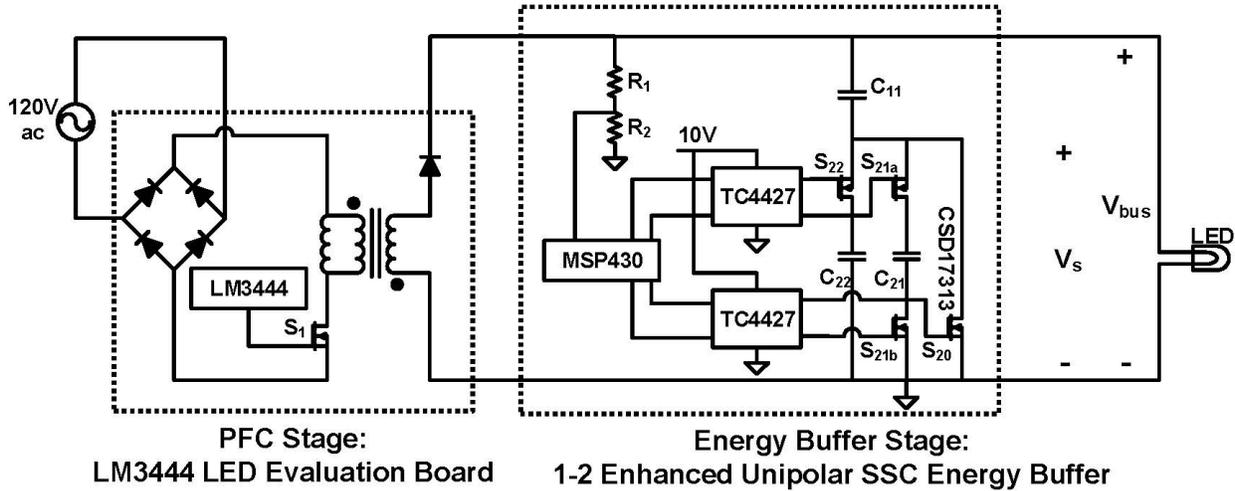


Fig. 8. Switch, gate-drive and control implementation of the prototype SSC energy buffer as part of the offline LED driver.

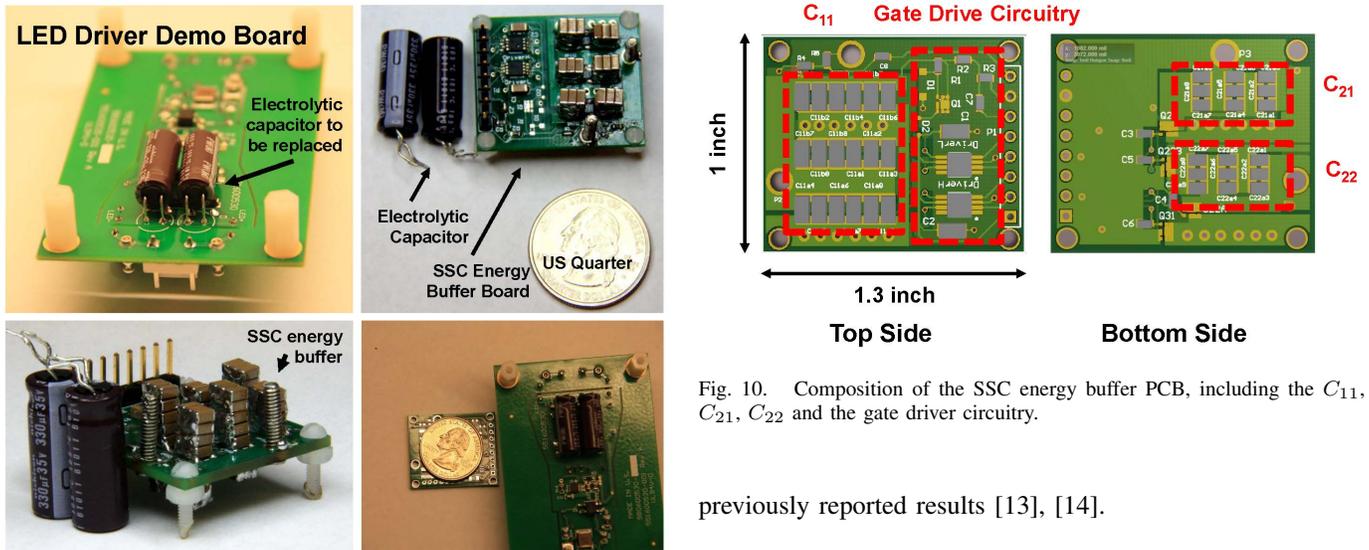


Fig. 9. Photograph comparing the size of the SSC energy buffer to that of the electrolytic capacitors it replaces. Also shown (top) is the LED driver.

LED driver evaluation board. The total volume of the two electrolytic capacitors is  $2010 \text{ mm}^3$ , while the total volume of the ceramic capacitors in the SSC energy buffer is  $975 \text{ mm}^3$ . Figure 10 shows the composition of the SSC energy buffer board. The majority of the board area is occupied by  $C_{11}$ ,  $C_{21}$  and  $C_{22}$ . The board area occupied by the control and gate drive circuits is much smaller and can be further reduced by implementing these as a custom integrated circuits.

Even with all the other circuit elements included, the displaced volume of the SSC energy buffer is not more than the volume of the electrolytic capacitors it replaces; and this volume can be reduced further by taking advantage of the rapid miniaturization and integration trends in semiconductor technology. The SSC-to-electrolytic capacitors passive volume ratio achieved by this prototype is a factor of four better than

Fig. 10. Composition of the SSC energy buffer PCB, including the  $C_{11}$ ,  $C_{21}$ ,  $C_{22}$  and the gate driver circuitry.

previously reported results [13], [14].

## V. EXPERIMENTAL RESULTS

Figure 11 shows the experimental waveforms of the prototype ceramic-capacitor-based SSC energy buffer operating as the twice-line-frequency energy buffer for an offline 8-W 21-V output LED driver. As can be seen the output dc bus voltage ( $v_{bus}$ ) is maintained within the required  $\pm 5\%$  ripple range ( $\pm 1 \text{ V}$ ), even though the individual block voltages vary across a much wider range. The voltage at the switch node ( $v_s$ ) compensates the variations in the voltage across the backbone capacitor  $C_{11}$ , resulting in the small ripple on the dc bus. Figure 11 also shows the grid side voltage  $v_{GRID}$  and current  $i_{GRID}$ . The replacement of the electrolytic capacitor with the SSC energy buffer has no impact on the grid side power factor and THD, which are determined by the PFC stage. The round-trip efficiency of the prototype SSC energy buffer was measured to be 98.2%. A high efficiency is achieved through the use of low ESR ceramic capacitors. Also because the switches in the SSC energy buffer switch at low multiples of the line frequency, the switching losses are very low.

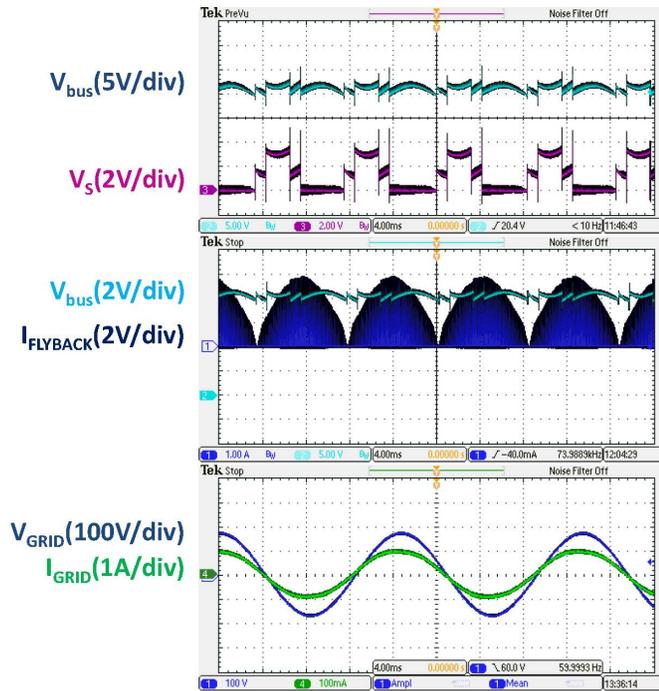


Fig. 11. Measured operation waveforms of the prototype, including the bus voltage  $V_{bus}$ , the voltage at the switch node  $V_s$ , the output current of the flyback converter  $I_{FLYBACK}$ , and the grid current  $I_{GRID}$ .

## VI. CONCLUSIONS

This paper introduces a compact stacked switched capacitor (SSC) energy buffer with ceramic capacitors for twice-line-frequency energy buffering, and demonstrated it in an offline 8-W 21-V output LED driver. The round-trip efficiency of this energy buffer is above 98% and its passive volume is less than half the volume of the electrolytic capacitors it replaces. The elimination of the electrolytic capacitors can lead to a much longer life for the LED driver. The reduction in volume is achieved in part by a new design methodology that optimizes the ratio of the capacitance values of the capacitors in the SSC energy buffer. Also, unlike previous implementations of the SSC energy buffer, this implementation uses simple ground referenced gate-drives and eliminates the need for a separate precharge circuit. All of these enables a compact, high efficiency design of the SSC energy buffer with its overall size comparable to the electrolytic capacitors it replaces.

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