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Fig. 1. A merged two-stage conversion architecture includes a switched capacitor first stage that provides voltage pre-regulation and transformation, and a high-frequency magnetic stage that provides fine regulation of the output. Converters having this architecture may be realized for operation either from wide-range (e.g., 25–200 V) dc voltage or from a rectified 120 V_{rms} ac voltage.
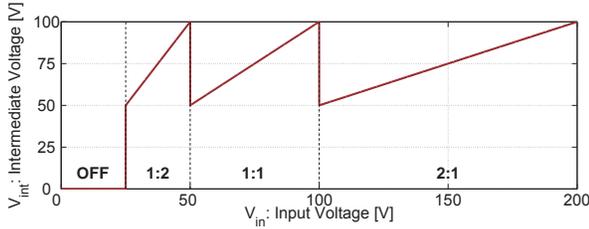

Fig. 2. The voltage transformation characteristic of the switched capacitor (first) stage in a dc-dc converter. The SC circuit is operated in different conversion modes depending upon the input voltage, such that the first stage output voltage varies over a much narrower range than the input voltage.
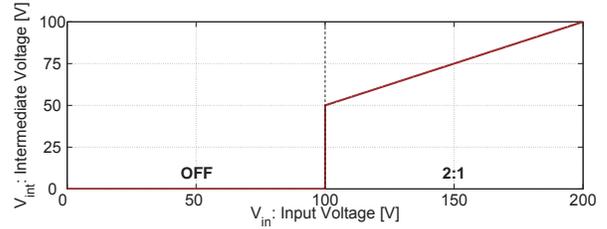

Fig. 3. The voltage transformation characteristic of the switched capacitor (first) stage in an ac-dc converter. The SC circuit is operated with 2:1 conversion ratio only when the input voltage goes above 100 V and is turned off for lower input voltages.

associated circuit design using GaN transistors, and controls to address these challenges, for both wide-range dc voltage and ac-line voltage. Section II of the paper presents the overall system requirements we target along with an overview of the design considerations for LED driver circuits. Section III of the paper presents the proposed architecture, circuit topology, and controls to address the system considerations. Section IV of the paper presents experimental results demonstrating the proposed approach, including implementations for both wide-range dc voltage and ac line voltage. Finally, Section V concludes the paper.

II. SYSTEM REQUIREMENTS AND DESIGN CONSIDERATIONS

The system architecture we adopt targets LED driver circuits operating either from a wide-range dc voltage or from grid-scale ac voltages at low-to-moderate power levels. We introduce circuit implementations and control circuitries suitable for power levels of up to a few tens of watts, wide-range input voltages of up to 200 V (e.g., compatible with 120 V_{rms} ac operation), and LED string voltages in the range of 30-40 V. Furthermore, for ac-line applications we seek designs having high power factor (e.g., Power factor > 0.9), while for dc-input applications we seek efficient operation across a wide input voltage range (e.g., 25-200 V input voltage). Lastly, we target substantial miniaturization of the driver conversion circuit through a combination of system architecture, circuit topology, and adoption of greatly increased switching frequencies.

We begin with an overview of the design considerations in achieving miniaturization of a converter in this application, which operates at high voltages, low powers, and across a

wide range of input voltage. To attain greater miniaturization, increases in switching frequency are necessary because the values of inductors and capacitors vary inversely with switching frequency. However, the sizes of passive components do not necessarily decrease monotonically with frequency, owing to magnetic-core loss, voltage breakdown, and heat transfer limits [6], [16]–[20]. Consequently, achieving substantial miniaturization through high frequency operation further relies upon appropriate passives design and careful selection of circuit topology to minimize the demands placed upon the passive components, especially the magnetic components.

A further consideration is that while passive component size may be made smaller with increased frequency, size reduces relatively slowly with frequency in practice. Moreover, some parasitic elements, such as semiconductor device parasitic capacitances and inductances, do not scale down at all with increased operating frequency. Consequently, the effects of parasitics become increasingly important as operating frequency increases. To achieve miniaturization through extreme high-frequency operation, an effective circuit topology should inherently absorb important parasitic components in its operation.

A third consideration specifically relates to operating characteristics at high voltages and low power levels. Converters operating at high voltages and low currents operate at high characteristic impedance levels, and consequently utilize relatively large inductors and small capacitors (e.g., characteristic impedance $Z_0 = \sqrt{L/C}$ scales as V/I [6]). Furthermore, the values of inductors and capacitors scale down with increasing resonant frequency (e.g., $\omega_0 = 2\pi f = 1/\sqrt{LC}$). Thus, for a given topology operating at high voltage and low current,

increasing switching frequency beyond a certain point may lead to capacitance values that are too small to be practically achievable (e.g., given parasitic capacitance levels) placing a practical bound on frequency and miniaturization. For miniaturization of converters at high voltage and low power, it is preferable to select system architectures and circuit topologies that require relatively low characteristic impedance values (i.e., yielding smaller inductances and larger capacitances) to reduce constraints on scaling up in frequency.

Lastly, operating range and control scheme are important architectural considerations. We consider designs operating either from a wide range dc voltage or from an ac line voltage, such that the system sees a wide range of input voltages. Zero-voltage switching (ZVS) techniques are necessary to reduce capacitive discharge loss and to achieve high-frequency operation at high voltages. However, soft-switching is often difficult to maintain across a wide input voltage range. It is thus an important challenge to develop designs that maintain the desired soft-switched operation across wide voltage conversion ranges.

III. SYSTEM ARCHITECTURE AND CIRCUIT TOPOLOGY

A. System Architecture

To address the above considerations, a merged-two-stage architecture is proposed, as shown in Fig. 1. The first stage is a variable-topology switched-capacitor (SC) circuit operating at moderate switching frequencies (e.g., tens to hundreds of kHz). The SC circuit can achieve high power density and efficiency at these frequencies because it employs only switches and capacitors and incorporates soft-charging operation [12], [13], [21]. However, the SC converter alone cannot efficiently provide the fine voltage regulation capability needed in this application [22]. Instead, this stage serves both to reduce the voltage range over which the second stage needs to operate, and to reduce the maximum voltage level (and hence impedance level) for which the second stage must be designed, in keeping with the design considerations described in the previous section.

The second stage is a magnetic-based stage that provides both additional voltage transformation and fine voltage regulation, and is operated at high frequency (e.g., HF, 3-30 MHz) in order to minimize magnetic component size. High-frequency operation is more readily achieved with high efficiency in the second stage because it operates at lower voltages and smaller voltage range with voltage transformation of the SC first stage. Furthermore, as described below, the topology of the second stage is selected such that it requires relatively small inductor values and inherently absorbs device parasitic capacitance (i.e., the drain-source capacitance of a switch transistor and the diode capacitance) as part of circuit operation, addressing some of the design considerations described in the previous section.

This architecture enables partitioning of the device requirements into "slow switching and high-voltage first stage" and "fast switching and low-voltage second stage" device categories. Moreover, as detailed below the two stages are designed to operate together (merged) in a manner that enables
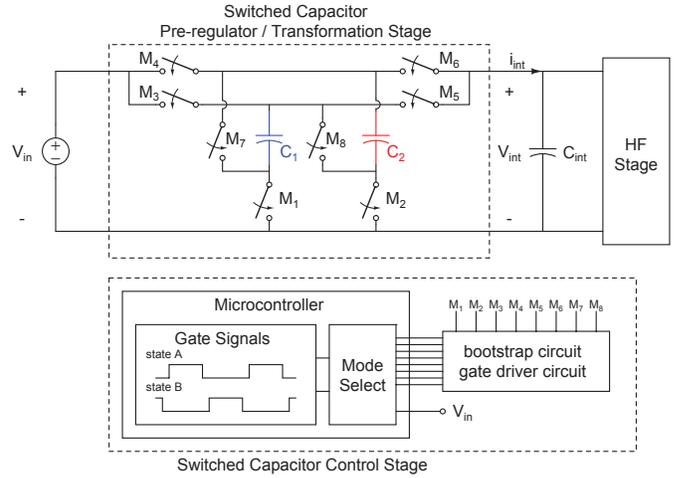

Fig. 4. The switched capacitor pre-regulator / transformation stage is comprised of two energy transfer capacitors and eight switches, and provides nearly continuous input and output currents. The fixed frequency 50% duty ratio gate signal is generated in the microcontroller, and the proper conversion mode is selected depending on the input voltage level.

TABLE II
ON-STATE SWITCHES OF THE SWITCHED CAPACITOR STAGE AT EACH STATE AND CONVERSION MODE

mode	state A	state B
1:2	M1, M3, M6, M8	M2, M4, M5, M7
1:1	M1, M3, M5, M8	M2, M4, M6, M7
2:1	M1, M4, M5, M8	M2, M3, M6, M7

higher efficiency and higher power density than could be achieved in a conventional architecture having separate stages [12], [13], [21], [22]. We describe each of these stages in more detail below.

B. First Stage – Switched Capacitor Circuit

1) SC Power Stage:

The first stage is a variable-topology SC circuit that requires only two energy transfer capacitors and provides nearly continuous input and output currents. To create a suitable intermediate voltage over which the second (regulation) stage can run, the SC transformation stage is operated in different conversion modes, depending upon input voltage. It can operate in three different conversion modes (i.e., 1:2, 1:1, and 2:1 conversion modes). For a wide-input-range dc-dc converter system operating from 25–200 V, all three of these conversion modes are utilized. For an ac-dc converter system operating from ac line voltage, sufficiently high power factor can be achieved through operation only over a limited voltage range in 2:1 mode, as will be detailed in Section III-E. The relations between input and intermediate voltage at the output of the SC first stage are shown in Fig. 2 and Fig. 3 for wide-range dc-dc conversion and ac-dc conversion respectively. Fig. 4 illustrates the power stage of the SC pre-regulator / transformation circuit, which is comprised of two energy transfer capacitors

TABLE III
CONFIGURATION OF THE SWITCHED CAPACITOR CIRCUIT FOR EACH
STATE AND CONVERSION MODE

mode	state A	state B
1:2	$i_{int} \uparrow$ C_2 V_{in} $\downarrow$ C_1 i_{int}	$i_{int} \uparrow$ C_1 V_{in} $\downarrow$ C_2 i_{int}
1:1	V_{in} C_1 C_2 i_{int}	
2:1	$i_{int}/2 \downarrow$ C_2 V_{in} $i_{int}/2 \uparrow$ C_1 i_{int}	$i_{int}/2 \downarrow$ C_1 V_{in} $i_{int}/2 \uparrow$ C_2 i_{int}

and eight switches. The switches turn on and off with 50% duty ratio with dead time. Table II shows the on-state switches in each state and conversion mode, and Table III presents the circuit configuration with this switch operation, where the current source i_{int} models the time-averaged currents drawn by the high-frequency regulation stage.

Additionally, our system is designed to "merge" operation of the two stages. A benefit of such a "merged two-stage" architecture [12], [13] is that the second high-frequency stage can "soft charge/discharge" the energy transfer capacitors in the SC stage, reducing loss and / or required capacitor size in the SC stage. In 1:2 step up conversion mode, the capacitors are soft discharged via the high-frequency second stage, and they are hard charged via the fixed input voltage source; thus in 1:2 conversion mode the SC circuit has a partial soft-charging characteristic. In 2:1 step down conversion mode, a portion (nominally half) of the second stage current (i_{int}) charges one capacitor and the remainder of the current discharges the other capacitor. The two capacitors charge and discharge such that the total voltage across them remains at the input voltage; thus in 2:1 conversion mode the SC circuit entirely operates with a soft-charging characteristic. Because the HF stage charges and discharges the SC stage as a current source (as opposed to high-current impulsive charging), the SC circuit can operate at low switching frequency (and have attendant low switching loss) while attaining low conduction losses. This combines the advantages of the slow and fast switching limits of conventional switched-capacitor converter operation [12], [13], [21], [22]. That is, in the soft-charging mode loss is not limited intrinsically by the capacitance value and change in operating frequency (as in hard charging in a conventional SC circuit), but rather by the I^2R loss associated with the charging current I passing through the total path resistance R (comprising switch resistances and ESR of the capacitors). The SC circuit thus can provide high efficiency and power density even at relatively low operating frequencies and/or with small energy transfer capacitors. The advantage of soft charging and the detailed loss estimation is calculated in the appendix.

The SC circuit serves multiple functions. First, by changing among different conversion modes, it can take a wide-range input voltage (25–200 V) and provide a narrow-range inter-mediate voltage (50–100 V), which is an allowable operating voltage range of the HF regulation stage. That is, an 8:1 input
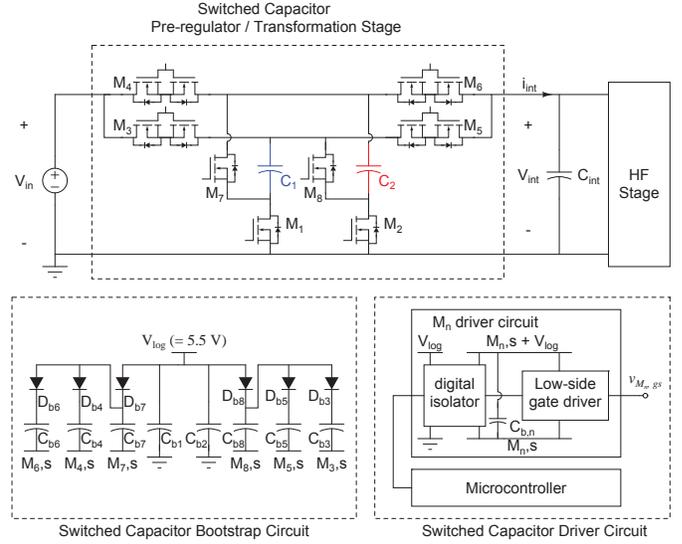

Fig. 5. The switched capacitor circuit comprises transistors, energy transfer capacitors, and bootstrap diodes and capacitors. The switches $M_3 - M_6$ are realized with back-to-back connections of two transistors to block bidirectional voltage. For the control circuitry, the logic power supply V_{log} (= 5.5V) is applied to a set of bootstrap diodes and capacitors to generate appropriate floating supplies for driving the transistors. It should be noted that this bootstrap configuration applies for all conversion modes.

voltage range is reduced to a 2:1 intermediate voltage range. Second, it reduces the peak input voltage for which the HF second stage must operate, lowering device voltage stress. Moreover, the first stage SC circuit improves the impedance levels of the HF stage (i.e., increasing allowable capacitance levels and reducing the required inductance values of the second stage). Lastly, the SC circuit provides a tremendous degree of flexibility to the system. Similar versions of the design can operate either from a very wide 8:1 dc input voltage range (25–200 V) or from a 120 V_{rms} ac-line voltage.

2) SC Stage Control and Driver Circuit:

The SC transformation stage is controlled by the micro-controller, independent of the HF regulation stage operation. The switches of SC stage are controlled to turn on and off by the microcontroller at a fixed frequency with 50% duty ratio. To select the frequency of the SC circuit, two specifications should be considered: the dissipation of SC stage and the intermediate voltage ripple over which the HF stage can operate well. Because of the soft-charging characteristic of the SC stage in our system architecture, the main dissipation at the SC circuit comes from hard-switching of the switches. This loss of the SC stage is thus proportional to the frequency of the SC circuit. The other consideration is the intermediate voltage ripple that the HF regulation stage can tolerate. For a given energy transfer capacitor value in the SC circuit (i.e., C_1, C_2 of Fig. 4), the intermediate voltage ripple increases as the frequency is reduced. Therefore, the frequency should be properly chosen as a compromise between dissipation of the SC stage and intermediate voltage ripple. Our current HF regulation stage topology can tolerate substantial voltage ripple in the intermediate voltage; thus, the SC circuit can be operated at frequencies as low as 20-30 kHz with acceptable
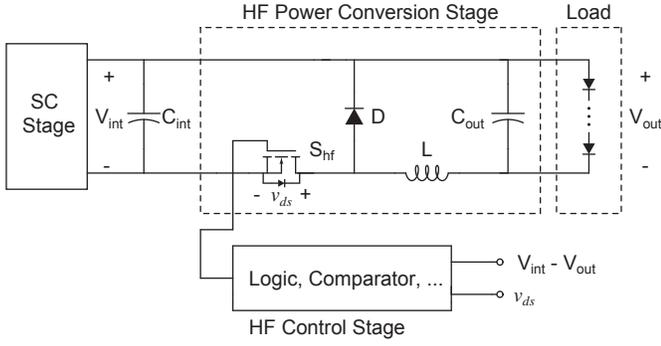
Fig. 6. Schematic of the second magnetic-based regulation stage. This converter stage is designed to operate at high frequency.

capacitor size. An example loss calculation is illustrated with mathematical expressions in the appendix.

The switched capacitor circuit is realized with power transistors ($M_1 - M_8$), bootstrap diodes ($D_{b3} - D_{b8}$), energy transfer capacitors ($C_1 - C_2$), and bootstrap capacitors ($C_{b1} - C_{b8}$) as shown in Fig. 5. It can be seen that the switches M3, M4, M5, and M6 are implemented with a back-to-back connection of two transistors to block bidirectional voltage. For the control circuitry, the logic power supply V_{log} (= 5.5V) powers the switch drivers through a bootstrap driver circuit. Each driver circuit for every switch in the SC circuit was configured with a digital isolator IC, low-side gate driver, and bypass / bootstrap capacitors. The selected digital isolator IC (Adum5240) in our design can be used to generate the floating power supplies (using an internal dc-dc converter) as well as the logic drive signals. However, the dissipation of this converter is unduly high in this application. Thus, to increase the efficiency of the SC control circuit, a separate bootstrap power supply circuit is implemented as illustrated in Fig. 5. The internal power supply in the digital isolator is used to charge the bootstrap capacitors at start-up; after this, the lossy internal power supply capability is disabled and power is provided by the bootstrap circuit. During normal operation the digital isolator IC only operates to shift control signal levels to the flying switch control port.

It should be noted that even in 1:1 conversion mode the bootstrap technique can be achieved by alternatively selecting either the M3&M5 current path or the M4&M6 current path with 50% duty cycle instead of keeping all switches M3, M4, M5, and M6 on continuously. In the bootstrap 1:1 conversion mode, one turns on and off switches in the M3&M5 and M4&M6 paths along with switches M1, M2, M7, and M8 to provide the paths to charge the bootstrap capacitors. The bootstrap configuration shown in Fig. 5 is applicable to all three conversion modes when the switches are controlled as shown in Table II.

C. Second Stage – HF Regulation Circuit

1) HF Regulation Power Stage:

The second stage of our converter, shown in Fig. 6, is a resonant transition discontinuous-mode inverted buck converter operating at frequencies in the vicinity of 5–10 MHz, with ZVS soft-switching over part of its input voltage range, and
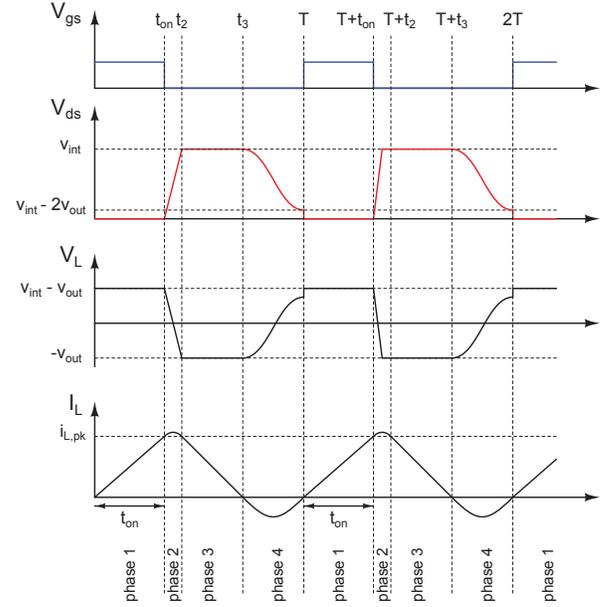

Fig. 7. Operating phases of the high-frequency resonant transition inverted buck converter. The converter achieves zero-voltage switching over most of its range, and low-loss near zero-voltage switching over the remainder of the operating range. Power control is readily achieved by varying the on-state duration of the switch (i.e., t_{on}, the duration of phase 1), and the operating frequency and the duty ratio are indirectly set by this on-state duration.
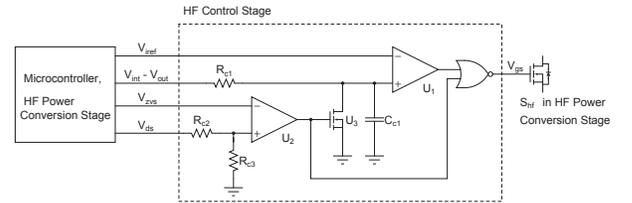

Fig. 8. Schematic of the HF regulation control circuit. This control circuit is designed to regulate the average inductor current by changing the switch on-time, and to operate the HF stage at zero-voltage or near zero-voltage switching conditions. Comparator U_1 triggers the switch turn-off event, and comparator U_2 triggers the switch turn-on event.

near-ZVS soft-switching over the rest of the range. Over the portion of its operating range for which it is soft switched, the converter waveforms are similar to those of the "Quasi-Square-Wave" ZVS buck converter [23], though the control techniques are different. The buck converter is "inverted" in the sense that it is designed with "common positives" so that the active switch is referenced to a constant ground potential and the load has its positive terminal referenced to the positive terminal of the HF stage input voltage. The active switch having its control port referenced to a fixed potential greatly simplifies level shifting of drive signals and mitigates capacitive current injection at the switch gate that would otherwise occur owing to large, fast voltage transitions during switching. Referencing the switch in this way is of great practical importance in achieving extreme high-frequency operation [6], and becomes increasingly important at higher switching voltages where level shifting and capacitive injection affecting switching are major concerns.

The buck converter operation cycles through four phases in a HF switching cycle, as illustrated in Fig. 7. During Phase 1,

the switch is on, and the inductor current i_L ramps up linearly. In Phase 2, the switch turns off, and the switch drain to source voltage v_{ds} rings up to the intermediate voltage (i.e., V_{int}, HF regulation stage input voltage). In Phase 3, the diode starts to conduct and i_L ramps down to zero. In Phase 4, both diode and switch are off, and the inductor rings with the net capacitance at the switch drain node ($C_{sw,d}$, switch output capacitance plus diode output capacitance). Inductor current i_L rings negative and v_{ds} rings down to zero or near zero volts (down to $V_{int} - 2V_{out}$). At this point, the switch is turned back on and the cycle repeats entering phase 1.

Equations (1)–(8) illustrate the inductor current (i_L) and switch drain source voltage (v_{ds}) in each phase, where $Z_d = \sqrt{L/C_{sw,d}}$, $w_d = 1/\sqrt{LC_{sw,d}}$, and $i_{L,pk} = (V_{int} - V_{out})t_{on}/L$, and the nonlinear capacitance variation (relative to voltage bias) is ignored. Equation (9) describes the switching period of the proposed high-frequency buck converter. It can be seen from equation (9) that for a given operating voltage (V_{int}, V_{out}) and parasitic capacitance level ($C_{sw,d}$), a converter with smaller inductance operates over a shorter time period (higher frequency).

Many converters operating from high voltages at low powers (and currents) suffer from large-valued (and consequently large-sized) inductors. A benefit of this topology is that it operates with high inductor current ripple, yielding a relatively small value of inductance and small magnetic energy storage. Moreover, as the system architecture enables a relatively low value of V_{int}, the needed value of inductor L (at a particular switching frequency) is further reduced as per equation (9). Lastly, the soft-switched (or nearly soft-switched) nature of the topology enables relatively high switching frequency (small period) to be achieved at acceptable loss, further reducing the required inductance value. Thus, both the architecture selected and the second-stage topology help minimize the size of the required magnetics.

2) HF Regulation Stage Control and Driver Circuit:

The specific characteristic of the LED load is that the LED load voltage is nonlinear with respect to the load current and is almost determined by the pre-defined LED string forward drop voltage. Therefore, to control output power level, the current

conducting in the LED string load should be adjusted; the fast closed-loop estimated-current control circuit introduced here modulates switch on-time of the HF second stage to adjust the current level. The ability of the controller to provide closed-loop control at the high operating frequency of the system is central to the effectiveness of the proposed approach.

The HF stage control circuit is designed to operate at high frequencies (to beyond 10 MHz) using fast comparators, RC integrators, and logic circuits as illustrated in Fig. 8. The control circuit drives the gate-source voltage v_{gs} of the switch (turning it on and off) as determined by the drain-source voltage v_{ds}, zero-voltage-switching threshold voltage V_{zvs}, cathode node voltage of the LED load (e.g., $V_{int} - V_{out}$), and peak-current threshold voltage V_{iref}; each voltage signal in Fig. 8 is directly connected to one of the HF power conversion stage and microcontroller.

This HF control circuit regulates switching based on two thresholds using a pair of comparators: peak-current threshold voltage (V_{iref}) turn-off with comparator U_1 and ZVS threshold voltage (V_{zvs}) turn-on with comparator U_2. First, comparator U_1 determines the on-time duration of the switch and turns off the switch by comparing V_{iref} and the (approximate) integral of voltage $V_{int} - V_{out}$. When the transistor begins its phase 1 on-state duration, v_{ds} is low, comparator U_2 output is low, and transistor U_3 is off such that the voltage on C_{c1} approximately integrates voltage $V_{int} - V_{out}$. After the capacitor C_{c1} is charged for a short duration Δt, $V_{U_1,+} = (V_{int} - V_{out})\Delta t/(C_{c1}R_{c1})$. The output of U_1 goes high and turns off the switch (v_{gs} low) when $V_{U_1,+}$ becomes larger than V_{iref} (i.e., $t_{on} = V_{iref}C_{c1}R_{c1}/(V_{int} - V_{out})$). Because the proposed high-frequency regulation stage is always operating at the edge of discontinuous conduction mode, as shown in equation (1) the inductor current i_L during the switch is on-state (phase 1) is as follows:

$$i_L = \frac{V_{int} - V_{out}}{L} \Delta t \tag{10}$$

$$i_{L,pk} = \frac{V_{int} - V_{out}}{L} t_{on} = \frac{V_{iref}C_{c1}R_{c1}}{L} \tag{11}$$

Thus, the voltage V_{iref} directly modulates the switch turn-on time to regulate peak current of the inductor, regardless of

$$i_L(t) = \begin{cases} \dfrac{V_{int} - V_{out}}{L}t & 0 \le t \le t_{on},\ phase1 \quad (1) \\[2mm] i_L|_{t=t_{on}}\cos(w_d(t - t_{on})) + \dfrac{V_{int} - V_{out}}{Z_d}\sin(w_d(t - t_{on})) \approx i_L|_{t=t_{on}}\cos(w_d(t - t_{on})) & t_{on} \le t \le t_2,\ phase2 \quad (2) \\[2mm] i_L|_{t=t_2} - \dfrac{V_{out}}{L}(t - t_2) & t_2 \le t \le t_3,\ phase3 \quad (3) \\[2mm] -\dfrac{V_{out}}{Z_d}\sin(w_d(t - t_3)) & t_3 \le t \le T,\ phase4 \quad (4) \end{cases}$$

$$v_{ds}(t) = \begin{cases} 0 & 0 \le t \le t_{on},\ phase1 \quad (5) \\[2mm] Z_d i_L|_{t=t_{on}}\sin(w_d(t - t_{on})) + (V_{int} - V_{out})(1 - \cos(w_d(t - t_{on}))) \approx Z_d i_L|_{t=t_{on}}\sin(w_d(t - t_{on})) & t_{on} \le t \le t_2,\ phase2 \quad (6) \\[2mm] V_{int} & t_2 \le t \le t_3,\ phase3 \quad (7) \\[2mm] V_{int} - V_{out} + V_{out}\cos(w_d(t - t_3)) & t_3 \le t \le T,\ phase4 \quad (8) \end{cases}$$

$$T = \frac{Li_{L,pk}}{V_{int} - V_{out}} + \frac{C_{sw,d}V_{int}}{i_{L,pk}} + \frac{Li_{L,pk}}{V_{out}} + \frac{\pi}{w_d} \approx \frac{Li_{L,pk}}{V_{int} - V_{out}} + \frac{Li_{L,pk}}{V_{out}} + \sqrt{LC_{sw,d}}\pi \tag{9}$$
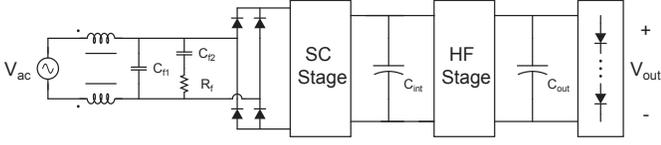
Fig. 9. The ac-input configuration of the proposed architecture includes a filter and full-bridge rectifier. Twice-line-frequency energy buffering is realized with a capacitance C_{out} placed across the system output.

the high-frequency regulation stage input voltage (V_{int}) and output voltage (V_{out}).

The turn on of the switch (ending phase 4 and starting phase 1) is determined by comparator U_2. After the switch turns off at the end of phase 1, the resistor-divided v_{ds} voltage goes above V_{zvs}, and transistor U_3 turns on. This discharges the voltage on C_{c1}, resetting the past-integrated C_{c1} voltage for controlling on-time duration in the next cycle and making the output of U_1 low. When the inductor current decreases down to zero at the end of phase 3 and the HF-stage diode turns off, phase 4 begins and the inductor starts to ring with the net capacitance at the switch drain node (That is, the switch drain-source voltage starts to ring down). When switch drain-source voltage v_{ds} rings down sufficiently, the resistor-divided v_{ds} voltage goes below V_{zvs}, and the output of U_2 goes low. The control circuit then turns on the switch again, and the cycle repeats. V_{zvs} is set such that – including logic delays – the switch is turned on at the correct point in the drain-voltage ringdown.

D. DC configuration

In a dc-dc configuration, the converter operates at wide input voltage range (i.e., 25–200 V). The switched capacitor stage changes the conversion mode as the input voltage varies and reduces the intermediate voltage range as shown in Fig. 2. The high frequency regulation stage then efficiently converts from the reduced-range intermediate voltage to the load voltage at a particular power level.

E. AC configuration

In an ac-dc configuration, the converter includes line frequency filter and full-bridge rectifier as shown in Fig. 9. The twice-line-frequency energy buffering for single-phase ac to dc conversion is realized with capacitance placed across the system output voltage. In an ac-dc converter high power factor is desired in addition to high efficiency and high power density. In commercial LED driver applications a power factor of at least 0.9 is desired, while in residential applications a power factor of 0.7 is acceptable. To attain high power factor, the input current waveform from the ac-line voltage should be proportional to the sinusoidal voltage waveform. In cases where the voltage waveform is sinusoidal and the current waveform is "clipped" to zero for low voltages (e.g., where the converter ceases to draw input current near ac-line zero voltage crossings), the current waveform providing the highest power factor is a "clipped" sine wave in phase with the voltage, as illustrated in Fig. 10. For a "cut in" voltage of
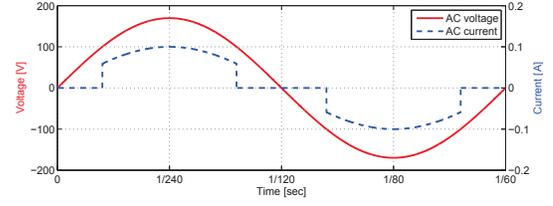

Fig. 10. Waveform of the sinusoidal ac voltage and a "clipped sine wave" ac current. The clipped-sinewave current pattern operating over a 108 degree range for each 180 degree half-cycle yields a power factor of 0.95 (this corresponds to a 100 V "cut in" voltage for a 170 V peak sinusoidal voltage). Operating over a 120 degree range per half-cycle yields a power factor of 0.97.
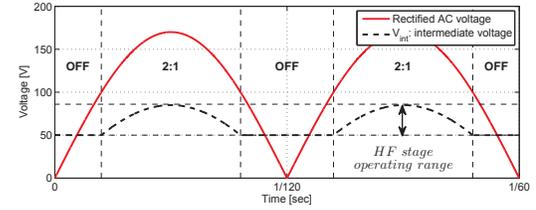

Fig. 11. The voltage transformation characteristic of the switched-capacitor (first) stage over the line cycle in an ac-dc converter. Note that both the SC stage and HF stage are turned off below 100 V input voltage, and the intermediate voltage (V_{int}) remains at 50 V during this off duration.

100 V (for a 170 V peak sinusoid), a power factor of > 0.95 is realized with a clipped sinusoid current waveform.

The proposed ac-dc converter is designed to approximately draw the current pattern of Fig. 10, with a "cut in" voltage of 100 V. Both the SC first stage and HF second stage are turned off below 100 V voltage range, and the load is buffered by output capacitor during this off period. It should be noted that, as shown in Fig. 11, the SC stage operates in the 2:1 conversion mode when the ac input voltage is above 100V and is in the off-state during the rest of the cycle. The intermediate voltage (i.e., the voltage which HF regulation stage operates) remains at 50 V during this off duration because both stages are turned off. The HF regulation stage thus operates with an intermediate voltage between 50 V and 85 V in this ac-dc case.

When the rectified ac voltage is above 100 V, the merged two-stage circuit is controlled to yield an input current that approximates a clipped-sinusoidal waveform. The filtered input current is proportional to inductor peak current $i_{L,pk}$ of the HF regulation stage, which can be directly changed by peak-current threshold voltage (V_{iref}) of the HF control circuit as described above. At low voltages, the converter is turned off by setting V_{iref} to 0, and when the rectified ac voltage goes above 100V, the V_{iref} peak-current threshold voltage is adjusted to be proportional to the rectified ac voltage by the microcontroller; the approximate clipped-sinusoidal input current then flows from the ac line voltage.

In the prototype converter, the ac-dc converter cuts in at 100 V (for a 170 V peak sinusoid) and ideally achieves 0.95 power factor. In LED driver applications, power factors exceeding 0.9 are not currently demanded in the market, so this operation mode is sufficient to provide the desired

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TABLE IV
COMPONENTS OF THE SC STAGE AND HF STAGE

SC power stage		
C_1, C_2	energy transfer capacitor	$1\mu F$, Ceramic 100V
$M_1 - M_8$	switch	EPC2012, GaN 200V 3A HEMT FET
$C_{b1} - C_{b8}$	bootstrap capacitor	$1\mu F$, Ceramic 16V
$D_{b3} - D_{b8}$	bootstrap diode	DFLS1150, Diodes Inc. 150V 1A Schottky
C_{int}	bypass capacitor	$2\times 10nF$, Ceramic 100V
SC stage control / driver circuit		
isolator / *iso*Power		ADum5240, Analog Devices
low-side gate driver		FAN3111C, Fairchild
HF power stage		
L	inductor	$2\times 422nH$, Coilcraft, Maxi Spring Air core
D	diode	STPS10170C, ST 170V 10A Schottky
S_{hf}	switch	EPC2012, EPC, GaN 200V 3A HEMT FET
C_{out}	output capacitor	DC Configuration $\qquad$ $10\mu F$, Ceramic 50V
		AC Configuration $\qquad$ $10\mu F$, Ceramic 50V
		$820\mu F$, Aluminum 50V
HF stage control / driver circuit		
U_1, U_2	comparator	LT1711, Linear Technology, rail-to-rail comparator
U_3	inverter	SN74LVC2G06, Texas Instrument, Inverter with open-drain outputs
R_{c1}	resistor	$100k\Omega$
R_{c2}	resistor	$200k\Omega$
R_{c3}	resistor	$10.5k\Omega$
C_{c1}	capacitor	$10pF$, Ceramic 50V
low-side gate driver		NC7SZ02, Fairchild, Tiny Logic Two-input NOR gate
Bridge rectifier and input filter for AC configuration		
Bridge rectifier		MB6S, Vishay
Common mode choke		1mH PM3700-40-RC, Bourns
C_{f1}	capacitor	$22\ pF$, Ceramic X1Y2 $250V_{ac}$
C_{f2}	capacitor	$220\ pF$, Ceramic X1Y2 $250V_{ac}$
R_f	resistor	$442\ \Omega$
Microcontroller		ATMEGA64M1, Atmel

performance. However, in applications for which higher power factor than 0.95 is required, the current conduction duration of the converter can be increased by cutting in at a lower voltage (e.g., 25 V for a 170 V peak sinusoid). To operate in this wide range, the SC stage then can changes the conversion modes among 1:2, 1:1, and 2:1 ratios (like the variable-topology SC circuit in dc-dc converter as shown in Fig. 2) and sets the intermediate voltage between 50 V and 100 V. It should be noted that the same two-stage architecture can be applied for universal ac line voltage, but the appropriate voltage rate components and a higher step-down conversion ratio HF regulation stage are necessary.

IV. EXPERIMENTAL RESULTS

Two implementations of the proposed converter have been developed. One operates from a wide-range dc input voltage (25-200 V dc), while the second operates with a front-end filter and full-bridge diode rectifier from 120 V_{rms} ac line voltage. The components and parameters chosen for the dc-dc converter and ac-dc converter implementations are listed in Table IV. Some additional auxiliary bypass capacitors, resistors, and protection diodes are used to connect the converter circuit to the logic voltage and the microcontroller.

In the HF regulation stage, ZVS soft-switching condition is necessary to achieve high efficiency. Fig. 12 shows a experimental measurement of switch gate voltage v_{gs} and switch drain voltage v_{ds} of the HF stage in the merged two-

stage converter, operating at a 60 V dc input voltage and a 35 V and 12.15 W load. The measured waveform illustrates high-frequency operation of the proposed HF regulation stage with ZVS soft-switching (i.e., the HF regulation stage operates at 7.8 MHz at this input voltage and power level. The switching frequency is changed and determined by the input voltage and power level, and the converter operates in high-frequency (3–30 MHz) region with ZVS (or near ZVS) condition).

Moreover, as previously discussed, soft-charging of capacitors is desired to boost the efficiency of the SC transformation stage. When the SC circuit operates in 2:1 step-down mode, it is fully soft-charged, and energy transfer capacitors charge and discharge based on current from the regulation stage. Fig. 13 shows the drain-source voltage (v_{ds}) of the HF regulation stage and the intermediate voltage (v_{int}) between SC transformation stage and HF regulation stage, when the converter operates from 165 V dc voltage. As can be seen, the intermediate voltage slowly discharges during each SC state, illustrating soft charging of the SC (first) stage by the HF (second) stage (merged two-stage operation). In the 1:2 mode, there is a mixture of soft- and hard-charging of the capacitors.

The microcontroller, SC stage and HF stage control circuit, and linear regulators are supplied by an external 5.5V power supply and dissipate about 0.6 W. The control circuit of the SC stage operates at 50 kHz frequency and uses about 0.3 W power to drive 8 level shifters and 8 low-side gate drivers. The HF control circuit operates in the 3-30 MHz frequency and
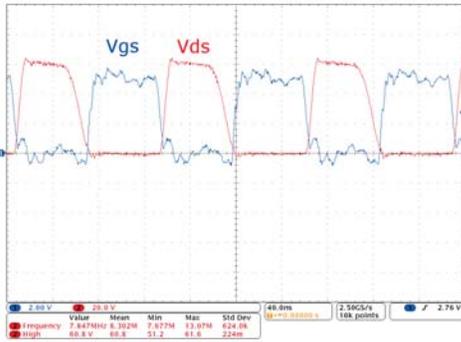
Fig. 12. Experimental v_{gs} and v_{ds} waveforms showing zero-voltage switching of the HF regulation stage (x: 40ns/div, y–v_{gs}: 2V/div, y–v_{ds}: 20V/div). The HF stage input voltage is 60 V and the output is a 35 V, 12.15 W load. The converter operates at 7.85 MHz under this condition.
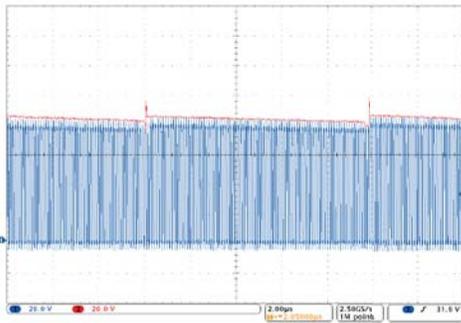

Fig. 13. The implemented dc-dc converter is connected to 165 V dc voltage, where the SC circuit operates in 2:1 step down conversion mode. Ch1 (blue, y: 20V/div) shows the measured switch drain-source voltage v_{ds} of the HF regulation stage, and Ch2 (red, y:20V/div) is the intermediate voltage (V_{int}) between SC transformation stage and HF regulation stage. It should be noted that the droop of intermediate voltage during each SC state shows the soft-charging characteristic of the SC (first) stage by the HF (second) stage (merged two-stage operation).

consumes about 0.2 W power. The small gate capacitance of the GaN transistor ($\sim$120 pF) requires only a small amount of energy even for high-frequency operation, but two high-speed (low propagation delay) comparators (LT1711) in the HF control circuit need significant supply current and dominate the loss of the HF control circuit. (It is noted that the authors have implemented and tested low-loss comparators for this application, but this is beyond the scope of this paper.) The loss of control circuits are not optimized in this prototype design and thus are excluded from efficiency calculations.

Measurements of the dc-dc converter power stage efficiency (i.e., excepting control and driver circuit losses) for various power and input voltage levels are shown in Fig. 14. It can be seen that the converter has a peak power stage efficiency of 96% with V_{in} = 50 V, V_{out} = 35 V, at an output power of 30 W. In Fig. 14, the efficiency waveform can be divided to three regions across the input voltage, 25–50 V, 50–100 V, and 100–200 V. In each region, the efficiency decreases at higher input voltage because the HF regulation stage starts to operate at near-ZVS instead of ZVS as the intermediate voltage goes higher than $2V_{out}$. However, the SC circuit changes conversion mode as the input voltage crosses 50 V and 100 V, and again
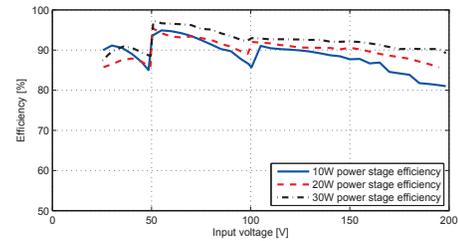

Fig. 14. Power stage efficiency of the merged two-stage converter prototype dc-dc converter configured to operate from a wide-range dc input of 25-200 V. Power stage efficiency is shown for three output power levels (10 W, 20 W, and 30 W) across the input voltage range.
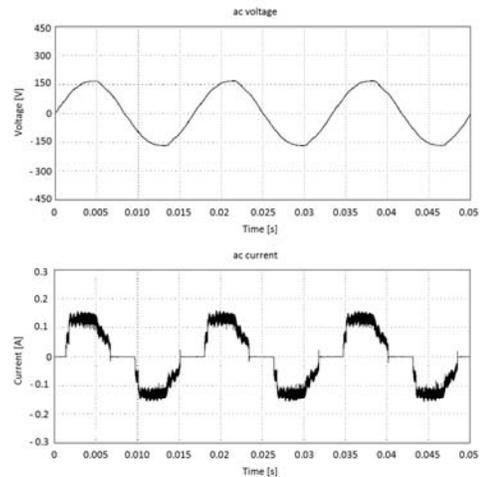

Fig. 15. Experimental input voltage and current of prototype ac-input merged two-stage converter operated from the ac line(x: 5ms/div (top): 150V/div, (bottom): 100mA/div). The prototype achieves a power stage efficiency of 88% and a 0.93 power factor using only commercially-available devices and components. Operation is shown for 35 V output at 8.4 W load power.
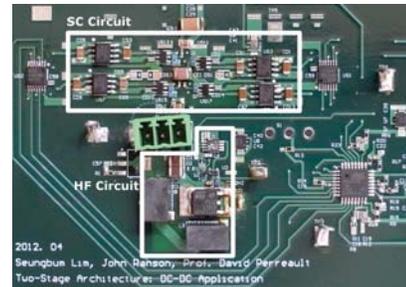

Fig. 16. Experimental prototype of dc-dc converter was designed on 3.5 in × 2.5 in PCB board. The switched-capacitor stage and HF regulation stage are outlined. It can be seen that the PCB is not optimized, and that much of the board area used is dominated by the control circuitry; circuit size can be dramatically reduced both by optimization and by use of more highly integrated control circuits.

sets the intermediate voltage to the desired operating range such that the HF regulation stage can operate more efficiently. Thus, as can be seen in Fig. 14, the efficiency makes discrete transitions when the input voltage crosses 50 V and 100 V, and owing to the mode changes the system maintains high efficiency across a wide input voltage range.

The ac-dc implementation including a bridge rectifier and

TABLE V
THE SPECIFICATION OF IMPLEMENTED PROTOTYPE CONVERTER

	dc-dc	ac-dc
output power	up to 30 W	8.4W
SC stage switching frequency	50 kHz	50 kHz
HF stage switching frequency	varying in 3-30MHz (HF region)	varying in 3-30MHz (HF region)
Efficiency	up to 96%	88.3%
Power Factor		0.93
Expected Power density (after opt.)	$> 60\ W/in^3$	$> 10\ W/in^3$

input filter was measured from a 120 V_{rms} 60 Hz ac line voltage. Fig. 15 shows the experimental input voltage and current waveforms, and it operates at 88.3% efficiency and 0.93 power factor for an 8.4 W load. It should be noted that for the ac-dc converter a relatively large electrolytic capacitor is required to buffer the twice-line-frequency energy if there is to be no flicker in the output; this is a disadvantage of the proposed architecture in ac-dc applications.

Fig. 16 shows a photograph of the dc-dc converter implementation with the SC transformation stage and HF regulation stage outlined. The experimental prototype was designed on a 3.5 in × 2.5 in PCB, and as can be seen the layout of PCB is not optimized and is dominated by the control circuitry. The required size could be dramatically reduced by layout optimization and by use of greater IC integration of the control circuits. We roughly calculated the volume of the converter after the optimization, and for the dc-dc converter 0.5 in^3 and for the ac-dc converter (without input filter and bridge rectifier) 0.8 in^3 volume are expected. Table V summarizes the measurement results.

V. Conclusion

A merged two-stage power conversion architecture and associated circuit topology and its application to LED driver circuits are demonstrated. This approach is specifically designed to address the challenges of low-power conversion from high and wide-range input voltages. A soft-charged multi-mode SC converter stage is introduced that provides compression of an 8:1 input range to a 2:1 output range. Depending on operating mode, this topology provides partial or complete soft charging of the capacitors appropriate load. We detail operation of this reconfigurable transformation stage and also introduce appropriate drive and bootstrap techniques for it. We further show that merging this stage with a resonant transition discontinuous-mode inverted buck converter enables conversion from a high, wide-range input voltage down to a low output voltage at greatly increased operating frequencies, and consequently greatly reduced magnetics size. The pairing and merging of these two stages enables increases in switching frequency of up to an order of magnitude over what is commonly achievable. The proposed power converter can be used in both dc-dc and ac-dc applications with low device stress, high efficiency, high power density, and high power factor.

The experimental prototypes of both a dc-dc and an ac-dc converter using this architecture are implemented for LED driver applications and presented along with experimental results. Through appropriate control and merged operation between the SC transformation and HF regulation stages, soft-charging of the SC stage and ZVS switching of the HF stage are achieved. Additionally, this proposed architecture and topological approach are likewise expected to be applicable to not only this LED driver circuit but also a variety of electrical applications which have wide-range dc input voltage or ac line input voltage.

Appendix

In this appendix we explore the dissipation and the intermediate voltage (V_{int}) fluctuation of the switched capacitor circuit, and illustrate how to choose a desired operating frequency of the switched capacitor circuit as a compromise among several considerations.

A. Dissipation of the Switched Capacitor Circuit

The dissipation of the switched capacitor circuit comes from two primary sources: energy transfer capacitor charge / discharge loss and switch output capacitor charge / discharge loss (we neglect gating loss, as this is a modest consideration here.)

The dissipation during charging and discharging the energy transfer capacitors can be calculated and estimated with a Thevenin model of the SC circuit [22]. In the Thevenin model, the output resistance represents the loss, and it changes with the operating frequency and capacitance level in the switched capacitor circuit. In the model of SC circuit with hard-charging operation, the output resistance can be plotted across the switching frequency with two asymptotes, the slow-switching-limit (SSL) and the fast-switching-limit (FSL), respectively. For instance, in our proposed 2:1 SC configuration, the effective SC stage Thevenin output resistance can be calculated as $1/(8Cf_{sw})$ in SSL and $3R_{sw,on}$ in FSL. Fig. 17 shows the output resistance of the hard-charging SC circuit across the frequency with different capacitance levels. To decrease this output resistance, the switched capacitor circuit can be operated with either larger capacitance or higher operating frequency, which consumes either more area or more loss from charging and discharging non-zero switch output capacitances (the second source of SC circuit dissipation described below).

Compared to hard-charging operation, soft charging operation adiabatically charges and discharges the energy transfer capacitors via the regulation stage, which allows it to operate at the FSL dissipation levels with small capacitance and low operating frequency. Fig. 17 also shows the output resistance of the proposed SC circuit with 2:1 conversion mode and soft-charging operation. With the output resistance of the Thevenin model, the first source of dissipated power in the 2:1 conversion mode of the SC circuit can be calculated as follows:

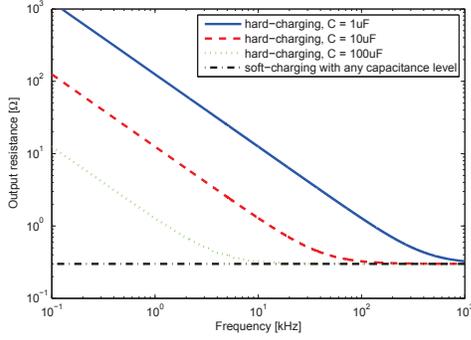$$P_{SC-diss,1} = i_{int}^2 R_{out} = \left(\frac{i_{in}}{2}\right)^2 3R_{sw,on} \qquad (12)$$

Fig. 17. The output resistance in the Thevenin model of the SC circuit represents loss from charging/discharging energy transfer capacitors, and it changes with SC configuration, capacitance level, operating frequency, and SC operation (hard-charging or soft charging). In this example, the output resistance of the proposed 2:1 SC configuration was calculated at several capacitance levels. The circuit was assumed to operate at 150 V input voltage and 30 W power level.

The second source of the loss in the SC circuit comes from the non-zero output capacitance across each switch. These output capacitances charge or discharge during every state change. For example, in 2:1 SC configuration, two switches M_7 and M_8 block V_{in} and the other switches (M_1-M_6) block $V_{in}/2$, causing dissipation as follows:

$$P_{SC-diss,2} = C_{oss}\left(2V_{in}^2 + 6\left(V_{in}/2\right)^2\right) f_{sw} \qquad (13)$$
$$= 3.5\, C_{oss}V_{in}^2\, f_{sw} \qquad (14)$$

(In the equivalent model of the SC circuit, this loss could be captured by a shunt resistor across the converter input port of value $R_{eq} = 1/(3.5C_{oss}f_{sw})$.) It should be noted that while this loss can be minuscule in a low-voltage SC circuit, in a high voltage SC circuit this loss becomes significant.

Overall, the total dissipation can be calculated by adding the two sources of loss components. Fig. 18 shows the estimated total dissipation across the operating frequency when the proposed 2:1 conversion mode SC circuit operates at 150 V dc input voltage and 30 W power level. In this example, we supposed 0.1 Ω switch on-resistance ($R_{sw,on}$) and 100 pF switch output capacitance (C_{oss}) referencing the EPC 2012 characteristic. As can be seen in Fig. 18, soft-charging is always better for higher efficiency and higher power density compared to hard-charging operation. It should be noted that at this power, operating voltage, and soft-charging operation, the loss component from switch output capacitance is a dominant factor, and it is proportional to the SC operating frequency.

B. V_{int} voltage fluctuation of the switched capacitor circuit

The essence of the soft-charging characteristic in SC circuit is to allow voltage fluctuation at the intermediate voltage, and adiabatically charge / discharge of energy transfer capacitors with a following regulation converter. The fluctuating intermediate voltage should reside in the operating range of the following HF regulation stage. The voltage fluctuation can be easily calculated at a particular power level, and here are
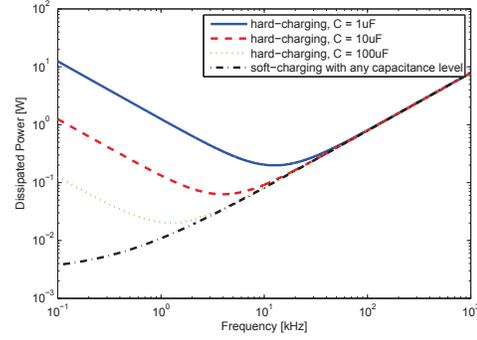

Fig. 18. The total dissipation of the proposed 2:1 conversion mode SC circuit is plotted across SC stage switching frequency. The SC circuit is assumed to be operating at 150 V dc input voltage and 30 W power level. Soft-charging operation is always better for higher efficiency and higher power density compared to hard-charging operation. In soft-charging operation at this operating voltage and power level, the loss at our design frequency mainly comes from charging / discharging the non-zero switch output capacitance, and it is thus proportional to the operating frequency. The main limit to how low the switching frequency may be set in soft-charging operation is the allowable voltage ripple at the SC stage output.
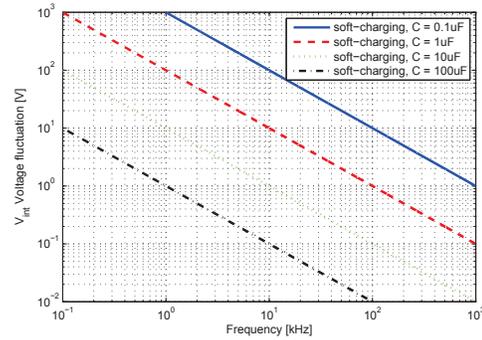

Fig. 19. Soft-charging operation in SC circuit causes ripple on intermediate voltage (V_{int}), the voltage between the SC stage and the following HF regulation stage. The intermediate voltage ripple changes with the energy transfer capacitor value, operating frequency, and power level. In this figure the V_{int} voltage fluctuation was plotted when the SC circuit is operated at 150 V dc input voltage and 30W power level with 2:1 conversion mode.

example equations for the proposed 2:1 configuration case:

$$\Delta Q_C = \frac{i_{int}}{2}t = \frac{i_{int}}{2}\frac{1}{2f_{sw}} = \frac{i_{int}}{4f_{sw}} = C\Delta V_{int} \qquad (15)$$

$$\Delta V_{int} = \frac{i_{int}}{4Cf_{sw}} = \frac{P_{out}}{4Cf_{sw}V_{int}} \approx \frac{P_{out}}{2C_1 f_{sw}V_{in}} \qquad (16)$$

The V_{int} voltage fluctuation is plotted across frequency as shown in Fig. 19, supposing 150 V input voltage and 30 W power level. As can be seen, the V_{int} voltage shows less voltage ripple at higher capacitance and higher operating frequency.

As illustrated above, the dissipation and intermediate voltage (V_{int}) fluctuation of the switched capacitor circuit are closely related to the switching frequency, capacitance level, and type of SC operation (hard charging or soft charging). It is thus essential to select a desired operating frequency compromising these trade-offs. Considering several characteristics at three different conversion modes simultaneously, the

proposed SC circuit was designed with $1\mu F$ energy transfer capacitors and operated with soft-charging characteristic at 50 kHz frequency. It should be noted that if wide output power range operation are desired, one might choose to also modulate the SC converter frequency with output power.

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