

A High-Power-Density Wide-Input-Voltage-Range Isolated dc-dc Converter having a MultiTrack Architecture

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Abstract—This paper proposes a *MultiTrack* power conversion architecture that represents a new way of combining switched-capacitor circuits and magnetics. The *MultiTrack* architecture reduces the voltage ratings on devices, reduces the voltage regulation stress of the system, improves the component utilization, and reduces the sizes of passive components. This architecture is suitable for power conversion applications that require both isolation and wide voltage conversion range. An 18 V to 80 V input, 5 V, 15 A output, 800 kHz, 0.93 inch² (1/16 brick equivalent) isolated dc-dc converter has been built and tested to verify the effectiveness of this architecture. By utilizing GaN switches, operating at higher frequency, and employing the *MultiTrack* architecture, the prototype converter achieves a power density of 457.3 W/inch³ and a peak efficiency of 91.3%. This power density is 3x higher than the power density of the state-of-the-art commercial converters with comparable efficiency performance across the wide operation range.

I. INTRODUCTION

POWER electronic designs have generally been cost driven. Simple circuit topologies with low complexity, low component count, and simple controls have traditionally been preferred in practical designs. However, with increasing electronic content in industrial and consumer applications, and wider deployment of renewable energy systems, power electronics is required to have much higher performance. At the same time, the relative cost of power devices and control circuitry has fallen (following the general trend in the semiconductor industry). Hence, enhancing system performance through more sophisticated circuit architectures is an attractive option and presents many emerging design opportunities [1].

Power conversion systems can generally be grouped into single-stage architectures and multi-stage architectures. In a single-stage architecture, multiple tasks (e.g., output voltage modulation, input current shaping) are realized in a single power stage. They have low circuit complexity and simple control, but cannot achieve high performance while meeting requirements such as wide operating ranges and high power density. Multi-stage architectures have multiple power conversion stages with each stage performing one or more functions. Each stage can be optimally designed to only address a portion of the system requirements. As a result, the overall system performance is often better, while the total component count and complexity is usually higher. In many cases, a multi-stage

architecture may process the full system energy multiple times, imposing a penalty on efficiency.

Switched-inductor circuits, switched-capacitor circuits and magnetic isolation circuits are often used as the basic building blocks of multi-stage systems [1]–[12]. They have complementary advantages and limitations. Switched-inductor circuits are popular for their voltage regulation capability. However, basic switched-inductor circuits suffer in terms of size and performance at high voltage conversion ratios, and their power density is typically limited by the bulky power stage magnetics. Switched-capacitor circuits, by contrast, can provide balanced efficiency and power density tradeoffs for fixed voltage conversion ratios, but can not efficiently regulate voltage and have limited voltage conversion ratio options with reasonable component count. Magnetic isolation circuits, i.e., isolated converters with fixed voltage conversion ratio (“dc transformers”) can provide high voltage conversion ratio, galvanic isolation and soft-switching. However, they often do not maintain high performance across wide operation range.

There has been significant recent work in hybridizing switched-capacitor and magnetic conversion, with consequent advantages. Building or merging multi-stage systems incorporating switched-capacitor circuits, switched-inductor circuits and magnetically-coupled circuits (e.g., “dc transformers”) has been one fruitful approach. A switched-capacitor voltage divider and a multi-phase buck converter were cascaded to implement a high performance laptop power supply in [4]. The wide-input-range converter presented in [5] likewise incorporated a switched-capacitor circuit with a switched-inductor circuit in a manner to best leverage their benefits in low-voltage CMOS. Clever usage of switched-capacitor and magnetic stages has been demonstrated in multi-output converter systems [6]. Integrated techniques have been applied with switched-capacitor converters at higher voltages: an on-chip switched-capacitor converter was combined with capacitive isolation circuits and magnetics as the dc-dc portion of a LED driver in [7].

More highly coupled use of switched capacitors and magnetics has also been exploited to advantage. For example, in [8], [9], it was shown that significant system benefits can be obtained by merging the operation of the magnetic and switched-capacitor stages through “soft charging” of the capacitor elements, enabling one or both of higher efficiency and smaller capacitor size. A few high-performance

high-frequency grid-interfaced LED drivers using merged circuit architectures were presented in [10]–[12]. Resonant switched-capacitor circuits and other “merged” switched-capacitor/magnetics techniques have also proven advantageous [13]–[15]. By adding one or more inductive components into the switched-capacitor circuit structure, enhanced performance with reasonable regulation capability and/or minimization of passive component size can be achieved.

In this paper, we propose a MultiTrack power conversion architecture that represents a new way of combining switched-capacitor and magnetic circuit elements. It incorporates a *hybrid switched-capacitor/magnetics* circuit structure that splits the wide voltage conversion range into multiple smaller ranges, delivers power in multiple tracks, and functionally merges the regulation stage and the isolation stage. The system operates in multiple operation modes across the wide input voltage range, with its performance optimized for each sub-division of the input voltage range. Compared to conventional two-stage designs, it gains advantages through distributed parallel power processing, rather than multiple full power processing, and facilitates reduced device ratings, reduced magnetics size, improved component utilization, and reduced drive of parasitic transformer capacitances. It also enables zero-voltage-switching (ZVS) (or near ZVS) of the transistors used in charge transfer among capacitors, which is not available in a traditional switched-capacitor circuit or a merged two-stage converter, without additional elements. The proposed approach embraces trends in the development of semiconductor devices, and is suitable for power converter designs operating at high frequencies (close to MHz or higher).

The remainder of this paper is organized as follows: Section II provides an overview of the MultiTrack power conversion architecture. A basic 2-Track implementation and its operation is introduced in Section III. The 2-Track architecture is extended to a generalized MultiTrack architecture in Section IV. Analysis and discussion about the advantages of the MultiTrack architecture are provided in Section V. Section VI presents several practical design considerations. Experimental and benchmark results are provided in Section VII. And Section VIII concludes the paper.

II. ARCHITECTURE OVERVIEW

Fig. 1 shows the block diagram of the proposed MultiTrack power conversion architecture. It comprises two merged conversion stages that provide the functional benefits of a switched-inductor circuit (for regulation), a switched-capacitor circuit (for distributing voltage stress among different levels and providing voltage balancing), and a magnetic isolation circuit (for transformation and galvanic isolation). While the circuit subsystems are actually merged, one can consider the desired functions independently. The switched-inductor portion of the circuit is principally responsible for voltage regulation; the magnetic isolation portion of the circuit offers isolation and voltage scaling (and - in some cases - a secondary means of voltage regulation); and the switched-capacitor circuit creates multiple related voltage levels (V_1 , V_2 , V_3 , etc.) and many stacked current tracks that bridge the other two subsystems.

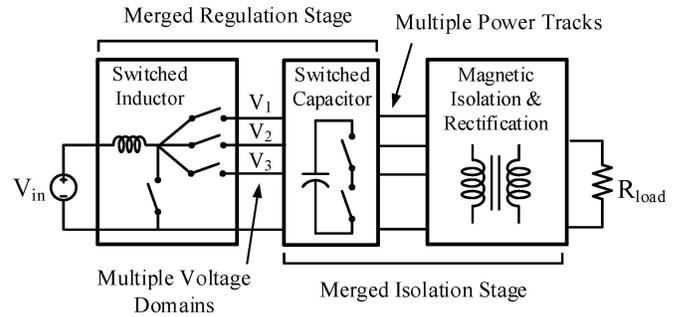


Fig. 1. The proposed MultiTrack power conversion architecture comprising multiple voltage domains and multiple power tracks. Its regulation and isolation stages are merged, hence reducing the amount of power that is “re-processed” by the two-stages.

One advantage of the Multitrack converter is that components of the subsystems are shared, and their functions are partially merged. The switched-inductor circuit block couples into the multiple levels of the switched-capacitor circuit to form a *merged regulation stage*. Likewise, by using a single set of switches to perform charge transfer and voltage balancing among different levels of the capacitor stack, and to drive the parallel-track magnetic isolation device, we obtain a *merged isolation stage*.

Merging the stages in this manner yields a circuit having improved performance as compared to what could be achieved with separate stages. In conventional wide input voltage dc-dc converter designs, there is usually a regulation stage (typically a buck or boost converter) that compresses the variable input voltage to a fixed intermediate bus voltage. This intermediate bus voltage is then processed by a separate isolation stage. Since the regulation stage has to be designed for the worst case (peak input voltage and peak input current), the voltage or current ratings of these components are usually not well utilized: when the voltage is high, the current is usually low; when the voltage is low, the current is usually high.

The proposed MultiTrack architecture improves the component utilization through a hybrid switched-capacitor/magnetics circuit structure. Multiple voltage domains with multiple ratiometrically-related intermediate bus voltages (V_1 , V_2 , V_3 , etc.) are synthesized using a ladder switched-capacitor circuit structure which also simultaneously acts to drive the isolation stage magnetics. This reduces the number of switches required and provides ZVS opportunities for the switches. Depending on the input voltage, the switched inductor circuit redistributes the regulation stage inductor current into the closest intermediate bus voltages, thus effectively reduces the voltage drop across the inductor, and reduces the stress on switches (as will be discussed in Section V).

III. A BASIC 2-TRACK EMBODIMENT

A 2-to-1 input voltage range 2-track converter as shown in Fig. 2 is a simple implementation of the MultiTrack architecture. This 2-track converter has two related intermediate bus voltages (V_X and $2V_X$) and has a 2-to-1 input voltage range between V_X and $2V_X$. The relative values of bus voltages V_X and $2V_X$ are synthesized by a 2:1 ladder switched capacitor

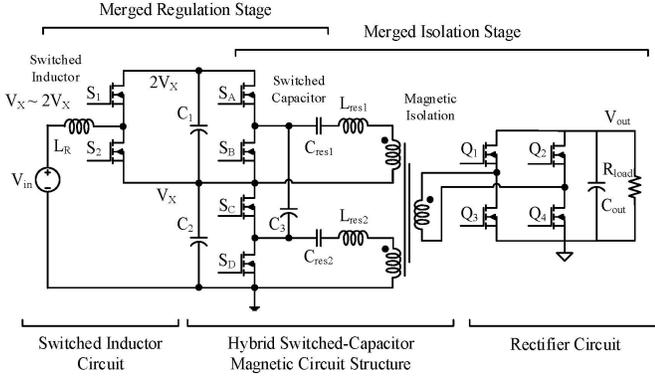


Fig. 2. Schematic of an example 2-to-1 input voltage range 2-Track converter comprising a switched-inductor circuit, a switched-capacitor circuit and a magnetic isolation circuit. The regulation stage and the isolation stage are merged by a *hybrid switched-capacitor-magnetic* circuit structure.

circuit structure, whose switches are also used as the inverter switches in the isolation stage.

We first introduce the merged isolation stage. The merged isolation stage includes a pair of half bridges (S_A/S_B and S_C/S_D) that operate synchronously to drive a pair of identical resonant tanks ($C_{res1}-L_{res1}$ and $C_{res2}-L_{res2}$). These are coupled to a *multiple-input-single-output* (MISO) transformer (whose leakage inductances form L_{res1} , L_{res2}), with the output tied to a synchronous full-bridge rectifier (Q_1-Q_4). The isolation stage has relatively fixed voltage conversion ratio. The system operates in a manner very similar to a conventional series-resonant converter, except that the magnetic core is driven in parallel by two identical primary windings.

S_A-S_D are reused to create a 2:1 ladder switched-capacitor structure that can balance the two stacked bus voltages (V_X and $2V_X$) formed by the two capacitors (C_1 and C_2). Charge is transferred through an additional capacitor, C_3 , which ties the two switch nodes together. The switched-capacitor charge-redistribution mechanism ensures $V_{C1} \approx V_{C2}$. The combination of a switched-capacitor circuit and a multiple-winding transformer may be described as a *hybrid switched-capacitor/magnetics* circuit structure. This structure serves as a core sub-section of the MultiTrack architecture - the switching of this structure drives the MISO transformer, and at the same time smoothly re-balances the power processed by different tracks with low loss. The hybrid structure also enables ZVS of the switched capacitor switches (which is not available in conventional switched-capacitor converters). Resonant switched-capacitor and zero-current-switching (ZCS) mechanisms can be included by adding inductive impedances in the C_3 branch.

The merged regulation stage in this 2-Track converter comprises inductor L_R and switches S_1 and S_2 . By controlling the duty ratio of S_1 and S_2 , the voltage of C_1 is regulated, and the voltage of C_2 is effectively regulated through the switched-capacitor mechanism. In this embodiment, voltage regulation and dynamic control are dominated by the modulation of S_1 and S_2 . For an input voltage v_{in} between V_X and $2V_X$, S_1 and S_2 are controlled such that the voltages across C_1 and C_2 are always V_X . If v_{in} is closer to V_X , S_2 has a higher duty ratio and more charge is delivered to V_X ; if v_{in} is closer to

$2V_X$, S_1 has a higher duty ratio and more charge is delivered to $2V_X$. If S_1 and S_2 are switched in complimentary pulse-width-modulation (PWM) mode, the duty ratio of S_1 that can regulate the voltage across C_1 and C_2 to be V_X , d_1 , is

$$d_1 = \frac{v_{in} - V_X}{V_X}. \quad (1)$$

and the duty ratio of S_2 , d_2 , is

$$d_2 = 1 - d_1 = 2 - \frac{v_{in}}{V_X}. \quad (2)$$

This is somewhat similar to regulating a boost converter, but with V_X instead of ground as the second potential. Other similar control approaches (e.g. DCM control, constant on-time control, current-mode control) can also be used.

The merged isolation stage of the MultiTrack architecture employs magnetic coupling to provide isolation and to combine the power carried by the multiple intermediate buses. In the 2-Track converter shown in Fig. 2, the isolation stage can be interpreted as two ac power tracks distributed in two stacked voltage domains ($[0, V_X]$ and $[V_X, 2V_X]$), each processing a half of the output power. The cross-sectional area of the magnetic core is determined by the volt-seconds of the secondary winding. The window area of the magnetic core is determined by the output current. Thus, the power conversion stress of the merged isolation stage in this 2-Track converter is the same as a conventional series-resonant converter, indicating equivalent magnetics volume and efficiency. It is in some respects similar to a series-primary parallel-secondary configuration [16], whereas only a single magnetic core and a single rectifier is needed. This MultiTrack configuration distributes the concentrated device voltage-ratings on the high-voltage side into multiple devices, which can take advantage of the distributed power processing concept [17]–[20]. Moreover, as will be shown shortly, the current driven through the common-mode capacitances of the transformer is much smaller than that in a single-primary-winding design. This effect is beneficial in high frequency designs.

IV. EXTENDED MULTITRACK ARCHITECTURE WITH WIDE INPUT VOLTAGE RANGE

The basic 2-Track converter shown in Fig. 2 is suitable to applications when $v_{in} \in [V_X, 2V_X]$ with a restricted nominal 2-to-1 input voltage range. However, by adding two additional switches (S_3 and S_4) in the regulation stage as shown in Fig. 3, the converter can handle any desired input voltage range in the $[0, 2V_X]$ region (i.e. $[V_{min}, V_{max}] \in [0, 2V_X]$), so long as the components are sized appropriately.

The voltage ratings of C_1 and C_2 are both V_X . The operation of this enhanced design can be split into two regions determined by the input voltage v_{in} . When $v_{in} \in [0, V_X]$, S_3 and S_4 are switching, S_1 is kept off, and S_2 is kept on. In this manner, the L_R , S_3 and S_4 formulates a ground referenced boost converter that feeds current into the V_X node. The switched capacitor circuit balances the voltages of C_1 and C_2 . When $v_{in} \in [V_X, 2V_X]$, S_3 is kept on, S_4 is kept off, and S_1 and S_2 are switching. The L_R , S_1 and S_2 formulates boost-based converter structure that feeds power from the input

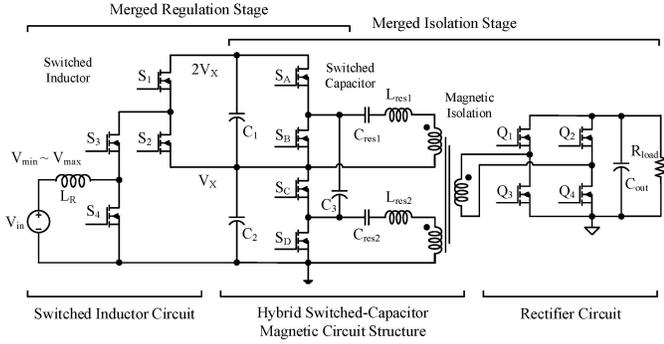


Fig. 3. An example 2-Track power converter that can handle wide input voltage range. For this converter, the maximum input voltage, V_{\max} , must be smaller than $2V_X$.

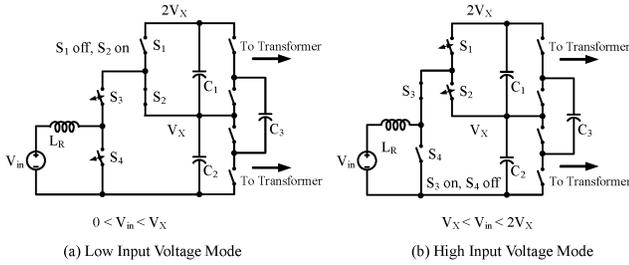


Fig. 4. Two operation modes of the two pairs of half-bridges in the regulation stage of a 2-Track converter: (a) when $0 < v_{\text{in}} < V_X$, S_3 and S_4 are switching, S_1 is kept off, and S_2 is kept on; (b) when $V_X < v_{\text{in}} < 2V_X$, S_3 is kept on, S_4 is kept off, and S_1 and S_2 are switching.

into both the V_X and the $2V_X$ node. Fig. 4 illustrates the operation of the switches in these two operation modes. Within each subsection of the voltage domain, conventional feedback control methodology (e.g. the classic PID based PWM control) for boost converters can be directly utilized in the proposed MultiTrack architecture. When the input voltage fluctuates between two regions, a hysteresis control can be utilized to stabilize the transition across the two regions.

Figure 4 shows the two different operating modes of the merged regulation stage of the circuit. Depending upon the operating mode, the switched capacitor charge transfer is used differently to maintain voltage balance between the two stacked capacitors. When the input voltage is high, power (from the input and inductor) is injected into both the V_X and $2V_X$ nodes, and the total voltage of the two stacked capacitors (voltage $2V_X$) serve to counter the input voltage (in providing volt-seconds balance on the inductor). When the input voltage is low, the input power is injected into the V_X node only. The switched capacitor energy transfer operates to redistribute charge such that the different windings of the isolation stage magnetics can be utilized equally. The PWM operation of the half-bridges (S_1 - S_4) in conjunction with the switched-capacitor conversion enables voltages V_X and $2V_X$ to be regulated with low stress on the inductor and with balanced utilization of the isolation stage magnetics across the full input voltage range.

In this wide input voltage range 2-Track converter, the magnitude of the voltage applied across the inductor L_R never

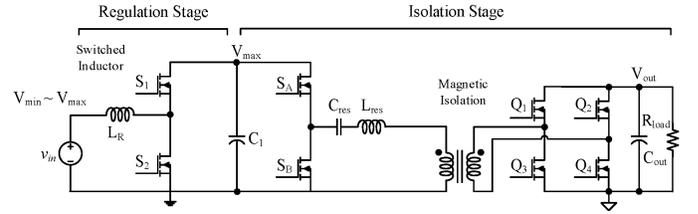


Fig. 5. Schematic of a conventional boost-type two-stage (BTS) converter having a boost converter as the regulation stage, and a series-resonant converter as the isolation stage.

exceeds V_X , and the charge coming from the input source is always delivered to the closest dc voltages to the input. For example, if $v_{\text{in}} \in [0, V_X]$, power coming from v_{in} is always delivered to the V_X node; if $v_{\text{in}} \in [V_X, 2V_X]$, power coming from v_{in} is always delivered to the V_X node and the $2V_X$ node. As will be analyzed, the smaller resulting voltage conversion ratio of the regulation stage can significantly reduce the inductor size and/or the regulation loss.

The MISO transformer in the isolation stage has multiple primary windings and a single secondary winding. One can synthesize different impedance tanks to implement different isolation circuits for different purposes, e.g., LLC converters, series-resonant converters, dual-active-bridge converters. If planar transformers are utilized, a systematic magnetics modeling technique [21] that can rapidly estimate the impedances and current distribution can be utilized.

Many known rectifier structures (e.g. center-tapped rectifier, current-doubler rectifier, full bridge rectifier, switched-capacitor step-down rectifier [22], etc.) are compatible with the MultiTrack architecture. A full bridge rectifier with high experimental flexibility is selected as the example in this paper.

V. COMPARATIVE ANALYSIS

The boost-type two-stage (BTS) power conversion architecture as shown Fig. 5 is widely used in wide input voltage range applications, e.g. grid-interface power factor correction (PFC) circuits [23]–[26]. In the BTS architecture, the input voltage is at first boosted to an relatively fixed intermediate bus voltage that is equal to or higher than the maximum input voltage. This voltage is then converted into the desired output voltage by an isolation stage with a fixed voltage conversion ratio.¹ Interestingly, the BTS converter is actually a 1-Track embodiment of the MultiTrack architecture - if there is only one power track and one intermediate voltage level.

Here we compare the 2-Track converter to a BTS converter for an input voltage range of $[V_{\min}, V_{\max}]$. The intermediate

¹A buck-type two-stage architecture with a buck converter as the regulation stage is also widely used, especially in telecom power converters. In a buck-type implementation, the wide input voltage range is first regulated to a voltage that is lower than or equal to the minimum input voltage. The analysis results for such a converter would be quite similar in terms of device stresses and energy storage requirements. Since the Buck converter is a topological dual of the Boost converter, many of their theoretical characteristics are similar or even identical. The MultiTrack design we have implemented is more related to the boost-type two-stage architecture because its regulation stage is more similar to a boost converter. As a result, we use the boost-type two-stage architecture as a benchmark in this paper.

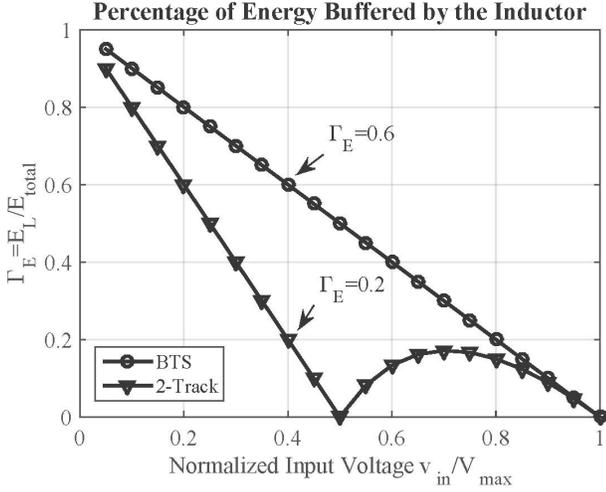


Fig. 6. Fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_L/E_{total}$). E_L is the energy buffered by the inductor. E_{total} is the total energy processed by the full system.

bus voltage of the conventional BTS converter is assumed to be V_{max} . The two intermediate bus voltages of the 2-Track converter are $\frac{1}{2}V_{max}$ and V_{max} .

A. Reduced Regulation Inductor Size.

Both the BTS converter and the 2-Track converter have a voltage regulation inductor (L_R) in the regulation stage. The size of L_R is proportional to the maximum amount of energy that it needs to buffer in each switching cycle, which is related to the voltage conversion ratio of the regulation stage [27]. We define Γ_E as the ratio between the energy buffered in the inductor in each switching cycle, and the total energy that the converter delivers in each switching cycle. For a fixed output power, a higher Γ_E ratio indicates a higher inductive energy buffering requirement, yield a larger inductor size. As derived in Appendix I, the Γ_E of the BTS converter when $v_{in} \in [V_{min}, V_{max}]$ is

$$\Gamma_{E,BTS}|_{v_{in} \in [V_{min}, V_{max}]} = 1 - \frac{v_{in}}{V_{max}}. \quad (3)$$

Γ_E increases monotonically as the input voltage reduces. This is because the boost converter in the BTS architecture has a higher voltage conversion ratio if the input voltage is lower (closer to V_{min}). The inductor needs to be sized for the worst case - when the input voltage equals to V_{min} .

The Γ_E of a 2-Track converter when $v_{in} \in [V_{min}, V_{max}]$ is a piecewise function of v_{in} . As derived in Appendix I, the Γ_E when $v_{in} \in [0, \frac{1}{2}V_{max}]$ is

$$\Gamma_{E,2-Track}|_{v_{in} \in [0, \frac{1}{2}V_{max}]} = 1 - \frac{v_{in}}{\frac{1}{2}V_{max}}. \quad (4)$$

The Γ_E when $v_{in} \in [\frac{1}{2}V_{max}, V_{max}]$ is

$$\Gamma_{E,2-Track}|_{v_{in} \in [\frac{1}{2}V_{max}, V_{max}]} = \frac{(V_{max} - v_{in})(v_{in} - \frac{1}{2}V_{max})}{\frac{1}{2}V_{max}v_{in}}. \quad (5)$$

(3)–(5) are plotted and compared in Fig. 6. The Γ_E of the 2-Track converter is lower than that of the BTS converter across the full input voltage range. As labeled in Fig. 6, if the input voltage range is $[0.4V_{max}, V_{max}]$, the maximum Γ_E of the 2-Track converter is 66.7% lower than that of the BTS converter, indicating significant inductor size reduction.

B. Reduced Switch Conduction Loss and Switch Stress.

The switches in the regulation stage of the BTS converter (S_1 and S_2) have to block the peak input voltage (V_{max}). In the 2-Track converter shown in Fig. 3, S_1 , S_2 and S_3 only need to block $\frac{1}{2}V_{max}$. S_4 still needs to block V_{max} , but it only conducts for achievable stresses and portion of the input voltage range. This mechanism reduces the achievable stresses and conduction loss of the switches. For an ideal Schottky junction device, the on-resistance (per die area) of the drift region is a quadratic function of its rated voltage V_B (“Baliga Figure-of-Merit”) [28]. In a BTS converter, S_A and S_B both needs to block V_{max} . Making the simplifying assumptions that the two switches have the same drain-to-source resistance $R_{V_{max}}$, and the regulation inductor has small current ripple, the total conduction loss in the two switches can be calculated as a function of the input voltage (v_{in}) and input power (P_{in}):

$$Loss_{BTS} = \left(\frac{P_{in}}{v_{in}}\right)^2 R_{V_{max}}. \quad (6)$$

In a 2-Track converter, S_1 , S_2 and S_3 need to block $\frac{V_{max}}{2}$. Their resistances are $\frac{1}{4}R_{V_{max}}$. S_4 needs to block V_{max} . Its resistance is $R_{V_{max}}$. The total conduction loss is a piecewise function of the input voltage v_{in} . When $v_{in} \in [0, \frac{1}{2}V_{max}]$, S_1 is kept off; S_2 and S_3 is conducting with a duty ratio of $(\frac{2v_{in}}{V_{max}})$; and S_4 is conducting with a duty ratio of $(1 - \frac{2v_{in}}{V_{max}})$. The input current, i_{in} , is also a function of v_{in} , $i_{in} = P_{in}/v_{in}$. Assume the inductor current equals the input current and has no ripple. the total conduction loss in the devices of the switched-inductor circuit can be estimated as

$$Loss_{2-Track} = \frac{P_{in}^2}{v_{in}^2} R_{V_{max}} \left(1 - \frac{v_{in}}{V_{max}}\right). \quad (7)$$

When $v_{in} \in [\frac{1}{2}V_{max}, V_{max}]$, S_4 is kept off. The inductor current constantly passed through two switches each has a resistance of $\frac{1}{4}R_{V_{max}}$:

$$Loss_{2-Track} = \frac{P_{in}^2}{2v_{in}^2} R_{V_{max}}. \quad (8)$$

For BTS converter, the resistances of both the two regulation switches are $R_{V_{max}}$, the total conduction loss is

$$Loss_{1-Track} = \left(\frac{P_{in}}{v_{in}}\right)^2 R_{V_{max}}, \quad (9)$$

(7)-(9) are plotted and compared in Fig. 7. As labeled in Fig. 7, if $v_{in} \in [0.4V_{max}, V_{max}]$, the estimated conduction loss of the switches in the regulation stage of the 2-Track converter is 46.7% lower than those in the BTS converter.

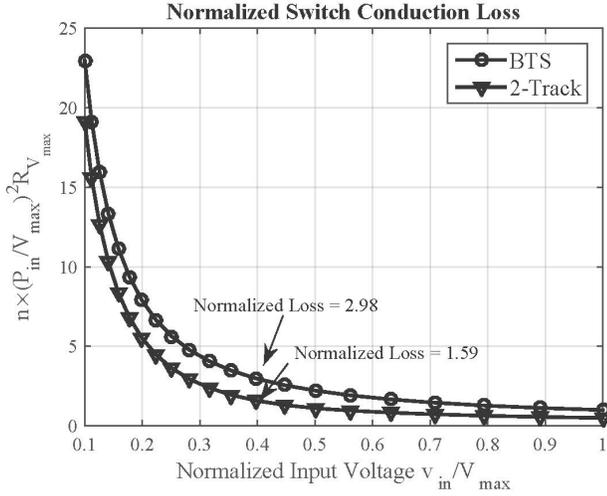


Fig. 7. Normalized switch conduction loss as a function of the normalized input voltage range. The 2-Track converter has a lower conduction loss than the Boost converter (1-Track) converter across the full input voltage range.

C. Soft-Switching and Reduced Switching Loss

The high-side switch of a boost converter (S_1 in Fig. 5) can operate as a diode, with zero-voltage turn on. Under PWM operation with small inductor current ripple, the low side switch (S_2) is usually hard-switched at both turn on and turn off. The rated voltage of S_2 is V_{\max} . And S_2 always blocks V_{\max} regardless of v_{in} . In an 2-Track converter, the low-side switches (S_2 and S_4) may also be hard-switched in the worst case. The voltage ratings of these switches are $\frac{1}{2}V_{\max}$ and V_{\max} , respectively. Although their voltage ratings are different, when they are switching, their off-state drain-to-source voltages are always $\frac{1}{2}V_{\max}$, which is much lower than the switching voltage of the devices in the BTS converter (V_{\max}), enabling reduced total switching loss to be achieved.

VI. PROTOTYPE DESIGN

To demonstrate the advantages of the MultiTrack power conversion architecture, an 18 V–80 V input, 5 V output, 15 A output, 75 W, 800 kHz, 2-Track converter has been built and tested. The prototype is designed based on the schematic shown in Fig. 3. The two intermediate voltage levels are regulated at 40 V and 80 V, respectively. A simplified bill-of-materials (BOM) of the prototype is listed in Table I.

Fig. 8 shows the gate drive implementation of the eight primary-side switches (S_1 – S_4 and S_A – S_D). Two identical gate drive modules are utilized. S_1 , S_2 , S_A and S_B are driven by one gate drive module referring to the $\frac{1}{2}V_{\max}$ node. S_3 , S_4 , S_C and S_D are driven by another gate drive module referring to the ground. Each gate drive module contains one linear regulator, four level-shifters and two half-bridge gate drivers. The ground-referenced gate drive module is powered by the input voltage. The $\frac{1}{2}V_{\max}$ referenced gate drive module is powered by C_1 . This gate drive configuration can be easily integrated and extended to drive the switches in an n -track implementation. An auxiliary transformer winding (4-turns) with full-bridge diode arrays and linear regulators is utilized to power the two secondary-side half-bridge gate drivers.

TABLE I
BILL OF MATERIALS (BOM) OF THE PROTOTYPE CONVERTER.

Device Symbol	Component Description
S_1 – S_4 , S_A – S_D	EPC2016c
L_R	Coilcraft EPL6024-522ME: 5.2 μH , 44 mohm, height (measured): 2 mm
C_{in}	X5R Ceramic, 100 V, 2 μF , 1206
C_1 , C_2	X7R Ceramic, 50 V, 10 μF , 1206
C_3	X7R Ceramic, 50 V, 15 μF , 1206
C_{out}	X5R Ceramic, 10 V, 188 μF , 0805
C_{res1} , C_{res2}	COG Ceramic, 50 V, 0.1 μF , 1206; X7R Ceramic, 50 V, 0.2 μF , 1206;
MISO Transformer	Ferroxcube EQ13, Core Material 3F45, turns ratio 4:4:1, 8-layer PCB layers and 2 external 2 oz foil layers.
Q_1 – Q_4	EPC2023c

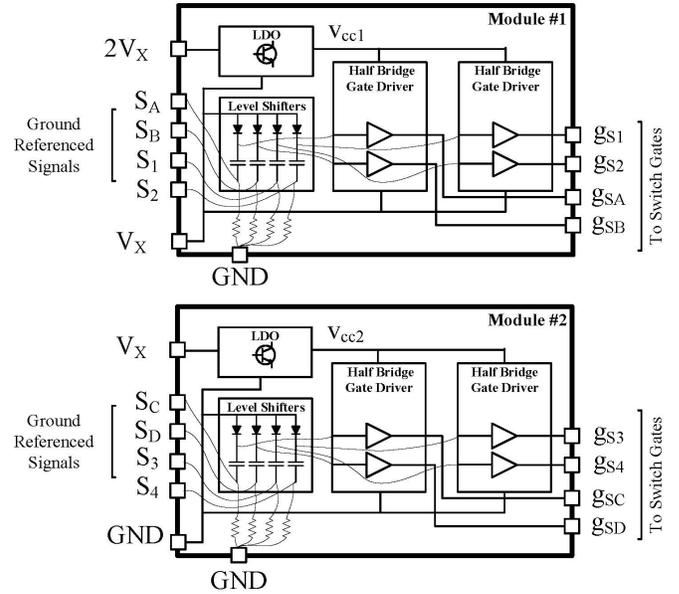


Fig. 8. The gate drive implementation of the primary side switches. Two identical gate drive module are stacked in two voltage domains. This gate drive implementation can be easily extended and utilized in an n -track implementation. The bottom gate drive module can be optionally powered from V_{in} to enable immediate start-up.

A Texas Instruments TMS320F28069 micro-controller with 4 PWM channels is utilized to control the prototype. As explained in Fig. 4, there are two operating modes for the regulation switches (S_1 – S_4): (1) when the input voltage is between 18 V and 40 V, S_2 is kept on, S_1 is kept off, and S_3 and S_4 switch; (2) when the input voltage is between 40 V and 80 V, S_3 is kept on, S_4 is kept off, and S_1 and S_2 switch. In actual operation, neither of S_2 and S_3 can be kept on continuously - an interval is needed to enable the boot-strap and level shifter capacitors to be refilled periodically. Also, when the input voltage is very close to 40 V, it is a challenge to modulate the duty ratio of S_2 and S_3 because their duty ratios are either very close to unity or zero. To address these practical issues, we have added a “Dual Modulation Mode” operation in which both the two half-bridge pairs are modulated:

1) *Low Input Voltage Mode*: when the input voltage is below

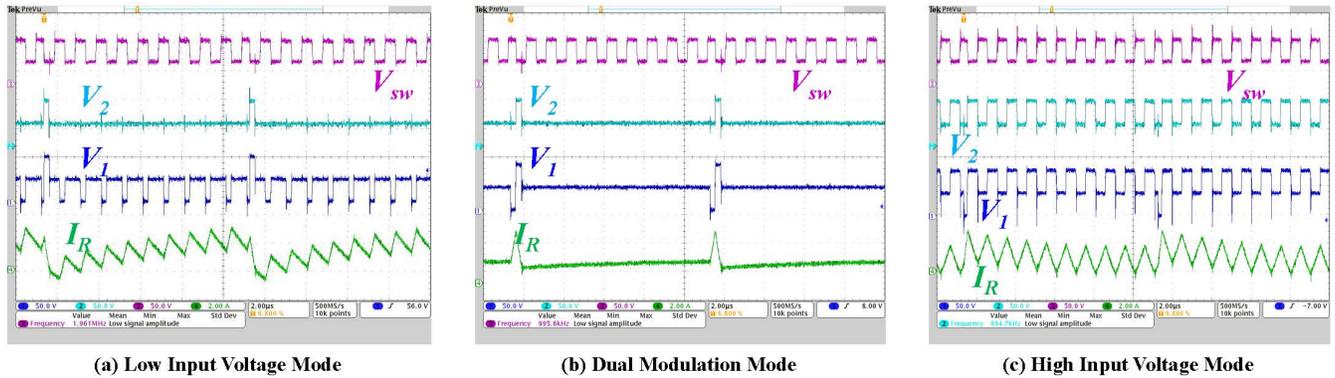


Fig. 9. Example operation waveforms of the prototype converter working in three different operation modes. V_{sw} is the switch node between S_A and S_B . V_1 is the switch node between S_3 and S_4 . V_2 is the switch node between S_1 and S_2 . I_R is the current of the regulation inductor. (a) Low Input Voltage Mode: $v_{in}=20$ V, $I_{out}=7$ A, with S_1 and S_2 switched at 80 kHz, and S_3 and S_4 switched at 800 kHz; (b) Dual Modulation Mode: $v_{in}=40$ V, $I_{out}=9.5$ A, with two half-bridges both switched at 80 kHz; (c) High Input Voltage Mode: $v_{in}=60$ V, $I_{out}=10$ A, with S_1 and S_2 switched at 800 kHz, and S_3 and S_4 switched at 80 kHz. The dual-modulation frequency was selected as 80 kHz in this demonstration to show the low frequency fluctuation of the inductor current. The real circuit operation used 20 kHz as the lower frequency.

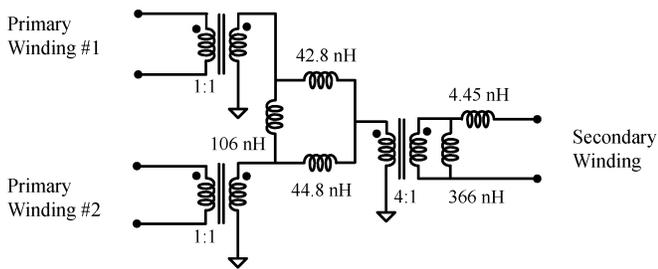


Fig. 10. Experimentally extracted cantilever model of the prototype MISO transformer.

40 V, S_1 is mostly kept off, and S_2 is mostly kept on. S_2 may be switched off for a short period of time (minimum transistor on-time) every few switching cycles (10-20 cycles) to reset the level-shifter capacitor of S_2 . S_3 and S_4 are switched at the PWM frequency.

- 2) *Dual Modulation Mode*: when the input voltage is close to 40 V, S_1 and S_4 are kept off, and S_2 and S_3 are kept on. S_2 and S_3 may be switched off for a short time every long period to reset their level-shifter/boot-strap capacitors. Modulating the difference between the on-time of S_2 and S_3 provides the desired voltage regulation capability when the input voltage fluctuates around 40 V.
- 3) *High Input Voltage Mode*: when the input voltage is above 40 V, S_3 is mostly kept on, and S_4 is mostly kept off. S_4 may be switched on for a short period of time every few switching cycles to reset the boost-strap capacitor of S_3 . S_1 and S_2 are switched at the PWM frequency.

Measured waveforms illustrating these three operation modes are shown in Fig. 9.

The regulation inductor should be designed such that it can work efficiently across the wide input voltage range and power range. Low profile is also a critical requirement in this prototype as the inductor tends to be the tallest component on the board. We choose to size the inductor such that it has 50% current ripple when the input voltage is at 30 V, the output

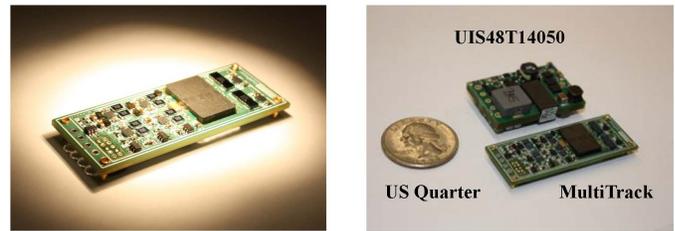


Fig. 11. Pictures of the MultiTrack prototype, a US quarter, and a commercial product (UIS48T14050).

power is 75 W, with 800 kHz switching frequency. The average inductor current is 2.5 A, and the calculated inductance value is $3.75 \mu\text{H}$. A low profile Coilcraft inductor (EPL6024-522) with 2 mm measured thickness is utilized to implement this inductor. Its loss across the overall input voltage range is within the loss budget. It is the tallest component on the board. It also becomes a major loss component when the input voltage is close to the minimum of the full voltage range (e.g. $18 \text{ V} < v_{in} < 25 \text{ V}$). A custom designed inductor with wider area and lower thickness could further improve the power density and efficiency of the prototype (for example, reducing the inductor height from 2 mm to 1.5 mm could raise the overall converter box power density from 453.7 W/in^3 to higher than 500 W/in^3).

The multiple ac-tracks in the isolation stage are implemented as low-Q series resonant converters. The resonant inductance of each low-Q tank is created using the leakage inductance of the transformer, together with the PCB trace inductances. Since the resonant tank has low-Q (when loaded with the equivalent rectifier resistance of 0.33 ohm at full power), precise impedance matching between the two primary windings is not necessary. The ac resistance of the secondary winding of the MISO transformer needs to be minimized because it has to carry the full output current (up to 15 A).

A Ferroxcube EQ13 core with 3F45 material was selected based on core loss and winding loss analysis. It was selected also because it has suitable window-area/core-area/height com-

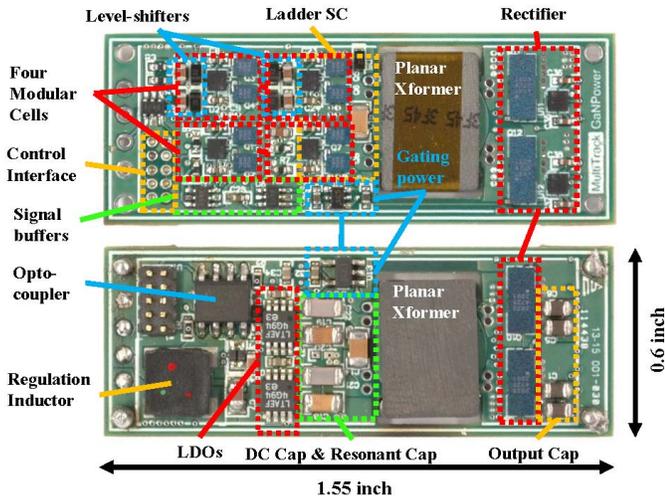


Fig. 12. Component placement on the top and bottom side of the PCB board. The four modular half-bridge cells contain level shifters, LDOs, gate drivers and switches.

binations. The windings were fabricated on a 8-layer printed circuit boards (PCB) with 2 oz copper on each layer. The finished pcb board thickness is 52 mil (1.32 mm).

The loop inductance between the two legs of the secondary winding also contributes to the series-resonant tank. Utilizing the method provided in [29], the loop inductance is estimated to be about 3 nH. The trace inductances added by the switches are estimated to be about 0.5 nH. The leakage inductance associated with the 10-layer planar windings is estimated utilizing the planar magnetics modeling approach presented in [21]. Fig. 10 shows the cantilever circuit model of the transformer extracted by doing open- and short-circuit measurements.

Fig. 11 shows pictures of the prototyped 18 V–80 V input, 5 V output, 75 W isolated dc-dc converter and a US quarter. Fig. 12 shows component placement on the top and bottom sides of the PCB board. There are four modular switch and gate drive circuits on the primary side. Each modular switch and gate drive circuit consists two switches (EPC2016c) formulating a half-bridge, one LM5113 half-bridge gate drive, and the corresponding signal paths. They are placed on the top side of the PCB board. The full bridge rectifier consists four switches: two of them are on the top side of the board, two of them are on the bottom side of the board. The opto-coupler, linear regulator, capacitors and other auxiliary circuits and chips are placed on the bottom side of the board. The regulation inductor (L_R) is placed on the left-bottom corner of the PCB board. The microcontroller (TMS320F28069) interfaces with the prototype through a 10-pin interface for experimental convenience. If the microcontroller needs to be placed on the board, the 10-pin interface can be removed to create sufficient board area. The estimated board area of the TMS320F28069 microcontroller is 12 mm \times 12 mm.

VII. EXPERIMENTAL RESULTS

A state-of-the-art commercial 1/16 brick 18 V–75 V input, 5 V output, 75 W isolated dc-dc converter (Power-One UIS48T14050) was utilized to benchmark this MultiTrack

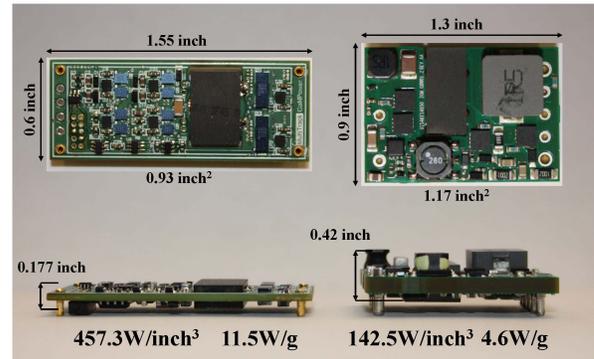


Fig. 13. Form factors of the prototype MultiTrack converter (left) and a comparable commercial converter (PowerOne UIS48T14050, right).

prototype [30]. This converter has the highest power density among commercial converters with similar input voltage range and the same output voltage that the authors were able to find. Fig. 13 compares the form factor of the two converters. Both converters have two magnetic devices - one transformer and one inductor (this commercial product is speculated to be a forward converter). Benefiting from the MultiTrack architecture and the higher switching frequency, the inductor utilized in the MultiTrack converter is about six times smaller than the inductor utilized in the commercial converter (80 mm³ v.s. 480 mm³). The box power density of the MultiTrack prototype is 457.3 W/inch³, which is 3.2 times higher than the 143.5 W/inch³ of the commercial product (the rated power is defined under 200 LFM 25 °C air flow and 125 °C peak device temperature). The prototype weighs 6.53 g, which is 42.7% of the 15.3 g of the commercial product.

Figs. 14–15 show the measured efficiency of the prototype with an ambient temperature of 25 °C at 200 LFM air flow (measured using a Pyle PMA90 digital anemometer with a 2.4 W fan). The prototype converter achieves a peak efficiency of 91.3% when the input voltage is 58 V and when the output current is 8 A. Its efficiency is comparable to the commercial product but shows a beneficial profile [30]. When the input voltage is high, the MultiTrack converter is more efficient. When the input voltage is low, the commercial converter is more efficient. Benefiting from the splitted voltage domains, the efficiency of the MultiTrack prototype is relatively fixed across the 18 V–80 V input voltage range. In contrast, the efficiency of the commercial product spans across a wide range (about 5% difference between $v_{in} = 18$ V and $v_{in} = 75$ V).

Fig. 16 compares the figures-of-merit (FOM) of the MultiTrack prototype and many state-of-the-art commercial products (with the power density defined under 200 LFM 25 °C air flow with 125 °C allowable device temperature). All these commercial products have 18 V–75 V input and 5 V output. They utilize Silicon devices and are switching at around 200 kHz–300 kHz. By employing the proposed MultiTrack power conversion architecture with reduced inductor size and PCB thickness, switching at higher frequency, and taking advantages of the miniaturized GaN switches, the MultiTrack converter achieves 3x higher power density while maintaining comparable efficiency and lower peak board temperature.

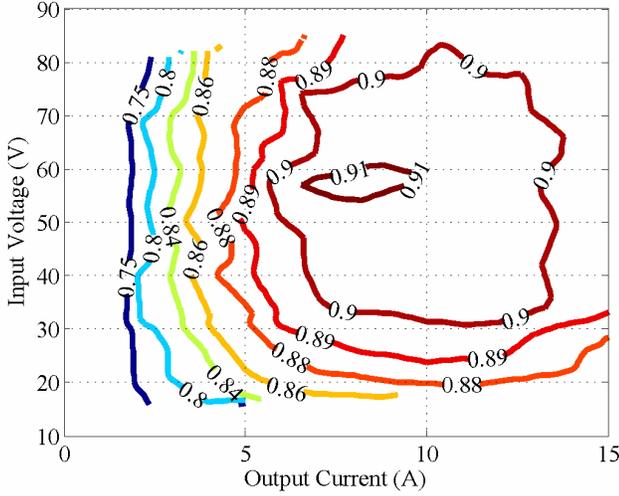


Fig. 14. Efficiency of the MultiTrack converter over the 18 V–80 V input voltage, 0 A–15 A output current range with 200 LFM, 25°C air flow.

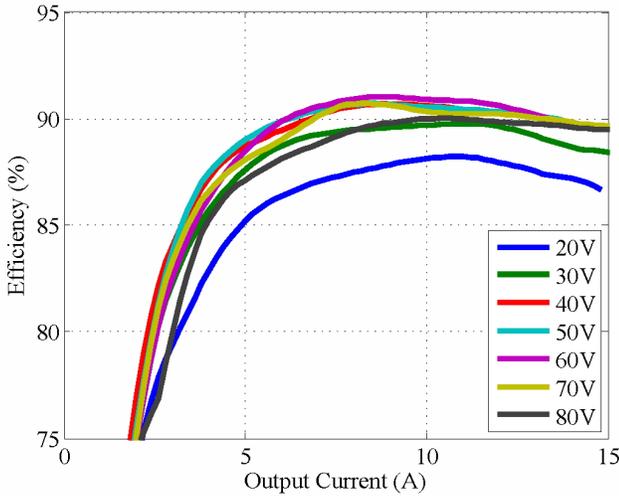


Fig. 15. Efficiency of the prototype converter over the 18 V–80 V input voltage, 0 A–15 A output current range with 200 LFM, 25°C air flow.

VIII. CONCLUSIONS

A MultiTrack power conversion architecture that is suitable for designing isolated dc-dc converters with wide input voltage range is explored in this paper. This power conversion architecture represents a new way of combining switched-capacitor circuits and magnetics. It leverages the complementary strengths of switched-inductor, switched-capacitor, and magnetic isolation circuits, and gains mutual benefits from the way they are merged together. Employing the distributed power processing concept, power is processed in multiple voltage domains and current channels, allowing many advantages to be achieved. A prototype 18 V–80 V input, 5 V output, 15 A, 800 kHz, 0.93 inch² (1/16 brick equivalent) isolated dc-dc converter was designed and tested. It achieves 3x higher power density than industry state-of-the-art product while maintaining high efficiency and low peak board temperature.

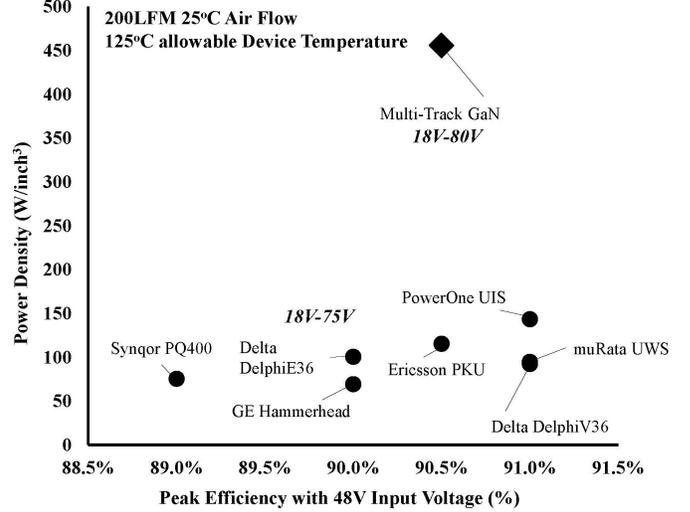


Fig. 16. Comparing the MultiTrack converter with many state-of-art commercial products (18 V–75 V input voltage, 5 V output voltage). The MultiTrack converter achieves 3x higher power density while maintaining comparable efficiency performance.

ACKNOWLEDGEMENTS

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APPENDIX I: INDUCTOR ENERGY STORAGE ANALYSIS

In the MultiTrack architecture, the full input voltage range is split by the two intermediate bus voltages ($\frac{1}{2}V_{\max}$ and V_{\max}) into two voltage domains ($[0, \frac{1}{2}V_{\max}]$ and $[\frac{1}{2}V_{\max}, V_{\max}]$). The inductor energy buffering ratio Γ_E is a piecewise function of the input voltage v_{in} . In each of the input voltage region, the regulation circuit can be modeled as a direct converter having v_{in} as the input voltage level, and $\frac{k-1}{2}V_{\max}$ and $\frac{k}{2}V_{\max}$ as the two output voltage levels, as illustrated in Fig. 17a ($k = 1$ or $k = 2$). Fig. 17b shows the inductor current i_R assuming the converter works in the critical continuous-conduction-mode (CCM). In the critical CCM mode, the inductor is fully charged and discharged in each switching cycle, yielding the highest inductor utilization ratio. The average current of i_R is I_{avg} , and the peak current of i_R is $I_{pk} = 2I_{avg}$. The switching period is T_{sw} . The total energy that is processed by this circuit in each switching cycle is

$$E_{total} = v_{in} \times I_{avg} \times T_{sw} = \frac{1}{2}V_{in}I_{pk}T_{sw}. \quad (10)$$

The inductance that enables the critical CCM operation is

$$L_R = \frac{(V_X - v_{in})d_X T_{sw}}{I_{pk}} = \frac{(V_X - v_{in})(v_{in} - V_Y)T_{sw}}{I_{pk}(V_X - V_Y)}. \quad (11)$$

The peak energy that is buffered in the inductor L_R is

$$E_{L_R} = \frac{1}{2}L_R I_{pk}^2 = \frac{1}{2} \frac{(V_X - v_{in})(v_{in} - V_Y)T_{sw}I_{pk}}{(V_X - V_Y)}. \quad (12)$$

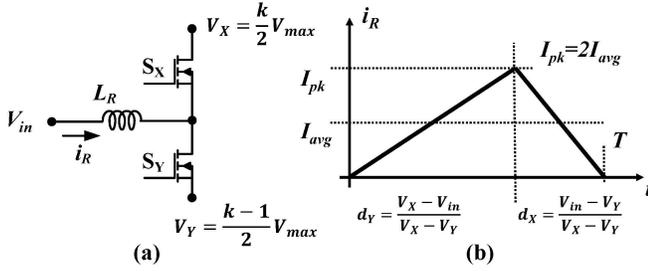


Fig. 17. The regulation circuit can be treated as an indirect converter having V_{in} , V_X and V_Y as the three nodal voltages.

The percentage of energy that is buffered in the inductor when v_{in} belongs to $[\frac{k-1}{2}V_{max}, \frac{k}{2}V_{max}]$ region, Γ_E , is

$$\begin{aligned} \Gamma_{E,2-track} \Big|_{\frac{k-1}{2}V_{max} < v_{in} < \frac{k}{2}V_{max}} &= \frac{E_{L_R}}{E_{total}} \\ &= \frac{(V_X - v_{in})(v_{in} - V_Y)}{(V_X - V_Y)} \\ &= \frac{(\frac{k}{2}V_{max} - v_{in})(v_{in} - \frac{k-1}{2}V_{max})}{\frac{1}{2}V_{max}v_{in}}. \end{aligned} \quad (13)$$

For an 1-Track converter, the Γ_E as a function of the normalized input voltage $\frac{v_{in}}{V_{max}}$ is

$$\Gamma_{E,BTS} \Big|_{v_{in} \in [V_{min}, V_{max}]} = 1 - \frac{v_{in}}{V_{max}}, \quad (14)$$

which is equal to the Γ_E of the boost converter in a BTS architecture.

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