

Tutorial: Using *M2Spice* to Simulate a Transformer with 8 Layers and 4 Windings operating at 500 kHz

Minjie Chen and Samantha Gunter

1 ORGANIZING THE GEOMETRY INFORMATION

M2Spice is well-suited for modeling planar magnetics with sophisticated winding/interleaving patterns. This tutorial introduces a few basic techniques about using *M2Spice* in planar magnetics designs. We choose a planar transformer with four windings, as shown in Fig. 1, as an example. This transformer has two primary windings, and two secondary windings. The two primary windings are driven by two different voltage sources, and the two secondary windings are loaded by two different resistors. If the skin- and proximity effects need to be considered, this example transformer cannot be easily solved using a conventional magnetics modeling approach.

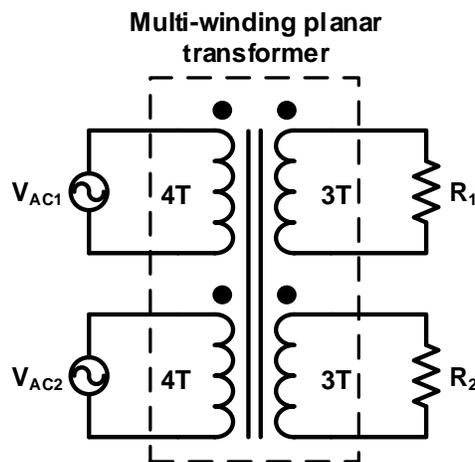


Fig. 1: A planar transformer with four windings. The leakage inductance, mutual inductance and magnetizing inductance are not shown. We wish to calculate the current sharing in the four windings considering the parasitics and skin- and proximity-effects.

The *M2Spice* software requires 18 different inputs about the core and the layer stack. These 18 variables are determined by the design of the core and the PCB layer stack.

1.1 MAGNETIC CORE

For this example, we choose to use a core produced by EPCOS. The geometry of the selected ELP43 core and the N49 material is shown in Fig. 2. A few parameters that will need to be utilized by *M2Spice* can be determined, including:

Input Description (variable name): **Example Value with units**

1. Name of the Component (x): **ex1**

You should assign a specific name to the magnetic device if you intend to have multiple sophisticated planar devices in the circuit simulation. Otherwise, this entry can be left blank.

2. Relative permeability of the core (μ_r): **1030**

3. Effective core area (A_c): **225 mm²**

4. Effective winding length per turn (d): **124 mm**

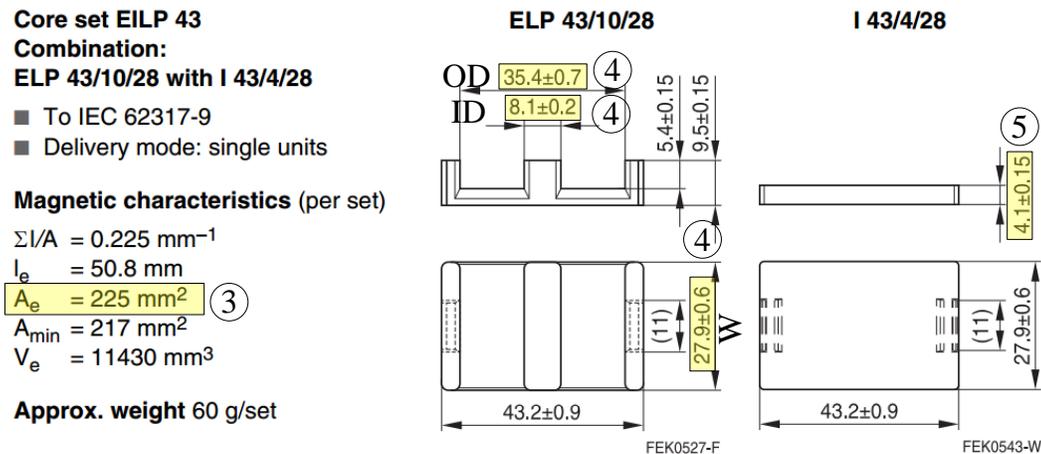
For the E core given in this example, this can be approximated as: $2W + \frac{\pi}{2}(OD + ID)$ where W is the width, OD is the outer diameter, and ID is the inner diameter of the core.

5. Thickness of the top and bottom core (c): **4.1 mm**

6. The targeted operation frequency (f): **500,000 Hz**

The netlist generated by *M2Spice* is rigorously accurate in single-frequency 1-D situations. It can usually provide sufficient accuracy in time domain circuit simulations.

Inputs 2-5 can usually be determined from the magnetic core manufacturer's datasheets.



Material	A_L value nH	μ_e	B_S^* mT	P_V W/set	Ordering code (per piece)
N49	5900 ±25%	1030 (2)	250	< 3.0 (50 mT, 500 kHz, 100 °C)	B66291G0000X149 (ELP core) B66291K0000X149 (I core)**

Fig. 2: Geometry of the ELP43 core (with I43) and the property of the N49 material. Available online: ELP43: http://en.tdk.eu/inf/80/db/fer_13/elp_43.pdf; N49: <http://en.tdk.eu/blob/528856/download/4/pdf-n49.pdf>.

1.2 PCB LAYER STACK

The windings for this example are fabricated with an eight layer printed circuit board (PCB). The PCB layer stack is shown in Fig. 3. The following information about the 1st to the 8th layers (from top to bottom, respectively) can be defined as:

Input Description (variable name):	Example Value with units
7. Number of Windings (nwind):	4
8. Total Number of Layers (nlayer):	8
9. Layer Thickness (h):	[0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3] m

The thickness of each copper layer from top to bottom. Common weights for PCB copper layers are ½ oz., 1 oz., 2 oz., 3 oz., and 4 oz. corresponding to thicknesses of 17.5 µm, 35 µm, 70 µm, 115 µm, and 140 µm, respectively.

10. Layer Conductivity (sigmac):	[5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7] S/m
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The conductivity of each copper layer from top to bottom. Usually the conductivity is the conductivity of copper: 5.8e7 S/m.

11. Spacing Thickness (s):	[1.82e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3] m
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The thicknesses of each spacing from top to bottom. The top spacing is the spacing between the top copper layer to the top core. The bottom spacing is the spacing between the bottom copper layer to the bottom core. This vector is usually one character longer than the number of layers.

12. Core Gap Length on the Top Side (gt):	0.2 mm.
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This is the total gap length the magnetic flux will travel on the top side. As shown in Fig. 3, the total gap length on the top side is the sum of the gap length of the two gaps (center leg gap and side leg gap).

13. Core Gap Length on the Bottom Side (gb):	0 mm.
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There is no gap on the bottom side of the core, in this example.

14. Spacing Permeability (mus):	[1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6] H/m
--	---

The permeability of each spacing from top to bottom. Usually mus is the permeability of air: $4\pi \times 10^{-7}$ H/m \approx 1.2566e-6 H/m.

15. Total Copper Width on Each Layer (w): [13.5e-3, 13.5e-3, 13.5e-3, 13.5e-3, 13.5e-3, 13.5e-3, 13.5e-3, 13.5e-3] m

This is the total copper width on each layer considering the potential clearance/spacing required by PCB manufacturers (trace to trace, trace to edge, etc.). This is usually a few millimeters smaller than the total window area width of the core. In this example, we use 13.5 mm as the effective copper width for all layers.

16. Number of Turns on Each Layer (m): [2, 1, 2, 3, 3, 1, 3, 2]

Number of turns on each layer from top to bottom. These turns are usually coaxial turns connected in series.

1.3 INTERCONNECTS

Fig. 3 also shows the following interconnect information, which formulate windings using layers.

- a) Winding 1 consists of layer 1 and layer 3. Layer 1 has 2 turns and layer 3 has 2 turns. Layer 1 and layer 3 are connected in series. Winding 1 has 4 total turns.
- b) Winding 2 consists of layer 2 and layer 4. Layer 2 has 1 turn and layer 4 has 3 turns. Layer 2 and layer 4 are connected in series. Winding 2 has 4 total turns.
- c) Winding 3 consists of layer 5 and layer 7. Layer 5 has 3 turns and layer 7 has 3 turns. Layer 5 and layer 7 are connected in parallel. Winding 3 has 3 total turns.
- d) Winding 4 consists of layer 6 and layer 8. Layer 6 has 1 turn and layer 8 has 2 turns. Layer 6 and layer 8 are connected in series. Winding 4 has 3 total turns.

The rest of the required parameters can be generated from the above description:

Input Description (variable name): Example Value with units

17. Connection style of each winding (wstyle): [0, 0, 1, 0].

This is used to indicate if a winding spread across multiple layers is connected in series or in parallel. The inputs must be either be '0' or '1'. '0' indicates a series connection and '1' indicates a parallel connection. The example value [0, 0, 1, 0] indicates that winding 1, 2, and 4 consist of multiple series layers; and winding 3 consists multiple parallel layers. The length of *wstyle* must match with *nwinding*. In this example, the *wstyle* must have four elements.

18. Belonging of each layer to windings (lindex): [1, 2, 1, 2, 3, 4, 3, 4].

- Layer 1 belongs to winding 1, thus the first element of *lindex* is 1.
- Layer 2 belongs to winding 2, thus the second element of *lindex* is 2.
- Layer 3 belongs to winding 1, thus the third element of *lindex* is 1.
- Layer 4 belongs to winding 2, thus the fourth element of *lindex* is 2.
- Layer 5 belongs to winding 3, thus the fifth element of *lindex* is 3.
- Layer 6 belongs to winding 4, thus the sixth element of *lindex* is 4.
- Layer 7 belongs to winding 3, thus the seventh element of *lindex* is 3.

- Layer 8 belongs to winding 4, thus the eighth element of *lindex* is 4.

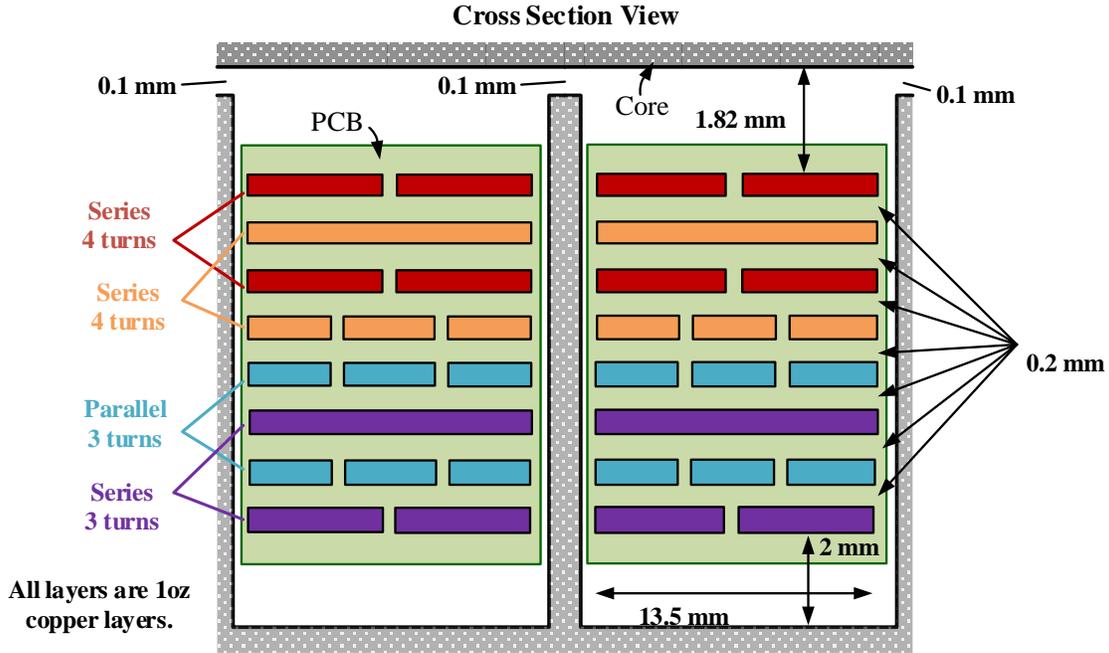


Fig. 3: Cross-section view of the example planar transformer.

Based on these design choices, we summarize the 18 required variables that are fed into *M2Spice*.

Table I Summary of the information that is required by *M2Spice*

1. Name of the Component (x):	ex1
2. Relative permeability of the core (μ_r):	1030
3. Effective core area (A_c):	225 mm ²
4. Effective winding length per turn (d):	124 mm
5. Thickness of the top and bottom core (c):	4.1 mm
6. The targeted operation frequency (f):	500,000 Hz
7. Number of Windings (n _{winding}):	4
8. Total Number of Layers (n _{layer}):	8
9. Layer Thickness (h): [0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3, 0.035e-3] m	
10. Layer Conductivity (σ): [5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7, 5.8e7] S/m	
11. Spacing Thickness (s): [0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3, 0.2e-3] m	
12. Core gap Length on the Top Side (gt):	0.2 mm
13. Core gap Length on the Bottom Side (gb):	0 mm
14. Spacing Permeability (μ_s): [1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6, 1.2566e-6] H/m	
15. Total Copper Width on Each Layer (w): [5e-3, 5e-3, 5e-3, 5e-3, 5e-3, 5e-3, 5e-3, 5e-3, 5e-3, 5e-3] m	
16. Number of Turns on Each Layer (m):	[2, 1, 2, 3, 3, 1, 3, 2]
17. Connection style of each winding (wstyle):	[0, 0, 1, 0]
18. Belonging of each layer to windings (lindex):	[1, 2, 1, 2, 3, 4, 3, 4]

2 GENERATING THE NETLIST

2.1 USER INTERFACE

The information presented in Table I can be fed into *M2Spice*. Once opened, the user interface (UI) of *M2Spice v1.1* looks like Fig. 4. There are eight functional buttons on the top row, followed by the variable entries and the corresponding notes.

- 1st column: variable names
- 2nd column: variable entries
- 3rd column: variable units
- 4th column: example input format

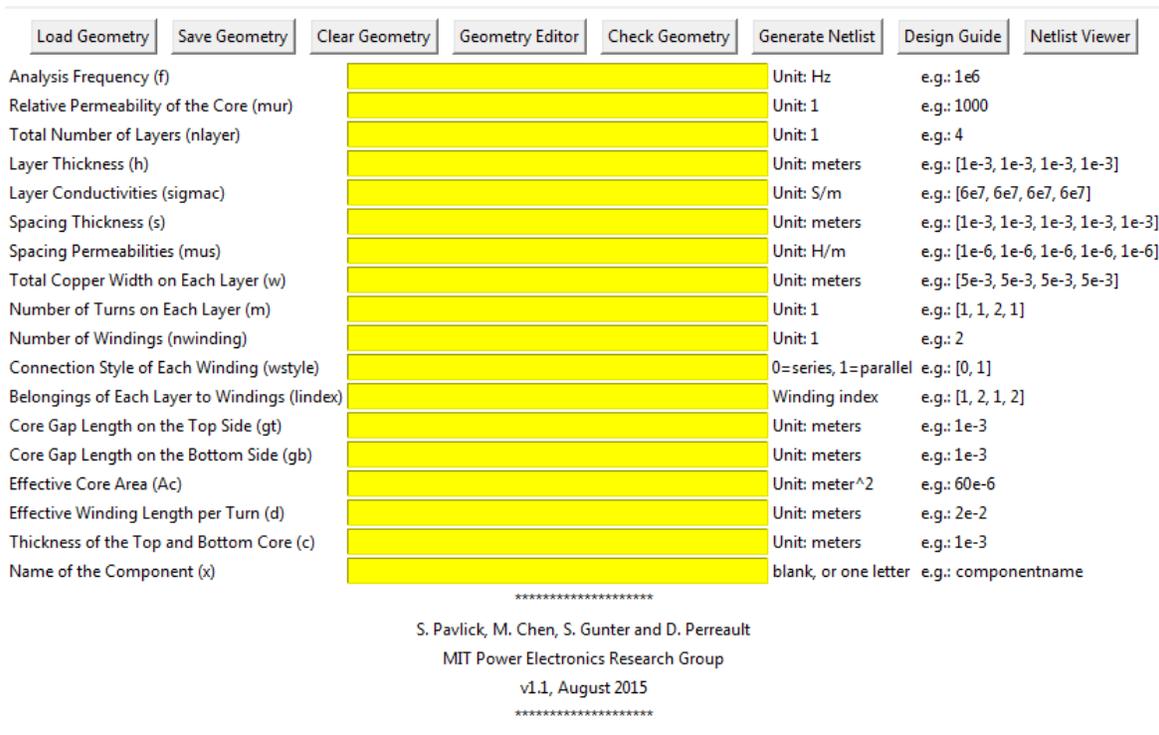


Fig. 4: User interface of M2Spice v1.1

2.2 EDIT GEOMETRY

One can manually type in the variables in the entries directly. Alternatively, one can click on the “Geometry Editor” button and open a separate dialog as shown in Fig. 5. The “Geometry Editor” allows long variables to be easily edited. Once the editing is finished, the “Forward Geometry” button will feed the variables into the main UI of M2Spice. Users can also save the geometry as a separate .txt file for future use by clicking the “Save Geometry” button.

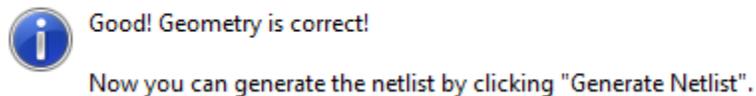
By clicking the “Load Geometry” button, a saved geometry .txt file can be automatically loaded into both the main UI, and the UI of the Geometry Editor. The software will fill in the variables one by one and report an error if any variable is missing.



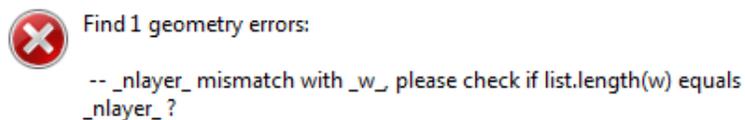
Fig. 5: Geometry Editor

2.3 CHECK GEOMETRY

Since the formats of multiple variables need to be matched, M2Spice is embedded with a function to check the format of the geometry before it is processed. This can be done by clicking the “Check Geometry” button. If the formats of the geometry information are matched, the software will report:



Otherwise, the software will report the corresponding error and provide some debugging hint, such as:



This error message indicates that the length of the variable *w* does not match with *n* layer. One will need to check that the length of variable *w* (Core Window Width) matches with *n*layer (Total Number of Layers).

2.4 GENERATE NETLIST

Once the geometry information is checked and valid, the netlist is ready to be generated. After clicking on the “Generate Netlist” button and choosing a file name, the user can select whether to view the netlist immediately through the embedded netlist viewer, or skip this step and open the netlist from another text editor.

The “Netlist Viewer” allows the generated netlist to be viewed and edited. The netlist has the following structure.

- 1) **Descriptive sentences.** The first few lines are commented with asteroids (*). These are descriptive sentences which described the planar structure. These are comments for design reference, and are not a part of the SPICE netlist.

```
* The name of the component is: _ex1.
* This planar structure has 4 windings and 8 layers.
* This netlist is generated for 500000.0 Hz operation.
* >>>> Winding 1 >>>>
* -> All layers in winding 1 are Series Connected;
* -> Its external Port Name: PortP1_ex1, PortN1_ex1
* --> Includes Layer 1
* ---> h 35.00um, w 13.50mm, turns 2, s above 1.82mm, s below 0.20mm
* --> Includes Layer 3
* ---> h 35.00um, w 13.50mm, turns 2, s above 0.20mm, s below 0.20mm
* -> Winding 1 has 4 total turns;
```

- 2) **Netlists for each layer.** The SPICE netlist starts with n paragraphs of netlist sections describing the n layers and the spacings between them.

```
*NetList for Layer 1
Le1_ex1 N1_ex1 P1_ex1 4 Rser=1f
Li1_ex1 G_ex1 Md1_ex1 1 Rser=1f
Lg1_ex1 Mg1_ex1 Md1_ex1 -67.26p Rser=1f
Rg1_ex1 Mc1_ex1 Mg1_ex1 4517.81u
Rt1_ex1 Mc1_ex1 Mt1_ex1 14.82u
Rb1_ex1 Mb1_ex1 Mc1_ex1 14.82u
Lt1_ex1 T1_ex1 Mt1_ex1 201.85p Rser=1f
Lb1_ex1 Mb1_ex1 B1_ex1 201.85p Rser=1f
Ls1_ex1 B1_ex1 T2_ex1 2.31n Rser=1f
K1_ex1 Le1_ex1 Li1_ex1 1
```

- 3) **Netlists for the magnetic core.** The following few lines are the netlist describing the magnetic core.

```
*NetList for Top and Bottom Ferrites, as well as the First Spacing on Top Side
Lft_ex1 T0_ex1 G_ex1 10958.79n Rser=1f
Lfb_ex1 T9_ex1 G_ex1 48743.74n Rser=1f
Ls0_ex1 T1_ex1 T0_ex1 21.01n Rser=1f
```

- 4) **Netlists for the Interconnects.** Finally, there are a few lines describing the interconnects. A few layers are connected in series to formulate the series layers. A few layers are connected in parallel to formulate the parallel layers. The interconnect wires are modeled as resistors with 1f ohm resistance. If needed, these values can be modified to capture the parasitic inductances.

```
* -> Winding 1 is Series Connected
* -->Include layer 1
* -->Include layer 3
```

```

RexP1_ex1 PortP1_ex1 P1_ex1 1f
RexN3_ex1 PortN1_ex1 N3_ex1 1f
RexM1_ex1 N1_ex1 P3_ex1 1f

* -> Winding 2 is Series Connected
* -->Include layer 2
* -->Include layer 4
RexP2_ex1 PortP2_ex1 P2_ex1 1f
RexN4_ex1 PortN2_ex1 N4_ex1 1f
RexM2_ex1 N2_ex1 P4_ex1 1f

* -> Winding 3 is Parallel Connected
* -->Include layer 5
RexP5_ex1 PortP3_ex1 P5_ex1 1f
RexN5_ex1 PortN3_ex1 N5_ex1 1f
* -->Include layer 7
RexP7_ex1 PortP3_ex1 P7_ex1 1f
RexN7_ex1 PortN3_ex1 N7_ex1 1f

* -> Winding 4 is Series Connected
* -->Include layer 6
* -->Include layer 8
RexP6_ex1 PortP4_ex1 P6_ex1 1f
RexN8_ex1 PortN4_ex1 N8_ex1 1f
RexM6_ex1 N6_ex1 P8_ex1 1f

```

- 5) **Ground for the magnetic domain.** There is an effective ground in the magnetic domain. This effective ground is tied to the circuit ground with a 1G ohm resistor.

```

*One 1G ohm resistor is used to ground the floating domain
Rgnd_example G_example 0 1G

```

3 LTSPICE SIMULATIONS

The generated netlist file can be utilized in SPICE simulations. Fig. 6 shows the schematic of the simulation setup. The two primary windings are driven by two different voltage sources. The two secondary windings are loaded by two resistors with different resistances. We use LTSpice simulation software to illustrate the current distribution in the four windings.

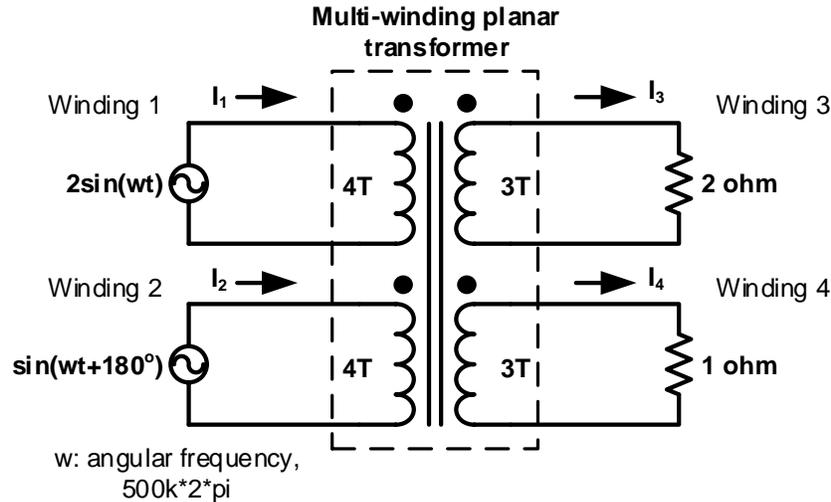


Fig. 6: Simulation setup of the example four winding transformer

Fig. 7 shows the screenshot of the LTSpice simulation schematic. The transformer netlist was copy-and-pasted into the schematic using the “.op” operation. The four port names (PortP1_ex1, PortN1_ex1, etc...) can be found in the commentary section of the netlist. A few “1F” resistors are included to avoid node naming issues (e.g., unintentional renaming of nodes).

It is recommended to use the “Alternate” simulation solver in LTSpice. (Tools/Control Panel/SPICE/Solver).

3.1 TIME DOMAIN SIMULATION

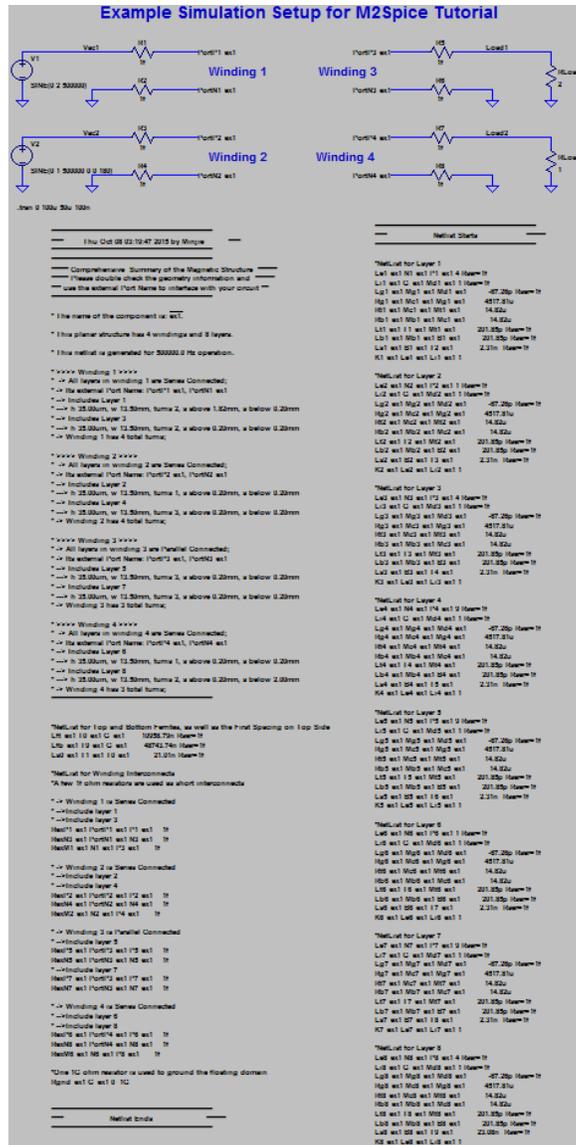
The simulation can be performed in time domain by adding a transient analysis command such as

```
.tran 0 100u 50u 100n
```

into the schematic. In this way, one can use LTSpice to see performance in the time domain and visualize the current distribution in the four windings. The time domain simulation results are shown in Fig. 8.

More importantly, the M2Spice can be used to visualize the current distribution within each layer. The current carried by each of the “Lg” inductors in the circuit netlist is the current flowing in each layer. By right clicking on the waveform panel in LTSpice and selecting “Add Trace” (or by pressing ctrl+A), one can then select the corresponding waveforms as shown in Fig. 9, and the current distribution in the eight layers can be visualized as shown in Fig. 10.

This information is crucial when designing planar magnetics. By knowing the RMS current values and their relative phase shifts, one can make informed decisions about the number and placement of layers.



(a)



(b)

Fig.7: Screenshot of the LTspice (a) full schematic and (b) close-up of port connections.

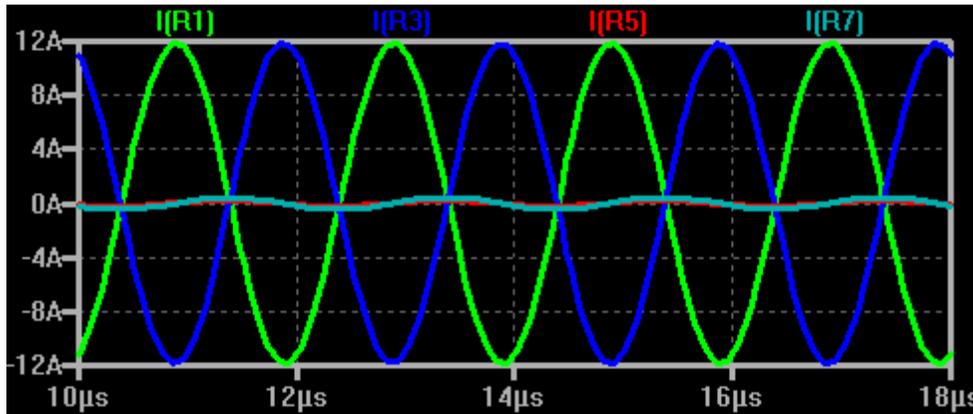


Fig. 8: Screenshot of the time domain simulation results showing the current waveforms into each of the transformer windings. I(R1) is I_1 , I(R3) is I_2 , I(R5) is I_3 , and I(R7) is I_4 from Fig. 6

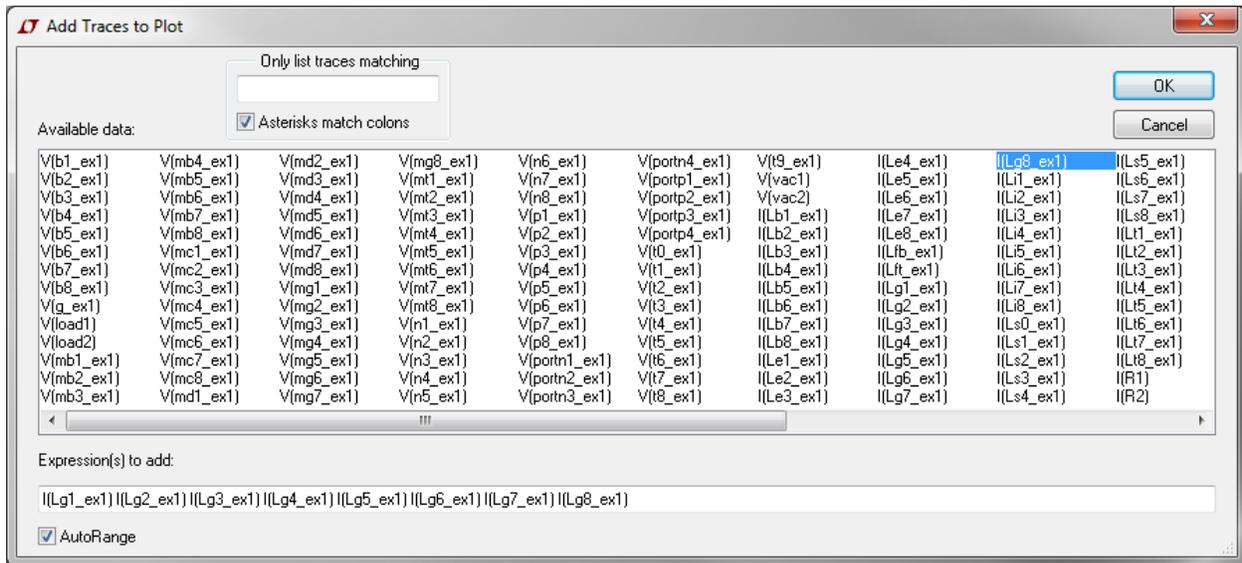


Fig. 9: Selecting the waveforms that need to be displayed in LTSpice.

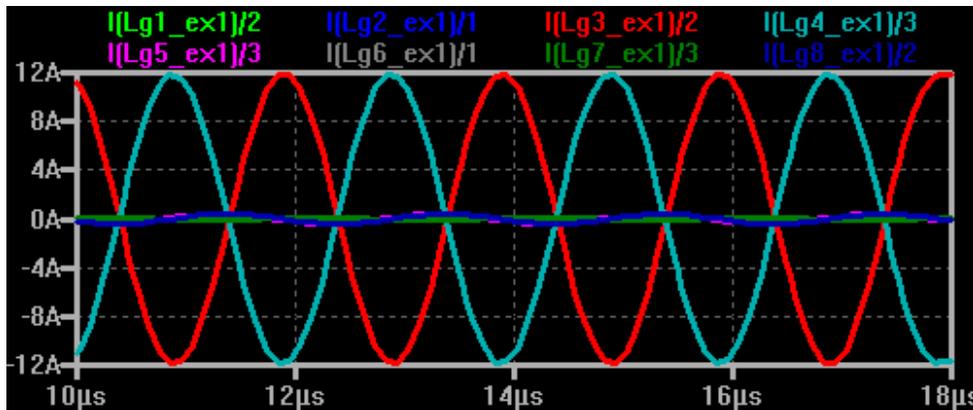


Fig. 10: Current distribution in the eight layers. Note that the currents are divided by the number of turns in each layer to provide the current in the physical component. Certain currents are identical due to their series connection.

3.2 FREQUENCY DOMAIN SIMULATION

LTspice can also perform frequency domain simulations. Here we use SPICE simulation to measure the port input impedance. Fig. 11 shows the schematic of the simulation setup. In the eight layer planar magnetic structure, we measure the input impedance of winding 1 when winding 2 is open-circuited. Winding 1 is connected to a unity sinusoidal voltage source with the desired frequency as shown in Figure 12. We measure the current I_1 to calculate the input impedance of winding 1.

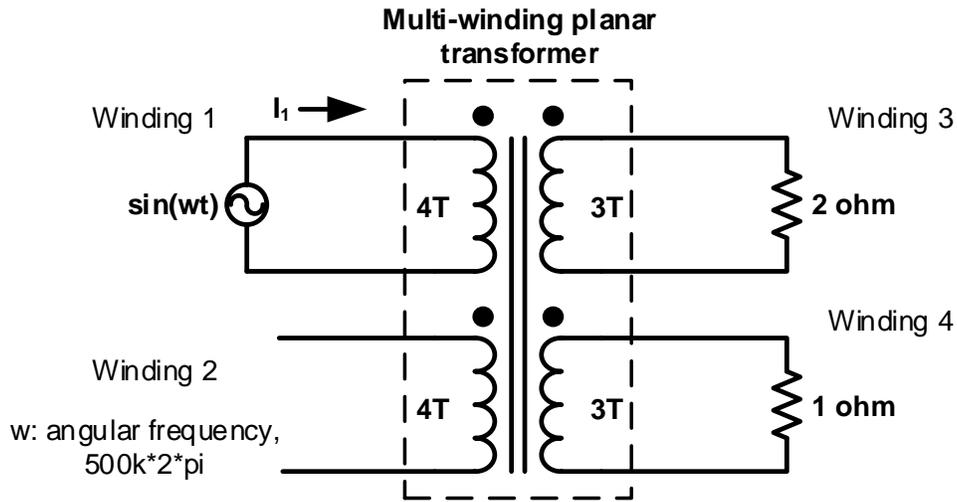


Fig. 11: Measuring the port input impedance through frequency domain simulations.

Example Frequency Domain Simulation using Netlists generated by M2Spice



Fig.12: Screenshot of the LTspice port connections.

In frequency domain simulation, the simulation command needs to be modified to

.ac list 500000

This performs the frequency domain analysis for a single frequency. The current flowing through R1, $I(R1)$, can be used to calculate the effective input impedance (magnitude and phase) of winding 1 as shown in Fig. 13.

I(Rexp6_ex1):	mag: 0.643753	phase: 156.425°	device_current
I(Rexn7_ex1):	mag: 0.233815	phase: -175.877°	device_current
I(Rexp7_ex1):	mag: 0.233817	phase: 4.12158°	device_current
I(Rexn5_ex1):	mag: 0.552665	phase: -9.49449°	device_current
I(Rexp5_ex1):	mag: 0.552654	phase: 170.505°	device_current
I(Rexm2_ex1):	mag: 0	phase: 0°	device_current
I(Rexn4_ex1):	mag: 3.11226e-019	phase: 138.313°	device_current
I(Rexp2_ex1):	mag: 0	phase: 0°	device_current
I(Rexm1_ex1):	mag: 0.730518	phase: -22.2139°	device_current
I(Rexn3_ex1):	mag: 0.73053	phase: 157.786°	device_current
I(Rexp1_ex1):	mag: 0.730543	phase: -22.2131°	device_current
I(Rload2):	mag: 0.643766	phase: -23.5756°	device_current
I(Rload1):	mag: 0.330046	phase: -19.096°	device_current
I(R8):	mag: 0.643727	phase: -23.5756°	device_current
I(R7):	mag: 0.643753	phase: -23.5752°	device_current
I(R6):	mag: 0.330046	phase: -19.096°	device_current
I(R5):	mag: 0.330033	phase: -19.0964°	device_current
I(R4):	mag: 3.11226e-019	phase: -41.6871°	device_current
I(R3):	mag: 0	phase: 0°	device_current
I(R2):	mag: 0.73053	phase: -22.2136°	device_current
I(R1):	mag: 0.730493	phase: -22.2148°	device_current
I(V1):	mag: 0.73053	phase: 157.786°	device_current

Fig. 13: Frequency domain simulation results that can be used to calculate the port impedance.