2016 IEEE Applied Power Electronics Conference (APEC '16)

Capacitively-Aided Switching Technique for High-Frequency Isolated Bus Converters

Seungbum Lim, Alex J. Hanson, Juan A. Santiago-González, and David J. Perreault
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139-4307
Email: sblim@mit.edu

***Abstract*—This paper presents a new capacitively-aided zero voltage switching (ZVS) technique for isolated bus converters. The proposed technique helps to achieve ZVS conditions for both inverter and rectifier switches with the aid of magnetizing current of the transformer and capacitors interconnecting primary and secondary side switching nodes. With the proposed topology, the ZVS conditions for inverter and rectifier switches occur at the same time, and (ideally) maintain constant required dead time independent of the load level of the converter. These features are particularly advantageous especially for designs operating at high frequencies where timing control becomes critical. The proposed approach is demonstrated in a 1.4 MHz prototype converter which operates from 36 Vdc and supplies a 12 Vdc output load (i.e., fixed input voltage and fixed voltage transformation ratio, 3 : 1) at a 36 W rating. Experimental results show ZVS operation of all devices independent of the load level, and the prototype converter achieves 94 % peak efficiency with 300 W / in^3 power density.**

I. Introduction

Advances in power distribution systems (e.g., for telecommunications, data centers, and dc distribution systems) have been driven by a demand for higher efficiency, smaller volume, and lower cost. The intermediate-bus architecture, which incorporates a "bus converter" stage (or "dc transformer") that provides isolation and voltage transformation but without the regulation capability, has become popular due to its advantages (e.g., system efficiency and power density) [1]–[4]. Moreover, there are many other power conversion architectures and applications in which the isolation and transformation function of the power electronics can be separated from any required regulation capability [2], [5]–[10]. Practical applications of such systems depend upon bus converters having small size, low loss, and high performance.

Recent advances in gallium-nitride (GaN) transistor technology facilitate higher frequency operation with improved transistor figures of merit (e.g., $R_{on} \times C_{oss}$ [11] or $\sqrt{R_{on} \times Q_g}$ [12], [13]), such that low-loss soft switching can be realized at high frequency [2], [14]–[19]. Furthermore, as shown in the study [20], increasing operating frequencies into the multi-MHz range can yield high performance in terms of the capabilities of available magnetic materials. However, leveraging the achievable performance of these devices and materials requires topologies and control techniques to address the challenging constraints of control timing (e.g., for ZVS switching and dead time) as frequency increases. This paper explores a topology and switching technique suitable for bus converters at multi-MHz frequencies.

There are many resonant converter topologies processing (quasi) sinusoidal waveforms that may be useful for isolated bus conversion (e.g., series-resonant [21], parallel-resonant [22], and LLC [23]–[27]). Differences among these converters are based on how the resonant tank and transformer are configured and utilized. While many of these converters can be designed with diode-based rectifiers, synchronous rectifiers are often used to reduce diode conduction loss and achieve higher efficiency (e.g., [1], [28]). Control and driver circuitry are then needed to accurately adjust gate-source signals of the secondary-side (output side) transistors. There are many commercial control / driver ICs which are specifically designed for controlling the secondary-side transistors to behave like diodes using only information available on the secondary. These integrated circuits usually sense the drain-source voltage of the secondary switch and compare it with threshold voltages to control the switch gate-source voltage. However, these techniques tend not to work well at frequencies above 1 MHz, because parasitics (e.g., parasitic capacitance/inductance from PCB and switch) make it difficult to achieve the necessary switch timing using drain-source voltage measurements. In addition, fast (low propagation delay) comparators consume a lot of control power and there are limits on the achievable response speed of such comparators, especially at low overdrive of the comparator inputs. Consequently, there is significant difficulty in making this self-sensing synchronous rectification approach work well in the multi-MHz regime. Direct control of the secondary side switches (e.g., from the primary side) likewise becomes challenging for these topologies at high frequencies. Control timing (and its variation with operating condition) thus becomes an increasingly challenging problem as frequency increases for many conventional resonant converter topologies employing synchronous rectification.

An alternative to resonant topologies in the bus converter (or dc transformer) application is the dual-active-bridge (DAB) converter [28]. In this topology there is active control of the timing of the primary switches relative to the secondary switches (such that the secondary switches are not operated like diodes, but do achieve ZVS). In addition to ZVS operation of all of the switches, this topology has the advantage that, for fixed conversion ratio applications. One achieves

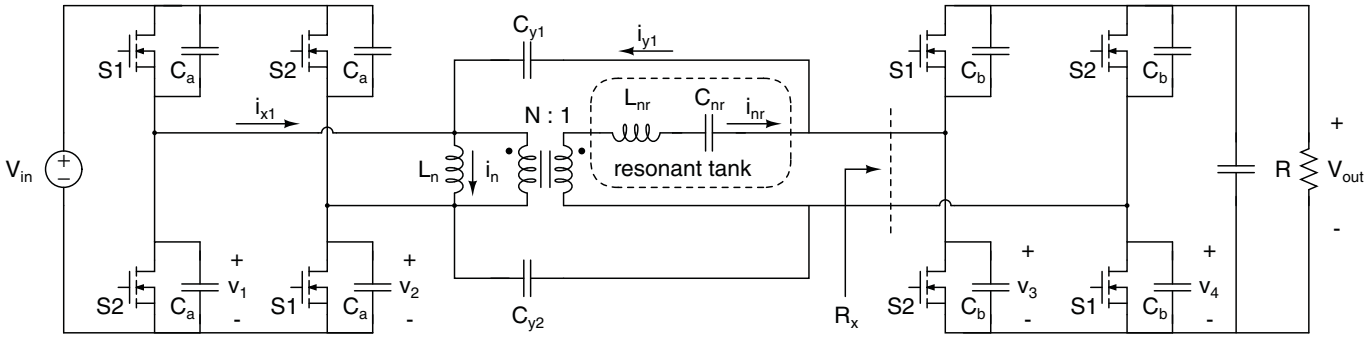

Fig. 1. The schematic shows the proposed isolated converter topology. It is designed with full-bridge inverter, transformer, resonant tank, full-bridge synchronous rectifier, and Y-rated capacitors interconnecting corresponding inverter and rectifier switch sets.

quasi-trapezoidal current waveforms that provide very low rms currents in the devices and transformer, yielding low conduction dissipation [29]. However, the driving signals need to be precisely controlled for all the switches, such that the DAB converter requires complex and accurate control circuitry with variable dead time, duty ratio, and phase shift (between inverter stage and rectifier stage) for various loads and input voltages. This complex control becomes increasingly difficult at high frequency and imposes heavy constraints on the achievable frequency, especially considering the timing delay and timing variability among signals crossing the isolation barrier. Overall, there is a difficulty in operating many conventional isolated converters with synchronous rectification at high frequency because of the complexities of achieving the necessary control timing among all of the switches when working across the isolation barrier. This highlights the need for new topologies and control approaches more suitable to this frequency range.

Here we propose a new ZVS technique applicable for unregulated isolated converters which addresses the challenge of maintaining ZVS operation with accurate switch timing in the MHz frequency range. Section II of the paper introduces the new bus converter topology and illustrates its operation, design considerations, and advantages. Section III of the paper demonstrates an implementation of the converter operating at 1.4 MHz and presents experimental results. Finally, in Section IV we conclude that the proposed topology can maintain high efficiency with simple control as operating frequency is increased into the high frequency regime.

II. Proposed Bus Converter Topology

The proposed converter is illustrated in Fig. 1. It is designed to act as a "dc transformer" in which the voltage conversion ratio is relatively fixed and no regulation capability is required. In our intended application the converter is used as a bus converter, in which input voltage is fixed in addition to conversion ratio, though it can operate well at variable input voltages within limitations constrained by device capacitance nonlinearities. The converter comprises a full-bridge inverter, transformer, resonant tank, full-bridge synchronous rectifier, and capacitors interconnecting primary and secondary side

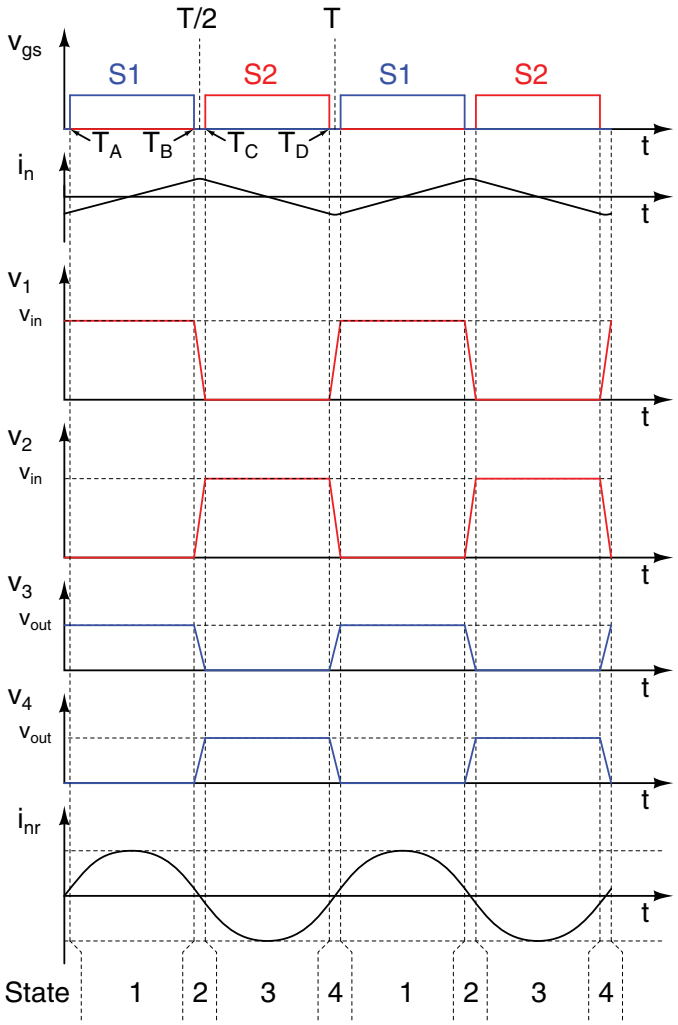

Fig. 2. The waveform describes the voltage and current of the proposed isolated converter topology shown in Fig. 1.

switching nodes. The capacitors C_{y1} and C_{y2} are implemented with Y-rated capacitors to meet isolation requirements.

The operation of the proposed converter topology naturally absorbs the leakage and magnetizing inductances of the trans-

former as well as the device and transformer capacitances, making it suitable for high-frequency operation. In considering the transformer parasitics, we utilize the cantilever model of the transformer, such that we only consider a single "leakage inductance" in addition to a "magnetizing inductance", and a "turns ratio" to characterize the transformer; these model components thus do not necessarily reflect the exact physical values (e.g., of the turns ratio), though we can directly map between this model and physical parameters [30].

As shown in Fig. 1, $\mathrm{C_a}$ and $\mathrm{C_b}$ are the output capacitances of the inverter and rectifier switches (plus any added capacitance), respectively, and $\mathrm{L_n}$ is the magnetizing inductance of the N:1 turns ratio transformer. For the selected operating frequency, the inductor $\mathrm{L_{nr}}$ and capacitor $\mathrm{C_{nr}}$ form a resonant tank, such that (ideally) only fundamental (first harmonic) frequency current flows through the resonant tank (i.e., $i_{nr} = \mathrm{I_{nr}}\, sin(2\,\pi\, f_{sw}\, t)$). In addition, all the switches at primary/secondary side are synchronized and controlled by either S1 or S2 gate signals as shown in Fig. 1.

A. Operation

Fig. 2 illustrates the ideal switch timing and operating waveforms of the proposed isolated bus converter topology. The resonant tank (composed of inductor $\mathrm{L_{nr}}$ and capacitor $\mathrm{C_{nr}}$) is tuned to the selected operating frequency, such that the current $\mathrm{i_{nr}}$ approximates a sinusoidal current as shown in Fig. 2. The converter operates at fixed frequency and all the switches are operated to have the same duty ratio with a fixed dead time as shown in Fig. 1 and Fig. 2.

To simplify the analysis, we assume 100% efficiency and small dead time between S1 and S2 signals such that no significant power is transferred through the interconnecting capacitors. With these assumptions, the input power (1) and output power (1) of the transformer are equal (2). The current flowing through the magnetizing inductor does not receive/send power through the transformer on average, so it drops out of the integral as shown in (3). Solving equations (1)–(3) show that the output voltage is simply V_{in} / N.

$$P_{in} = \frac{2}{T}\int_0^{\frac{T}{2}} V_{in}\left(\frac{I_{nr}}{N}\, sin\,(\omega t) + I_n(t)\right) dt = \frac{2V_{in}}{T}\int_0^{\frac{T}{2}} \frac{I_{nr}}{N}\, sin\,(\omega t)\, dt \quad (1)$$

$$P_{out} = \frac{2V_{out}}{T}\int I_{nr}\, sin\,(\omega t)\, dt \quad (2)$$

$$P_{in} = P_{out} \quad \Rightarrow \quad V_{out} = \frac{V_{in}}{N} \quad (3)$$

With the above assumptions, the converter cycles through four states as described below, with the polarity of the voltages and currents as illustrated in Fig. 1.

State 1 : $T_A < t < T_B$ — In this state, the S1 switches are turned on and S2 switches are turned off. $\mathrm{V_{in}}$ is applied across the transformer primary such that magnetizing current increases linearly. Voltages v_1, v_2, v_3, and v_4 are clamped to $\mathrm{V_{in}}$, 0, $\mathrm{V_{out}}$, and 0, respectively. The capacitors $\mathrm{C_{y1}}$ and $\mathrm{C_{y2}}$ do not conduct current because the voltages across them remain fixed.

State 2 : $T_B < t < T_C$ — State 2 starts as the S1 switches turn off under ZVS conditions using their output capacitances to snub the switch turn offs. During this dead time, the current through the resonant tank (approximately sinusoidal current) is in phase with the voltage applied to the transformer, so that current i_{nr} is close to zero for the short dead time (or, even considering non-zero instantaneous current, the average current of i_{nr} during the dead time is zero, so that i_{nr} current does not affect to voltage on v_3 and v_4 during the dead time). After the S1 switches turn off, the magnetizing current starts to decrease the voltage v_1, and also v_3 through $\mathrm{C_{y1}}$. Likewise, the magnetizing current charges the voltage of v_2 and v_4 via $\mathrm{C_{y2}}$. By selecting correct capacitances $\mathrm{C_{y1}}$ and $\mathrm{C_{y2}}$ with respect to the secondary-side switch output capacitances, the required dead times to achieve ZVS for the primary switches and secondary switches can be matched (this will be further described in section II-B). When the drain-source voltage of the S2 switches are discharged (close enough) to zero, the S2 switches are turned on with ZVS condition and the system enters state 3.

State 3 : $T_C < t < T_D$ — In this state, the S2 switches are turned on and S1 switches are turned off. Therefore, $-\mathrm{V_{in}}$ is applied across the primary magnetizing inductance of the transformer, such that magnetizing current decreases monotonically.

State 4 : $T_D < t < T + T_A$ — All the S2 switches turn off with ZVS conditions with the aid of the transistor output capacitances snubbing the turn off. Then, similar to state 2 but with opposite polarity, utilizing the magnetizing current and capacitors $\mathrm{C_{y1}}$ and $\mathrm{C_{y2}}$, the drain-source voltages of the S1 switches decrease and create an opportunity for ZVS turn-on of the S1 devices. When the S1 switches turn on, state 1 is entered and the cycle repeats.

The equations for magnetizing and resonant tank currents are as follows (dead time between S1 and S2 is ignored here for simplicity).

$$i_n = \begin{cases} \frac{V_{in}}{L_n}\,(t - \frac{T}{4}) & 0 < t < \frac{T}{2} \\ -\frac{V_{in}}{L_n}\,(t - \frac{3T}{4}) & \frac{T}{2} < t < T \end{cases} \quad (4)$$

$$i_{nr} = I_{nr}\ sin\,(2\pi f_{sw}\, t) = \frac{\pi}{2}\ \frac{V_{out}}{R}\ sin\,(2\pi f_{sw}\, t) \quad (5)$$

B. Design parameters

For the desired operation as illustrated above, the Y-rated capacitors need to be selected properly to achieve ZVS conditions for the secondary-side switches. During dead time (when switches S1 and S2 are all off), the current through the switches and resonant tank is close to zero. Then, the magnetizing current i_n flows through inverter side output

capacitors (C_a), Y-rated capacitors (C_{y1} and C_{y2}), and rectifier side output capacitors (C_b). The current and voltage relations during the dead time (state 2 and 4) are as follows:

$$i_n(t) \;=\; i_{x1}(t) \;+\; i_{y1}(t) \tag{6}$$

$$i_{x1}(t) \;=\; -\,2C_a\frac{dv_1}{dt} \tag{7}$$

$$i_{y1}(t) \;=\; C_{y1}\,\frac{d(v_3-v_1)}{dt} \;=\; -\,2C_b\,\frac{dv_3}{dt} \tag{8}$$

To achieve ZVS conditions for inverter switches and rectifier switches at the same time, the value of capacitors C_{y1} and C_{y2} can be selected based on the relations in (8). If the converter achieves ZVS for both primary and secondary switches during the dead time, the voltages of v_1 and v_3 at the beginning and the end of the dead time at state 2 are as shown in Fig. 2 and equations (9) and (10).

$$v_1(T_B) = V_{in}\,, \quad v_3(T_B) = V_{out} = \frac{V_{in}}{N} \tag{9}$$

$$v_1(T_C) = 0\,, \qquad v_3(T_C) = 0 \tag{10}$$

Integrating eq. (8) over the dead time (i.e., from T_B to T_C), we can calculate the desired capacitance for C_{y1} and C_{y2} as illustrated in (11)–(13).

$$\int_{T_B}^{T_C} i_{y1}(t)dt \;=\; C_{y1}\,(v_3(t)-v_1(t))\;|\,_{T_B}^{T_C} \tag{11}$$

$$\;=\; -\,2C_b(v_3(t))\;|\,_{T_B}^{T_C} \tag{12}$$

$$\Rightarrow \quad C_{y1} \;=\; \frac{2C_b}{N-1} \tag{13}$$

This illustrates that the values of the interconnecting capacitors C_y should be selected based on the effective capacitance C_b and turns ratio of the transformer. Then the ratio between C_y and C_b makes the required ZVS dead time for inverter switches (v_1) and rectifier switches (v_3) the same. It should be noted that if the switch capacitors are significantly nonlinear, we may need to select an effective value C_b. Also, the range of input voltages (and scaled output voltages) that the converter can accommodate with ZVS may be limited by how much effective capacitance Cb changes with variations in output voltage.

Furthermore, we can estimate the dead time for the converter from the equations above. If we treat the magnetizing current as almost constant during the relatively short dead time, then we can regard the magnetizing current during dead time (i.e., states 2 and 4) as follows:

$$i_n(T_B) \;\simeq\; i_n(T_C) \;\simeq\; i_n(T/2) \;\simeq\; \frac{V_{in}T}{4L_n} \tag{14}$$

Then, the required dead time can be calculated from (6)-(8), (13), and (14) as follows.

$$\int_{T_B}^{T_C} i_n(t)dt \;=\; -\,2C_a v_1(t)\,|\,_{T_B}^{T_C} \;-\; 2C_b v_3(t)\,|\,_{T_B}^{T_C}$$

$$=\; 2\,C_a V_{in} \;+\; 2\,C_b\,\frac{V_{in}}{N} \tag{15}$$

$$\Rightarrow \quad \frac{V_{in}}{L_n}\,\frac{T}{4}\,(T_C-T_B) \;=\; 2\,C_a\,V_{in} \;+\; \frac{2\,C_b\,V_{in}}{N}$$

$$\Rightarrow \quad T_C - T_B \;=\; DeadTime \;=\; \frac{8L_n(C_a+C_b/N)}{T} \tag{16}$$

The dead time between high and low side switches can therefore be easily calculated for the selected converter designs and it is independent of load level. However, it should be noted that both L_n and T should be selected together to keep the magnetizing current in a reasonable range. That is, the magnetizing current needs to be large enough to fully discharge/charge capacitors (C_a and C_b) for ZVS with a modest dead time duration, but is also constrained not to be too high to reduce conduction loss and to get high efficiency.

Another design consideration is selecting the quality factor (Q) of the resonant tank of the converter. For the series-resonant tank structure used on secondary side, the Q is defined as shown in (17), where R_x is the effective impedance looking into the synchronous rectifier from the resonant tank as illustrated in Fig. 1 and defined by (18) [21].

$$Q \;=\; \frac{Z_{Lr}}{R_x} \;=\; \frac{Z_{Cr}}{R_x} \;=\; \frac{\omega L_r}{R_x} \;=\; \frac{1}{\omega C_r R_x} \tag{17}$$

$$R_x \;=\; \frac{8}{\pi^2}\;R \tag{18}$$

With a selected Q the voltage across the resonant capacitor is as follows.

$$v_{Cr} \;=\; \frac{1}{C_{nr}}\int i_{nr}(t)\,dt \;=\; \frac{1}{C_{nr}}\int \frac{\pi}{2}\,\frac{V_{out}}{R}\,sin(\omega_{sw}t)\,dt$$

$$=\; -\frac{\pi}{2}\frac{V_{out}}{C_{nr}\;\omega_{sw}\;R}\;cos\,(\omega_{sw}\,t)$$

$$=\; -\frac{4}{\pi}\,Q\,V_{out}\;cos\,(\omega_{sw}\,t) \tag{19}$$

Larger Q values give ideal sinusoidal currents (at fundamental frequency), but require larger resonant inductances (L_{nr}) and larger voltage rating of the resonant capacitors (C_{nr}) as described in (17) and (19), and consequently higher loss.

To keep the resonant components physically small, especially L_{nr} so that it can be replaced by the leakage inductance of the transformer, we prefer a low-Q resonant tank if possible. It turns out that since the voltage applied to the transformer is an odd waveform, even a very low quality factor resonant tank does not alter the basic operation of the converter as long as the resonant tank current is small and crossing zero during the dead time. From numerous simulations of the proposed approach, it is found that the converter can maintain good operation with Q as low as 0.1 at full load (and so is effective

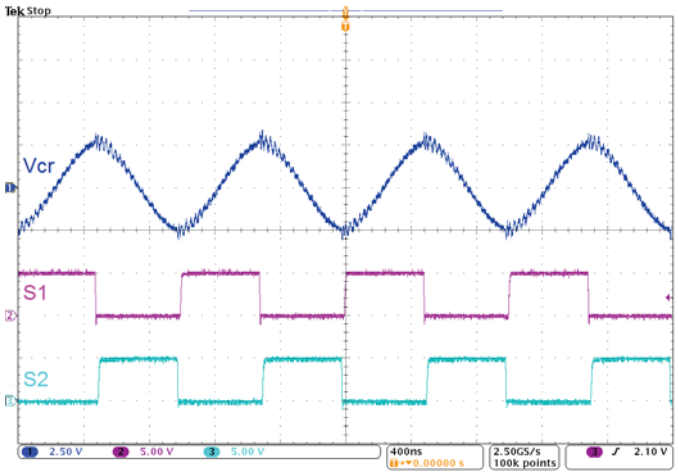

Fig. 3. The figure shows the waveform of the prototype converter when the resonant tank is tuned at operating frequency. ch1 shows the voltage across the resonant capacitor (2.5 V/div), ch2 and ch3 show the gate-source signal for S1 and S2 switches (5 V/div). The resonant tank can be simply tuned by measuring the phase of the resonant capacitors referenced to the control signals.

even at light loads). In our designs, we chose Q values between 0.1 and 1, and tuned the resonant tank as described in section III-A.

C. Advantage

The proposed isolated bus converter has several advantages over conventional topologies at high frequency. The first advantage is reliably achieving ZVS for the rectifier switches, even at high frequency. This made possible by the inclusion of the Y-rated capacitors interconnecting primary and secondary switches. Compared to many conventional resonant converters (which do not obtain ZVS operation for the rectifier stage), the ZVS capabilities for the proposed topology offers high efficiency at high frequency operation.

Secondly, the switch control circuitry and timing are greatly simplified because the ZVS conditions happen simultaneously for both inverter switches and rectifier switches independent of the load level. This advantage originates from the characteristic of the proposed converter which completely splits the function of different current components: The first component (resonant tank current, i_{nr}) is used to deliver power through the transformer, while a second component (magnetizing current, i_n) is for achieving ZVS.

Because the resonant tank is tuned at the operating frequency and thus flows sinusoidal current in phase with the control signals, the power delivering current (i_{nr}) becomes close to zero during the dead time, such that it ideally does not affect the zero-voltage switching conditions of the converter; instead, when the load level changes, only the amplitude of the power delivering current varies. On the other hand, magnetizing current does not deliver power from input voltage to output voltage, instead it can be used to achieve ZVS for primary and secondary switches. For a given input voltage at a certain operating frequency, the magnetizing current waveform is always the same independent of the load current, such that the same dead time is expected (and the dead time is also maintained as voltage levels vary as long as the capacitors are linear). Therefore, even though the load level changes, the converter always achieves ZVS conditions.

Once the switch components, transformer, and specifications of the converter are decided, the switch driving signals can be specified to have dead time as shown in (16). The same switch driving signals, then, can be used for various load levels while

TABLE I
SPECIFICATIONS AND COMPONENTS OF THE PROTOTYPE CONVERTER

Specification	
Input Voltage	36 Vdc
Output Voltage	12 Vdc
Output Power	up to 36 W
Switch and Driver IC	
Inverter	GaN switch EPC 2014C Coss $\simeq$ 150 pF
Rectifier	GaN switch EPC 2015C Coss $\simeq$ 700 pF
Driver IC	LM5113 half-bridge driver, TI
Y-rated capacitors	
C_{y1}, C_{y2}	680 pF Y3 X7R 250 Vac (rating) and 1500 Vac (withstand), Johanson Dielectrics
Transformer	
Core	Ferroxcube 3F45 EQ13 with 0.28 mm gap
Number of Turns	6 : 2 (i.e, N=3)
Winding	Planar structure with 62 mil thickness PCB 12 layers of 2 oz copper
L_N	5.8 μH (measured from primary side)
L_{nr}	60 nH (estimated)
C_{nr}	0.22 μF C0G/NPO 50V, TDK
Control	
Microcontroller	TMS320F28035, TI
Switching Frequency	1.4 MHz
Dead time	16.66 ns

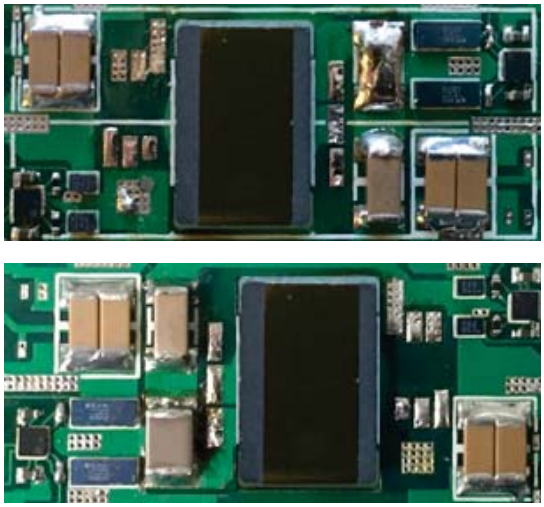

Fig. 4. The figure shows the top and bottom sides of implemented prototype converter. The specifications and components are presented in Table I. The main power stage converter has a size of 1.2 in $\times$ 0.6 in $\times$ 0.17 in, yielding a power density of 300 W/in^3.

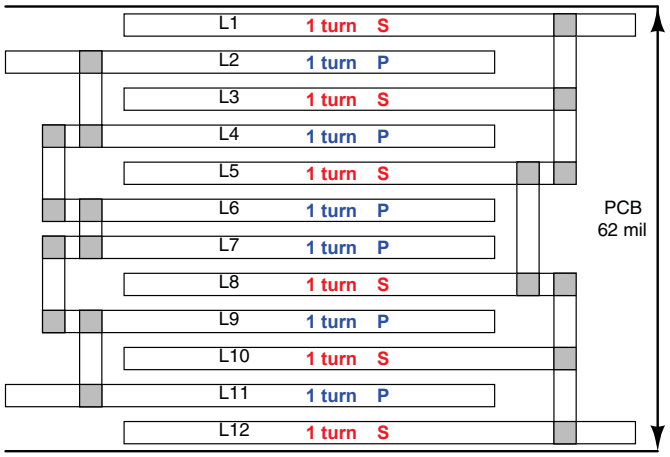

Fig. 5. The figure shows the layer configuration of the planar transformer of prototype converter as shown in Fig. 4. Primary side is wound 6 turns around core by connecting 6 layers of 1 turn/layer copper traces, and secondary side is wound 2 turns by connecting two of 3 parallel copper trace layers. The copper layers of planar transformer is then fully interleaved to reduce proximity effect.

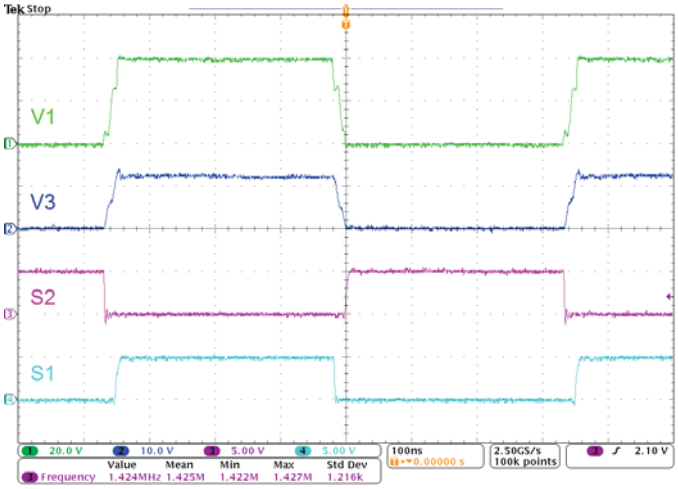

Fig. 6. The figure shows the waveform of the prototype converter when the converter operates from 36 Vdc to 12 Vdc supplying 36 W power. ch1 shows drain-source voltage for primary switch switch (v_1) (20 V/div), ch2 shows drain-source voltage for secondary switch (v_3) (10 V/div), and ch3 / ch4 show gate-source signal voltage for S2 and S1 switches respectively, (5 V/div). As can be seen, the primary and secondary switches achieve zero voltage switching at the same time using same control signals.

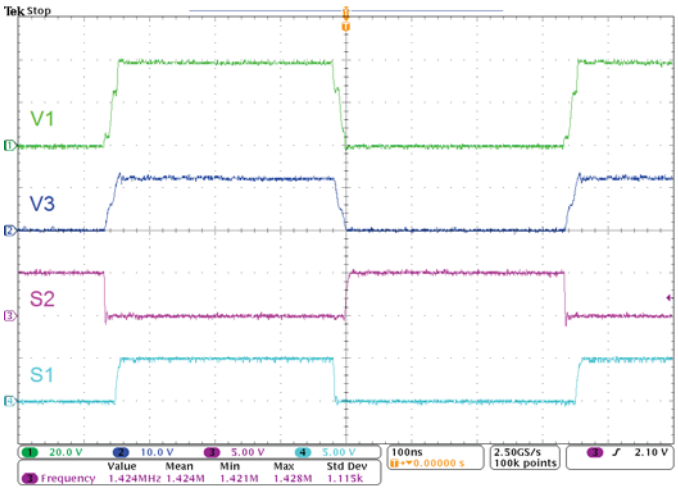

Fig. 7. The figure shows the waveform of the prototype converter when the converter operates from 36 Vdc to 12 Vdc supplying 18 W power. ch1 shows drain-source voltage for primary switch switch (v_1) (20 V/div), ch2 shows drain-source voltage for secondary switch (v_3) (10 V/div), and ch3 / ch4 show gate-source signal voltage for S2 and S1 switches respectively, (5 V/div). As can be seen, the primary and secondary switches still keep zero voltage switching condition at different power level even though the same control signals are used.

maintaining ZVS operation, such that the converter can operate efficiently for wide load range at high frequency without adding any extra control complexity.

III. Implementation and Experimental Results

In this section, we present an implementation of the proposed capacitively-aided isolated bus converter, and show the experimental results. The prototype converter is designed and tested from 36 Vdc input voltage to the 12 Vdc load supplying up to 36 W. (These specifications are drawn from the application in which the proposed bus converter will be used, but it should be emphasized that the topology's potential application is not limited to this voltage range, step-down ratio, or power level.)

A. Converter design and tuning

To operate the prototype converter as described in section II, the resonant tank of the converter needs to be tuned at the operating frequency. For the inductance (L_{nr}) of the resonant tank, one can use (the cantilever model) leakage inductance of the transformer or add external inductors for a higher inductance level, but since the leakage inductance is relatively small (i.e., up to 100 nH) compared to the magnetizing inductance, it is hard to measure the exact leakage inductance. As a consequence, it is hard to predict the exact resonant frequency for a selected resonant capacitance (C_{nr}). Thus, iterative tuning steps are necessary to match the resonant frequency and operating frequency in a given design.

Since measuring high frequency current is significantly hard, one simple strategy instead for this iterative tuning is using the voltage across the resonant capacitor. If we assume that sinusoidal current flows through the resonant tank, the voltage across the capacitor is sinusoidal as well, with 90 degree phase shift as shown in (5) and (19). For that reason, we can simply check the resonant tank by measuring the resonant capacitance voltage and checking the phase information compared to the gate-source signals. Then we can either tune the operating frequency of the converter or the resonant capacitance to get the right phase shift between voltage across resonant capacitor and gate-source voltages. To illustrate, Fig. 3 shows example measured waveforms of voltage across the resonant capacitor (ch1 – v_{cr}) and gate-source signals (ch2 – S1 and ch3 – S2) when the resonant tank is adjusted correctly.

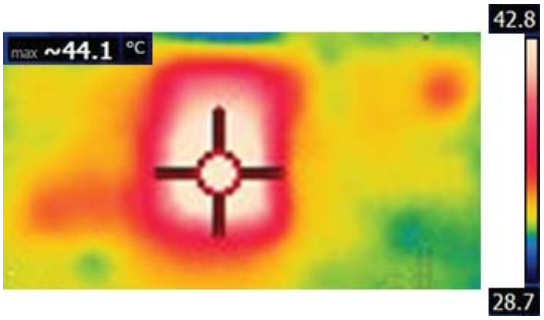

Fig. 8. This figure shows the captured image from infrared temperature camera when the converter operates from 36 Vdc to 12 Vdc at full power, 36 W. Comparing the temperature information to the prototype converter shown in Fig. 4, low loss dissipation is expected from the switch by achieving zero-voltage switching.

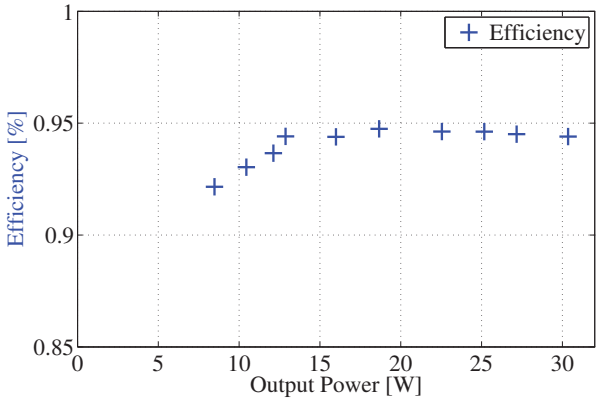

Fig. 9. The figure shows the measured efficiency of the prototype converter across the power range when the converter operates from 36 Vdc to 12 Vdc. The converter shows high efficiency up to 94 % for wide load range because of maintaining zero-voltage switching conditions independent of the load.

B. Prototype Converter Implementation

The selected components for the prototype converter are described in Table I. We used gallium-nitride (GaN) high-electron-mobility transistors (HEMT) driven by LM5113 half-bridge driver ICs. A microcontroller produces two switching signals (S1 and S2) at 1.4 MHz frequency with a 16.66 ns dead time between them, and controls the primary and secondary sides switches with these signals. We selected 680 pF, Y-rated capacitors as these are commercially available and close to the capacitance calculated from (13). (One could also add additional capacitance across the switches or transformer to get a precise match.)

We used 3F45 core material with an EQ13 core structure and distributed 0.28 mm gap (i.e., center post and side legs are all gapped by 0.28 mm), and designed the planar transformer with 5.8 μH magnetizing inductance utilizing 12 layers of 2 oz copper PCB traces. Six turns of copper trace (one turn per layer, and six layers connected in series) are wound on primary side, and two turns of trace coppers (one turn per layer, with two series-connected sets of three parallel copper layers) are fabricated on the 62 mil thickness PCB as illustrated in Fig. 5. As can be seen, primary and secondary windings are fully interleaved to reduce the ac resistance and conduction loss from proximity effect.

We used the leakage inductance of the transformer (approximately 60 nH) as the resonant inductance, and selected a 0.22 μF resonant tank capacitance through the iterative process described above (using a C0G/NPO capacitor with low dissipation factor). From the tuned resonant capacitance and the selected operating frequency, Q-value was set to be around 0.16 at full load. Fig. 4 shows the front and bottom side of the implemented prototype converter with the components described above.

C. Experimental Results

Fig. 6 illustrates the measured converter waveforms when the converter operates from 36 Vdc to 12 Vdc at 36 W load (1.4 MHz switching frequency). Channel 1 and 2 show the drain-source voltage for primary and secondary switches (i.e., v_1 and v_3 respectively), and channel 3 and 4 show the measured gate-source signal waveform for S2 and S1 switches. As can be seen from the measured waveform, the prototype converter presents nice ZVS operation for both primary and secondary switches at the same time. Likewise, Fig. 7 shows the measured waveforms when the converter operates at same input / output voltage but delivers 18 W power with same gate-source signals at the same switching frequency and same dead time. As can be seen, the converter maintains zero-voltage switching conditions independent of the load level as described in section II-C.

Fig. 8 shows a captured image from FLIR E6 infrared camera when the converter operates from 36 Vdc to 12 Vdc at 36 W load. Comparing the temperature information to the photograph of the prototype converter shown in Fig. 4, low temperature rise can be seen near the switches, which is expected since ZVS operation dissipates very little power in the switches. With the aid of zero-voltage switching operation and maintaining ZVS independent of the load level, the prototype converter shows up to 94 % efficiency over a wide load range as illustrated in Fig. 9, yielding a high power density of 300 W/in^3.

IV. Conclusion

A new capacitively-aided zero voltage switching (ZVS) technique for isolated bus converters is presented. The proposed technique has significant advantages for achieving ZVS condition and precise control timing for both the inverter and rectifier switches through the use of the Y-rated capacitors interconnecting the inverter and rectifier switch nodes. With properly selected interconnecting capacitors, the ZVS conditions for inverter and rectifier switches occur at the same time, and furthermore (ideally) the required dead time for ZVS operation becomes independent of the load of the converter. These advantages allow to use simple control circuit design, especially when the converter operates at high frequency. The proposed approach is implemented with a prototype converter which operates from 36 Vdc to 12 Vdc, up to 36 W load (i.e.,

a fixed input voltage and a fixed voltage transformation ratio of $3:1$). Experimental results show ZVS soft-switching and excellent efficiency for a wide load range, and the prototype converter achieves up to 94 % efficiency with a high 300 W/in^3 power density.

REFERENCES

[1] Y. Ren, M. Xu, J. Sun, and F. Lee, "A family of high power density unregulated bus converters," *Power Electronics, IEEE Transactions on*, vol. 20, no. 5, pp. 1045–1054, Sept 2005.

[2] S. Lim, J. Ranson, D. Otten, and D. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *Power Electronics, IEEE Transactions on*, vol. 30, no. 2, pp. 805–816, Feb 2015.

[3] R. Miftakhutdinov, "Power distribution architecture for tele- and data communication system based on new generation intermediate bus converter," in *Telecommunications Energy Conference, 2008. INTELEC 2008. IEEE 30th International*, Sept 2008, pp. 1–8.

[4] L. Mweene, C. Wright, and M. Schlecht, "A 1 kw 500 khz front-end converter for a distributed power supply system," *Power Electronics, IEEE Transactions on*, vol. 6, no. 3, pp. 398–407, Jul 1991.

[5] M. Chen, K. K. Afridi, S. Chakraborty, and D. J. Perreault, "A high-power-density wide-input-voltage-range isolated dc-dc converter having a multitrack architecture," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 2017–2026.

[6] P. Yeaman and E. Oliveira, "A high efficiency high density voltage regulator design providing vr 12.0 compliant power to a microprocessor directly from a 48v input," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 410–414.

[7] M. Salato and U. Ghisla, "Optimal power electronic architectures for dc distribution in datacenters," in *DC Microgrids (ICDCM), 2015 IEEE First International Conference on*, June 2015, pp. 245–250.

[8] M. Salato, "Datacenter power architecture: Iba versus fpa," in *Telecommunications Energy Conference (INTELEC), 2011 IEEE 33rd International*, Oct 2011, pp. 1–4.

[9] R. Farrington and M. Schlecht, "Intermediate bus architecture with a quasi-regulated bus converter," US Patent 7,787,261, 2010.

[10] M. Schlecht, "High efficiency power converter," US Patent 7,269,034, 2007.

[11] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc-dc power conversion," *Power Electronics, IEEE Transactions on*, vol. 21, no. 2, pp. 380–393, March 2006.

[12] B. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *Electron Device Letters, IEEE*, vol. 10, no. 10, pp. 455–457, Oct 1989.

[13] A. Huang, "New unipolar switching power device figures of merit," *Electron Device Letters, IEEE*, vol. 25, no. 5, pp. 298–301, May 2004.

[14] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture for an LED driver circuit," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, Mar. 2013, pp. 854–861.

[15] S. Lim, D. Otten, and D. Perreault, "Power conversion architecture for grid interface at high switching frequency," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, Mar. 2014, pp. 1838–1845.

[16] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, Feb 2009, pp. 1–14.

[17] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High-frequency pwm buck converters using gan-on-sic hemts," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2462–2473, May 2014.

[18] L. Xue, Z. Shen, D. Boroyevich, and P. Mattavelli, "Gan-based high frequency totem-pole bridgeless pfc design with digital implementation," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 759–766.

[19] B. Macy, Y. Lei, and R. Pilawa-Podgurski, "A 1.2 mhz, 25 v to 100 v gan-based resonant dickson switched-capacitor converter with 1011 w/in3 (61.7 kw/l) power density," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 1472–1478.

[20] A. J. Hanson, J. A. Belk, S. Lim, D. J. Perreault, and C. R. Sullivan, "Measurements and performance factor comparisons of magnetic materials at high frequency," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 5657–5666.

[21] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *Power Electronics, IEEE Transactions on*, vol. 3, no. 2, pp. 174–182, Apr 1988.

[22] V. Vorperian, "Approximate small-signal analysis of the series and the parallel resonant converters," *Power Electronics, IEEE Transactions on*, vol. 4, no. 1, pp. 15–24, Jan 1989.

[23] B. Yang, F. Lee, A. Zhang, and G. Huang, "Llc resonant converter for front end dc/dc conversion," in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, vol. 2, 2002, pp. 1108–1112 vol.2.

[24] D. Fu, Y. Liu, F. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in llc resonant converters," *Power Electronics, IEEE Transactions on*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[25] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series-parallel resonant (llc) dc-dc converter," *Industrial Electronics, IEEE Transactions on*, vol. 58, no. 1, pp. 289–297, Jan 2011.

[26] J. Zhang, J. Wang, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in llc resonant converter," *Power Electronics, IEEE Transactions on*, vol. 27, no. 11, pp. 4549–4561, Nov 2012.

[27] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth locked loop (pwll) for automatic resonant frequency tracking in llc dc-dc transformer (llc -dcx)," *Power Electronics, IEEE Transactions on*, vol. 28, no. 4, pp. 1862–1869, April 2013.

[28] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *Power Electronics, IEEE Transactions on*, vol. 28, no. 8, pp. 3931–3940, Aug 2013.

[29] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *Industry Applications, IEEE Transactions on*, vol. 27, no. 1, pp. 63–73, Jan 1991.

[30] R. Erickson and D. Maksimovic, "A multiple-winding magnetics model having directly measurable parameters," in *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE*, vol. 2, May 1998, pp. 1472–1478 vol.2.