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A Soft-Switched High Frequency Converter for Wide Voltage and Power Ranges

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***Abstract*—Power converters requiring wide voltage and power ranges (including power factor correction converters) are difficult to effectively implement with soft switching at high frequencies, limiting their density and/or efficiency. We propose a soft-switched converter that can operate at HF (3–30 MHz) across wide input voltage and power ranges. A prototype converter experimentally achieves zero voltage switching in the MHz regime and outputs 400 Vdc across input voltages of 10–400 Vdc and output powers of 100–400 W. This converter will permit further miniaturization of grid-interface and other converters while still maintaining high efficiency.**

I. Introduction

The need for high performance power electronics with wide operating ranges is ubiquitous, especially in grid-connected power conversion. Few modern devices can be plugged directly into the ac grid, owing to the increased preponderance of dc loads, the replacement of passive loads with active electronics, and the spread of variable speed drives and other "smart" features for ac loads. The proliferation of such loads has also spurred regulation requiring that they do not pollute the source with reactive power, i.e. that they look substantially resistive to the grid. Power factor correction (PFC) converters that meet these requirements must therefore operate over much of the line cycle, an inherently wide input voltage range. This input voltage range becomes even wider if converters must operate with *universal input*, including grids with ac mains voltages from $85\,\mathrm{V_{rms}}$ up to $265\,\mathrm{V_{rms}}$ or nearly $400\,\mathrm{V}$ amplitude. Other applications like automotive and mass transportation, for different reasons, also demand converters which operate over wide voltage or power ranges.

Obtaining increased efficiency and miniaturization in such converters is limited, in large part, by difficulties in operating at high frequency. While individual components have proven capable[1] of achieving high performance well into the HF (3–30 MHz) and even VHF (30–300 MHz) ranges [1], [2], current circuits and architectures that achieve high performance at high frequencies often can do so only over limited voltage or power ranges. These converters rely on soft switching to maintain high efficiency at high frequency and often lose this feature as operating conditions vary. Thus circuits, architectures, and control currently present the greatest obstacle to obtaining the advantages of high frequency operation for wide operating range power conversion.

Here we present a step-up power converter which achieves zero-voltage switching (ZVS) across wide input voltage and power ranges. The converter can therefore achieve high density and efficiency through high frequency operation even in demanding applications like power factor correction.

Section II of the paper reviews some existing soft switching power converters and how they lose effectiveness outside narrow operating ranges.

Section III presents the proposed converter and its operating modes. The converter is analyzed, and it is shown that the converter achieves ZVS across wide input voltage and power ranges. Additional analysis is provided in Appendix A.

Section IV discusses some of the available control options and provides useful guidelines for design.

Section V discusses the advantages and appealing features of the converter, with special reference to power factor correction applications.

Section VI discusses implementation details and design considerations for practical application of the proposed converter. A prototype converter is presented which, operated at dc, experimentally achieves ZVS across the universal input voltage range. The prototype operates with efficiencies up to $98\,\%$, showcasing the converter's potential for high performance. These results are summarized in Section VII.

II. Limitations of Existing Converters

When a switch is turned on with voltage across it, the energy stored in the capacitance at the switching node is lost as heat through a current spike in the switch.[2] This capacitance is bounded below by the device output capacitance, which can be substantial even in wide-bandgap technologies like gallium

[1]These include the typical culprits of high frequency trouble: switching devices and magnetic components. Wide-bandgap devices have permitted much greater flexibility into the HF and VHF ranges, and low permeability magnetic materials have been shown with improved performance to $\sim$10 MHz, well above typical switching frequencies.

[2]The dual of this situation is also true. Turning off a switch with current through it will result in a voltage spike and will dissipate the energy stored in any inductance included in the switching loop. This and other recovery related losses are important at high power levels where IGBTs are commonly employed, but for powers below $\sim$10 kW and voltages below $\sim$1 kV, the use of FETs often renders these losses ignorable.

nitride (GaN).[3] This is especially true at higher voltages typical of wide voltage range applications, including grid-interface conversion, and prohibits operation in the MHz regime with hard switching. This loss can be avoided by circuit operation which allows switch voltages to decrease before the switches are turned on; this type of "soft" switching is known as zero-voltage switching (ZVS).

While many converters can use ZVS to reduce switching loss and operate at high frequencies [4], [5], such converters frequently lose efficiency outside a narrow operating range:

Resonant converters are often operated under frequency control above the relevant resonant frequency in order to inductively load the switching node and achieve ZVS. These converters must increase frequency at light load, decreasing efficiency [6], [7]. Relatively wide frequency ranges also complicate the design of efficient magnetics and EMI filters. Finally, resonant converters can suffer in large-signal transient conditions in which passive networks may take many cycles to store or release resonant energy.

Quasi-resonant converters [8] also rely heavily on frequency control and experience its associated disadvantages. Additionally, resonant peak voltages necessitate more highly rated devices, and circulating currents incur needless loss.[4]

Phase-shift control of full bridge resonant inverters can be employed at a fixed frequency, but it is difficult to achieve soft switching for all of the switches and ensure current balancing in the inverter legs, especially as power is varied [9], [10] (though this can be mitigated by resonant network design [11]–[13]). Other fixed frequency control techniques (e.g. asymmetrical clamped mode control and asymmetrical pulse width control [14], [15]) also lose ZVS at low output power, reducing light load efficiency.

Auxiliary circuits can be added to traditional circuits, as in the zero-voltage-transition pulse-width-modulated (PWM) boost converter [16]. These circuits achieve ZVS for the main power switch by using another smaller device which is still hard switched and therefore frequency limited.

Resonant-transition (RT) PWM converters operate near boundary conduction mode (BCM), allowing an additional resonant transition phase to bring the switch voltages to zero [17]. Most of these converters can only achieve true ZVS across a limited voltage range. Valley-detection can permit switching at reduced nonzero voltages, but turn-on losses still occur.[5] The boost converter in particular is frequently used in power factor correction, but even when operated with a resonant transition, it can only achieve ZVS when $V_{in} < V_{out}/2$. While this condition can be satisfied when stepping up from $120\,\mathrm{Vac}$ to a typical $\sim 400\,\mathrm{Vdc}$ bus, it is severely violated when boosting from $265\,\mathrm{Vac}$ as required for universal input.

Triangular current mode conversion [18] operates like resonant-transition PWM conversion, but it allows the inductor to build up "reverse current" before the resonant phase. The additional stored energy allows the inductor to fully discharge the switch voltage(s), achieving true ZVS. Since it is desirable to keep the reverse current as low as possible to maintain low rms inductor current, the converter only has one control handle and therefore must vary frequency to control output power.

Stacked/multilevel/modular converters introduce a great deal of complexity to divide power processing into multiple paths and/or into separate voltage domains [19], [20]. These approaches work well and achieve additional advantages like distributed heat generation, but may present difficulty in reliability and time-to-market due to their implementation and control complexity.

III. Converter Operation

The proposed converter addresses many of these concerns. Its operation is described qualitatively here, and analyzed quantitatively in Appendix A. The circuit topology (shown in Fig. 1a) consists of two half-bridges with switching nodes A and B connected by an inductor. The lumped capacitances at each switching node C_A,C_B (fundamental to the operation of the converter) are explicitly shown, though they may merely comprise switch output capacitance. One possible switch implementation is shown in Fig. 1b, which is capable of stepping up voltages in the modes presented here.

While the topology resembles that of a two-switch buck-boost converter (see e.g. [21], [22]), its operation is fundamentally different. The proposed phases of operation are illustrated in Fig. 2:

Energy Storage: Switches SA1 and SB1 are on. The inductor voltage is $+V_{in}$ and its current increases linearly. This phase ends when SB1 is turned off after a controlled time. The duration of the energy storage phase is one control handle on output power.

LC Resonant Commutation[6]: Switch SA1 is on. The inductor current charges any (parasitic) capacitance at node B (C_B). This is a resonant transition, but the initial inductor current typically makes it a rapid one and its duration can often be ignored for analysis. This phase ends when v_B reaches V_{out}, at which point SB2 is turned on. This is most easily accomplished by implementing SB2 as a diode.

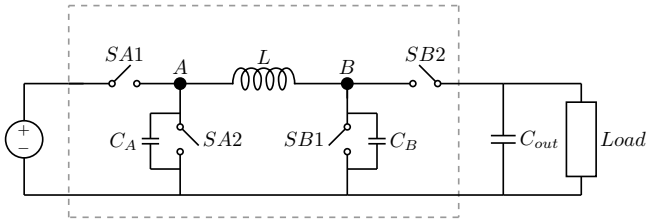
Direct Energy Delivery: Switches SA1 and SB2 are on. As in so-called "direct converters," charge is delivered in a direct path from the input to the output. The voltage across the inductor ($V_{in} - V_{out}$) is negative, and the inductor current decreases. This phase ends when SA1 is turned off after a controlled time. The duration of the Direct Energy Delivery phase is a second control handle on output power.

[3] State-of-the-art commercially available GaN FETs with blocking voltages of hundreds of volts and current ratings of several amperes (e.g. [3]) can have hard-switching energy dissipation on the order of $E_{oss} = 3\,\mu\mathrm{J}$, or $3\,\mathrm{W/MHz}$. This may be tolerable at $100\,\mathrm{kHz}$ ($0.3\,\mathrm{W}$), but efficiency constraints and thermal limits in packaged devices prohibit this approach into the MHz regime.

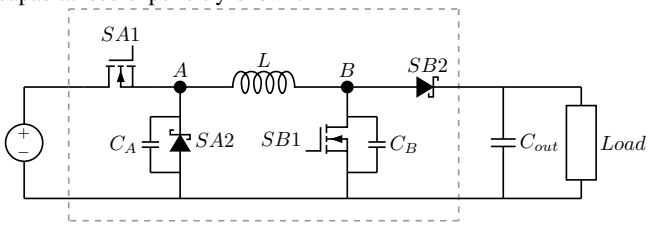
[4] Switch on-state resistances scale superlinearly with rated blocking voltage, incurring hidden additions to loss.

[5] It is sometimes argued that "partial" soft switching is sufficient because E_{oss} scales quadratically with voltage and losses are therefore mostly mitigated. While partial soft switching may indeed be sufficient for many applications, the argument is often spurious: nonlinear device capacitances make E_{oss} sub-quadratic with voltage and frequently close to linear, e.g. [3].

[6] Resonant phases are designated LC, CL, or CLC based on the order the relevant elements appear in the circuit diagram



(a) The proposed converter topology, with lumped switching node capacitances expclicitly shown.



(b) One possible switch implementation of the proposed topology. This implementation is sufficient to operate the converter in the modes presented in this work.

Fig. 1

CL Resonant Commutation: Switch SB2 is on. The parasitic capacitance at node A (C_A) is discharged through the inductor. Like the LC Commutation phase, it is typically short due to the initial inductor current. This phase ends when v_A reaches zero, at which point SA2 is turned on. Like SB2, SA2 may most easily be implemented as a diode.

Indirect Energy Delivery: Switches SA2 and SB2 are on. As in "indirect converters," energy is delivered from the inductor to the output without a direct connection to the input. The voltage across the inductor ($-V_{out}$) is negative and greater in magnitude than in the Direct Energy Delivery phase. The inductor current therefore continues to decrease with a sharper slope. This phase ends when the inductor current reaches zero, at which point SA2 and SB2 are turned off (this occurs naturally if SA2 and SB2 are implemented as diodes).

CLC Resonant Reset: No switches are on. The parasitic capacitances C_A and C_B form an equivalent CLC resonant network with the inductor, with initial conditions $v_A = 0$, $v_B = V_{out}$, and $i_L = 0$. The resonant transition will discharge C_B and charge C_A. This phase ends when v_A reaches V_{in} and v_B reaches zero, at which point[7] both SA1 and SB1 are turned on and the converter re-enters the Energy Storage phase.

The proposed converter operation ensures that every turn-on event occurs with ZVS. Thus, even with the presence of several switches, the switching loss may be kept low well into the MHz regime. This may be achieved for any combination of input and stepped-up output voltages, and theoretically for any power level. Thus, the converter may maintain high efficiency at high frequency, even with wide ranges of operation.

[7]Technically, v_A will reach V_{in} before v_B reaches zero, but the difference in time is very short. Once v_A is clamped to V_{in}, node B is discharged even faster than it otherwise would be.

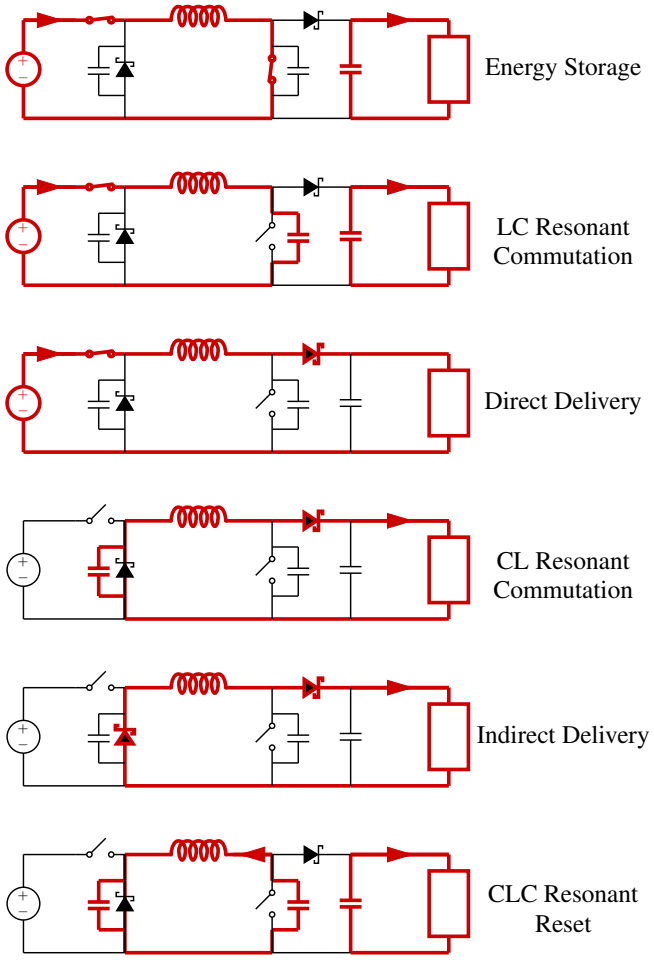


Fig. 2: Switching pattern for the proposed operating mode which achieves ZVS for any input voltage. Other modes are possible (e.g. leaving SA1 on to operate as a RT boost converter).

IV. Control

The converter output power is controlled by varying the durations of the Energy Storage and Direct Delivery phases by means of the SA1 and SB1 on-times. Because these are two independent control handles, there are infinite combinations which yield the same output power or the same operating frequency.

Qualitatively, the available combinations may be divided into two regions (see Fig. 3). The first (denoted the trapezoidal region) comprises a short Energy Storage time and a long Direct Delivery time, resulting in a "wide and flat" inductor current waveform. Long Energy Storage times and short or non-existent Direct Delivery times result in a (nearly) triangular inductor current waveform. This is denoted the triangular region. The two regions are divided by a specific combination of moderate Energy Storage and Direct Delivery times for which the converter transmits the most power at a given frequency, or operates at the highest frequency for a given power; this combination is denoted the maximum power mode.

The extent of the trapezoidal region is limited by the current i_2 at the end of the direct delivery phase (see Fig. 3), which must be sufficient to deplete the charge from C_A during the subsequent CL Resonant Commutation phase. For a given power, there is a minimum Energy Delivery time and corresponding maximum Direct Delivery time which still achieves a full discharge of C_A and brings v_A to zero. At the other end of the spectrum, the extreme of the triangular region is a pointed waveform with no Direct Delivery time and is equivalent to two-switch buck-boost conversion with a Resonant Reset transition.[8]

Timing combinations in the triangular region are generally avoided due to their higher rms currents. At a given frequency, for instance, for any output power achieved by a (nearly) triangular waveform, there is a corresponding combination in the trapezoidal regime that processes the same power for less peak and rms current.

There are at least three ways to express the two available control handles. In the circuit, these are the SA1 and SB1 on-times. In terms of operating phases, they are the Energy Storage and Direct Delivery phase durations. Finally, these handles may be expressed as the inductor current waveform shape and the operating frequency, which are roughly connected to the ratio and sum of the Energy Storage and Direct Delivery phase durations. It may be useful to think in terms of any of these three expressions.

For example, the third expression makes it clear that the ability to change waveform shape within the trapezoidal region allows the designer to constrain operating frequency of the converter with variations in power. If the range of required powers is narrow enough, single frequency operation can be used by simply varying waveform shape within the trapezoidal region. For wider power ranges a range of frequencies may be required. However, by also using waveform shape the frequency variations may be kept small.

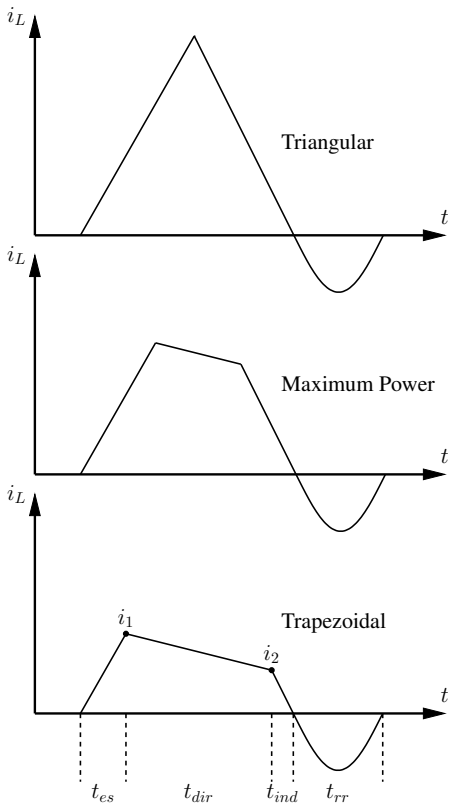


Fig. 3: Operating modes illustrated by qualitative inductor current waveforms at constant frequency. The (relatively short) CL and LC resonant commutation times are omitted for clarity; in practice they manifest themselves as rounded waveform corners as in Fig. 5. Between the trapezoidal regime and the triangular regime, there is a timing combination that transmits maximum power for a given frequency. The trapezoidal regime is preferred over the triangular regime because the major sources of loss scale rapidly with current.

V. Advantages

The proposed converter presents a number of advantages over existing approaches like those presented in Section II:

1) The converter achieves ZVS across wide voltage and power ranges, permitting efficient high frequency operation.
2) Switches need only be rated for the input and output voltages, not resonant voltage peaks.
3) A minimal amount of reverse/"circulating" current is used to achieve ZVS on all switches, reducing conduction loss.
4) The converter may be operated with low frequency variation. For sufficiently narrow ranges of output power, the converter may even be operated at fixed frequency.
5) The presence of SA1 gives the converter built-in avenues for controlling inrush current on startup. This is particularly important when comparing it to the ubiquitous boost PFC converter which, in practice, often has additional components and loss to control inrush current.
6) Because the stored energy in the inductor and capacitors is "reset" every cycle, it may achieve single-cycle transient response and more fully take advantage of high frequency operation than fully resonant converters.
7) On-time control eliminates the need for careful tuning of resonant components whose values may drift with time and temperature.
8) Because the converter transmits more power as input voltage increases, it may take advantage of constant on-time control over a line cycle to achieve power factor correction, similar to popular BCM boost converters (see Appendix A).
9) Finally, the converter may operate in more desirable modes when circumstances permit. For example, when $V_{in} < V_{out}/2$, a simple RT boost converter would also achieve ZVS with less loss. By simply leaving SA1 on, the proposed converter can operate in such a mode.

[8]The converter could push this farther and turn off SA1 *before* SB1. This would not create a Direct Delivery phase, but rather a Circulating Phase in which the inductor current was constant. While such a concept may be useful elsewhere (e.g. to provide smoother current transitions to reduce core loss [23] or for control advantages [21]), here the triangular region is avoided altogether to keep rms current low.

VI. Implementation Details

A prototype has been implemented for the specifications listed in Table I. Though the experimental results are only shown for operation with dc input, the specifications anticipate a two-stage power factor correction architecture operated from universal input (80–265 Vac) with a $\sim$400 Vdc output bus. This section contains both particular implementation details and practical considerations for designers.

A. Switches

The switch configuration of Fig. 1b is chosen to permit both the operating mode presented in Section III and operation as a RT boost converter. Switches SA2 and SB2 are implemented as diodes, while SA1 and SB1 are implemented as FETs. Since there is only incidental commutating current through SA1 and SB1, their (equivalent) body diodes are used instead of discrete antiparallel diodes.

GaN FETs are chosen to keep the parasitic capacitances C_A,C_B and dynamic $R_{DS,on}$ low to permit HF operation. At the time of writing, there are only a handful of available GaN FETs with blocking voltages over 400 V. This implementation used 650 V Navitas 6105 devices.

The selection of diodes in the MHz regime is not trivial, as their high frequency performance often degrades compared to reported datasheet values [24]. Diodes operated at HF must thus be chosen through extensive experimentation. The Cree (now Wolfspeed) C3D1P7060 SiC Schottky diode is known to this group to maintain good performance in the MHz regime with small footprint, and it was chosen for this implementation.

B. Lumped Capacitances and Nonlinearity

To achieve high frequency operation and its consequent advantages, C_A and C_B are kept as low as possible, and therefore primarily comprise the output capacitances associated with the switches (C_{FET},C_D). Since each switch output capacitance is between a switching node and a constant voltage, they may be lumped together. Moreover, if the lumped values C_A and C_B are the same, then the Resonant Reset phase can achieve ZVS for both SA1 and SB1 as explained in Section III. In practice, however, these capacitances are nonlinear and hence not instantaneously equal.

Both C_{FET} and C_D decrease with voltage, and in this case C_{FET} is consistently larger than C_D for a given voltage. Thus, for example, the net capacitance C_B is largest when v_B is near zero and smaller when v_B is near V_{out}. It is smaller still for intermediate voltages. The analogous statement, in reverse, is true for C_A.

This is most problematic in the Resonant Reset phase. At the beginning of this phase, C_B and C_A have only moderate values and the inductor stores relatively little energy before its voltage polarity reverses. Near the end of the phase, C_A and C_B take on larger values than at the beginning. The stored inductor energy is not sufficient to charge C_A and discharge C_B, and the node voltages do not necessarily reach V_{in} and zero, respectively. The converter loses ZVS and hence efficiency.

This issue may be addressed in several ways. Nonlinear capacitance may be added to linearize C_A and C_B. However such capacitors tend to be large and lossy. Low-loss linear capacitance may be added to partially linearize C_A and C_B. For this approach to be effective, the linear capacitance would have to be large to dwarf the device capacitances; this will require the converter to operate at lower frequency and lose some of its advantages.

The advantages of high frequency may be maintained by noting that the trouble is not nonlinear capacitance *per se*, but rather the asymmetry in the net capacitance-voltage characteristic. If the diode and FET had the same characteristic, for example, then the larger net capacitances at the beginning of the Resonant Reset phase would allow the inductor to store sufficient energy in the first half of the phase to achieve ZVS at the end of it. This scenario may be simulated by using parallel diodes to increase their capacitance to more closely match that of the FET. For the prototype presented here, each of SA2 and SB2 is implemented with two diodes in parallel.

C. Inductor

The inductor value is chosen according to the power/frequency argument outlined in Section IV. A desired frequency range and a required power range are defined. Then, for a given inductor value, the circuit is simulated in SPICE to identify the achievable power range between the following extremes:

1) Minimum power transmitted at the highest allowable operating frequency for the most "wide and flat" trapezoidal waveform shape
2) Maximum power transmitted at the lowest allowable frequency in maximum power mode

If the range between these two powers includes the desired operating range, then the chosen inductor value is valid. It was found that smaller inductor values expand the achievable power range and shift it to higher values. For the specifications in this implementation, inductor values between 10–20 µH were found in simulation to process the desired power in the desired frequency range. An inductor value of 15 µH was chosen for prototyping.

The inductor was prototyped using Fair-Rite 67 material which has the best known loss characteristics in the 2–5 MHz frequency range [2]. The windings were formed by 450-strand 48 AWG litz wire. The strand diamter is 31.6 µm which corresponds to the skin depth at about 4 MHz in copper. Thinner strands are generally not available at reasonable expense.

D. Timing and Ring-Down Detection

As explained in Section IV, the controlled switches SA1 and SB1 are turned on when the Resonant Reset phase restores their respective voltages to zero, and turned off after a controlled time. The circuit to accomplish this is shown in Fig. 4 (for previous uses, see [19], [25]). An identical copy is used for each of SA1 and SB1, with the control circuitry

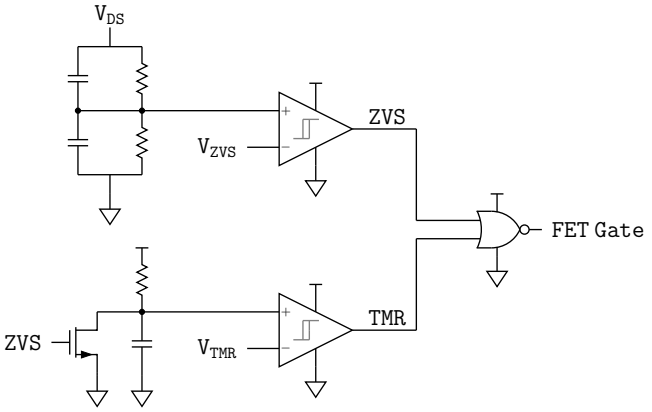


Fig. 4: "Ring down" detection circuit used to ensure ZVS turn-on in the proposed converter. In this implementation, the control circuitry is referenced to the source of the FET (when the source is not ground, an isolated or bootstrapped supply is required). This circuit can be ground referenced with some modification, though such an implementation requires driving the gate through an isolator, which incurs additional delay.

referenced to the source of the FET. In the case of SA1, this requires an isolated supply (or bootstrapping scheme) and care regarding charge injection onto node A (the signal ground). An isolated supply with minimal isolation capacitance is chosen (see Table II).

One comparator monitors the voltage V_{DS} across the switch in question (a capacitive divider with the same step-down ratio as the resistive divider is included to ensure fidelity for fast transients). As this voltage "rings down," the comparator signals the FET to turn on. The reference voltage V_{ZVS} would be set to zero for a zero-delay system, though in practice it is set at some positive value to "anticipate" the zero crossing. Delays must be considered carefully, especially at high frequency. While there is usually a window of available time to turn on the switches with zero voltage (while the body diode commutates current), it is possible for delays to be sufficient to miss this window.

The output of the ring-down detection comparator releases a ramp generator, which is implemented as an RC circuit.[9] When the ramp crosses some specified threshold V_{TMR}, it signals the FET to turn off. Thus the FETs are controlled through dc voltages V_{ZVS} and V_{TMR} which in this implementation are provided by a microcontroller and discrete DAC.

VII. Experimental Results

The prototype converter was able to consistently achieve ZVS across the entire input voltage range $\sim$10–400 V. Fig. 5 shows characteristic experimental waveforms including the inductor current and switching node voltages. It can be seen that ZVS is achieved to within reasonable tolerance and that the inductor current waveform matches analysis well even at MHz frequencies.

[9]The use of a resistor will cause some distortion in the ramp gain, but this is frequently more manageable than achieving good performance from discrete current sources at HF.

[10]Resonant transition boost mode for $V_{in} < V_{out}/2 = 200\,\mathrm{Vdc}$, proposed operating mode for $V_{in} > V_{out}/2$.

[11]Proposed operating mode only

TABLE I: Experimentally Achieved Prototype Specifications

Specification	Value
Input Voltage[10]	10–400 Vdc
Output Voltage	400 Vdc
Operating Frequencies [11]	2–2.5 MHz
Output Powers[11]	100–400 W
Efficiency	98.2 % peak

TABLE II: Components Used in Prototype

Component	Part
Microcontroller	PIC24F16KM202
DACs	LTC2602
Comparators	LTC6752
GaN FETs	Navitas 6105
Diodes	Cree C3D1P7060Q
Logic Series	SN74LVC(XXXX)
Isolated Power Supply	Burr-Brown DCV01
Inductor Core	Fair-Rite 67,
Inductor Windings	26 turn, 450-strand 48-AWG
Inductor Configuration	Toroid #5967002701 cut in half

The converter in its proposed operating mode is capable of operating across a wide voltage and power range with only a 25 % variation in frequency (see Table I). Still lower voltages and powers were achieved by operating in RT boost mode, while only increasing frequency to about 3 MHz ($\sim$50 % total variation).

The peak efficiency achieved for the initial prototype was above 98 % (operated at dc). Efficiency vs power curves at various input voltages are shown in Fig. 6. The operating range of the prototype was constrained by the reliability of integrated functionality in the selected GaN FETs, especially at higher current and temperature, not due to any fundamental restriction from the topology or thermal concerns.

VIII. Conclusion

Based on analysis and experimental results, we conclude that the proposed converter may effectively achieve ZVS for any combination of input and stepped-up output voltages. Thus, over a wide operating range, the converter can take advantage of high operating frequency to achieve both good efficiency and power density. From the literature and experimental results, it is expected that component performance will allow for increased frequencies up to tens of megahertz. Finally, based on our experience with the experimental prototype, we predict that control response speed and reliability (especially in ring-down detection) will be the most constraining obstacle to practical implementation at frequencies beyond a few MHz.

The converter topology itself is flexible and amenable to fundamental mode changes in response to circuit conditions. Both the proposed operating mode and Resonant Transition boost mode are presented here, though additional step-up and step-down options are possible.

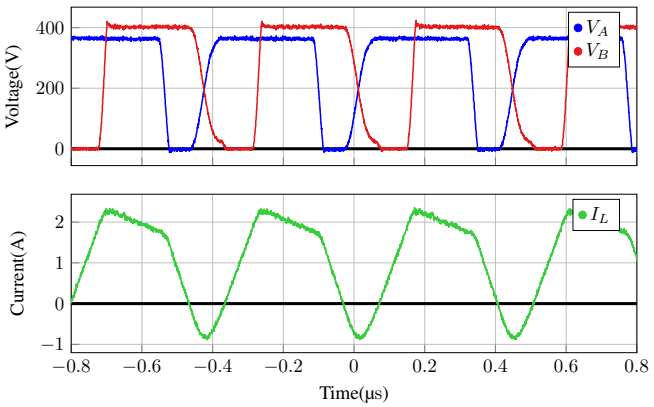


Fig. 5: Experimental inductor current and switching node voltage waveforms: $V_{in} = 355\,\text{V}$, $V_{out} = 400\,\text{V}$, $P_{out} = 355\,\text{W}$, $\eta = 98.0\,\%$. The inductor current waveform shape is as expected from analysis (the slight pointedness in the inductor current during the Resonant Reset phase is due to nonlinear capacitance which is smaller in the middle of the phase). At the end of this phase, v_A has reached V_{in} and v_B has (very nearly) reached zero, accomplishing ZVS.

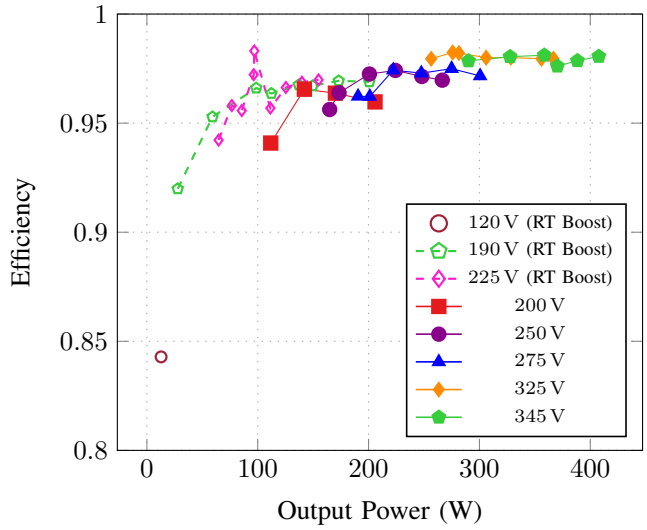


Fig. 6: Measured efficiency across power for parameterized input voltage, including the proposed operating mode and Resonant Transition boost mode. Reliable ZVS was achieved across the entire input voltage range $V_{in} < V_{out}$, permitting high efficiency. Efficiency is also maintained across a very wide power range. The power range achieved for a given input voltage is bounded below (in the proposed mode) according to the C_A discharge limitation explained in Section IV. The power is bounded above by thermal performance issues associated with an integrated GaN gate driver; it does not represent a fundamental limitation.

Acknowledgment

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Appendix A
Circuit Analysis

The switching period is divided into four sections corresponding to the four longest operating phases of the converter (see Fig. 3): the Energy Storage t_{es}, Direct Delivery t_{dir}, Indirect Delivery t_{ind}, and the Resonant Reset t_{res} durations. The peak inductor current (at the end of the Energy Storage phase) is denoted i_1, and the inductor current at the end of the Direct Delivery phase is denoted i_2.

The voltages V_{in} and V_{out} are assumed to be given and constant through the switching period. The times t_{es} and t_{dir} are commanded, and t_{res} is determined by the values of resonant elements. The unknowns are the Indirect Delivery time t_{ind} and the transferred power (equivalently, the input and output currents).

The Indirect Delivery period can be determined by volt-second balance on the inductor (note that the average voltage across the inductor during the Resonant Reset period is approximately zero for a half-period resonance):

$$V_{in}t_{es} + (V_{in} - V_{out})t_{dir} - V_{out}t_{ind} + 0 \cdot t_{res} = 0 \tag{1}$$

$$\implies t_{ind} = -t_{dir} + \frac{V_{in}}{V_{out}}(t_{es} + t_{dir}) \tag{2}$$

The average output current may be calculated next. Current is only delivered to the output during the Direct and Indirect Delivery phases, yielding an average current of:

$$\langle i_{out} \rangle = \frac{1}{T}\left[\frac{1}{2}(i_1 + i_2)t_{dir} + \frac{1}{2}i_2 t_{ind}\right] \tag{3}$$

Substituting $i_1 = V_{in}t_{str}/L$ and $i_2 = V_{out}t_{ind}/L$ and simplifying, it is found that

$$\langle i_{out} \rangle = \frac{V_{in}^2(t_{es} + t_{dir})^2 - V_{in}V_{out}t_{dir}^2}{2L(V_{out}t_{str} + V_{out}t_{res} + V_{in}(t_{str} + t_{dir}))} \tag{4}$$

As an example, consider Fig. 5, which has $V_{in} = 355\,\text{V}$, $V_{out} = 400\,\text{V}$, $t_{str} = 100\,\text{ns}$, $t_{dir} = 100\,\text{ns}$, $t_{ind} = 75\,\text{ns}$, and $t_{res} = 100\,\text{ns}$. Plugging into (4) yields an output current of $\langle i_{out} \rangle = 0.925\,\text{A}$, which corresponds to an output power of $P_{out} = 370\,\text{W}$. The actual measured output power was $355\,\text{W}$, which is within $5\,\%$ of the calculated value. The error is understood to be even smaller, as the above calculation does not take losses into account. Including the measured efficiency of $\eta = 98\%$, the calculated and measured efficiencies are just over $2\,\%$ different.

This analysis also shows that the converter can approximately achieve automatic power factor correction by not changing on-times over the line cycle, similar to that achieved by the BCM boost PFC. Computing $V_{in}/\langle i_{in} \rangle$ and using conservation of power $V_{in}\langle i_{in} \rangle = V_{out}\langle i_{out} \rangle$ (approximately true), the following is obtained:

$$\frac{V_{in}}{\langle i_{in} \rangle} = \frac{2L(t_{es} + t_{res} + \frac{V_{in}}{V_{out}}(t_{es} + t_{dir}))}{(t_{es} + t_{dir})^2 - \frac{V_{out}}{V_{in}}t_{dir}^2} \tag{5}$$

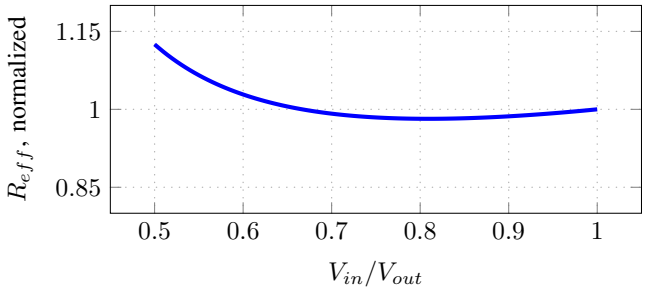

Fig. 7: Large signal input resistance of the converter operated with $t_{es} = t_{dir} = t_{res}$ (see (6)), normalized to its value when $V_{in} = V_{out}$. Below $V_{in}/V_{out} = 0.5$, it is more straightforward and efficient to operate in Resonant Transition Boost mode.

For a converter to operate with unity power factor, its input current must be proportional to its input voltage. It is apparent from (5) that this is not quite the case for the proposed operating mode. Nevertheless, the V_{in}-dependent terms in (5) are somewhat anchored by accompanying constant terms, and may be dwarfed by those terms in many circumstances.

Indeed, taking a reasonable scenario like $t_{dir} = t_{es} = t_{res}$, the large signal effective resistance of the converter is given by

$$\frac{V_{in}}{\langle i_{in} \rangle} = \frac{L}{t_{es}} \frac{4 + 4\frac{V_{in}}{V_{out}}}{4 - \frac{V_{out}}{V_{in}}} \tag{6}$$

For the example timing values which yield (6), the large signal resistance (see Fig. 7) changes by less than $15\,\%$ over the relevant voltage range for this operating mode, $1/2 < V_{in}/V_{out} < 1$. Thus the converter may achieve good power factor without changing switch on-times over the course of the line-cycle (allowing for variable on-times on that time scale would naturally permit unity power factor).

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