

Single Phase Universal Input PFC Converter Operating at HF

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Abstract— Single-phase ac to dc converters for computers and related applications have requirements that are difficult to meet while achieving both high power density and high efficiency: wide input voltage range, large voltage step down, galvanic isolation, harmonic current limits and hold-up requirements. This work explores a circuit architecture and topology that seeks to address this challenge, and presents a 250 W, 24 V output, universal input PFC converter prototype achieving 34.9 W/in³. The converter operates at variable switching frequencies in the range of 1-4 MHz; the measured efficiency at 230 Vac RMS, 60 Hz input is 95.33% at full load and 84.57% at 8% load.

Keywords—off line converter, single phase PFC, universal input, high frequency

I. INTRODUCTION

Single-phase PFC converters in the hundreds of watts range typically need to meet EN61000 harmonic current specifications, operate over universal input voltage, source hold-up energy for line transients, and provide large voltage step down and isolation to the output. Meeting the EN61000 specification requires precise control of the converter input current in order to provide a waveform with low harmonic content. The universal input voltage range is often defined from 86 to 264 Vac RMS which translates to instantaneous input voltages between 0 and 372 V. This is a fairly wide input voltage range and it is difficult to make the converter operate efficiently at all operating points, particularly as a converter needs to operate over much of the line cycle to meet line harmonic specifications. Finally, converters for server applications are often expected to deliver full load during a transient event in which the ac line is disconnected; a typical hold up time is one full line cycle or 20 ms in the case of a 50 Hz ac input. The converter needs to have an energy storage element to provide said energy and this usually requires significant volume. In addition to these specifications, ac-to-dc converters take pulsating power and deliver dc power. There needs to be sufficient energy storage in the converter to buffer the twice-line-frequency power pulsations. Simultaneously meeting all these requirements while achieving high efficiency and power density is a challenge [1-3].

There are two main types of circuit architectures used to solve this problem: single-stage [4-6] and two-stage [7-9]. In this paper a two-stage PFC circuit architecture suitable for high-frequency (multi-MHz) operation at high efficiency and

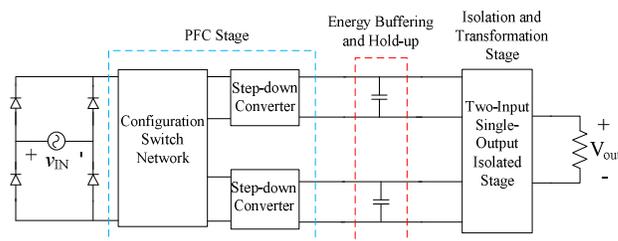


Fig. 1. Single phase ac/dc converter architecture. The converters consists of a rectifier bridge, a configuration switch network, two step-down converters, energy buffering capacitors and an isolation and transformation stage.

power density is developed and experimentally tested. Figure 1 shows the architecture of the converter. The front end is the PFC stage and the 2nd stage is an isolation and regulation stage. For reasons that will be described, the first stage has two outputs and the second stage has two inputs. The energy buffering capacitors are placed at the two ports that interconnect the two stages. The proposed system utilizes structural reconfiguration to reduce the operating requirements of the subsystems and achieve a combination of high efficiency and high power density.

The PFC stage consists of an input bridge rectifier, a configuration switch and two step-down converters, each of which has its output connected to an energy buffer capacitor. The configuration switch connects the inputs of the step-down converters in parallel if the input ac voltage is low (i.e. 85 to 130 Vac RMS) and in series if the ac voltage is high (i.e. 170-264 Vac RMS). The state of the configuration switch is set once when the converter is connected to the ac line based on the ac input voltage, and stays that way for the remainder of the operating time. This scheme allows the step-down converters to have a reduced and relatively narrow voltage range regardless of the line voltage magnitude. The peak voltage rating of the PFC step-down “building block” converters is 186 V, which enables the use of high performance, small footprint GaN FETs. Moreover, having a lower peak input voltage is favorable for achieving operating frequencies in the multi MHz range [7]. As described below, we select a buck-type power stage that enables high-frequency operation in the MHz range and current-sensorless control. The reduction in required operating range afforded by reconfiguration enables good line waveform quality to be achieved despite input voltage range

limitations of buck conversion.

Typically PFC converters use boost-type converters because they allow nearly sinusoidal current to be drawn from the line (thus providing very high power factor) [1-3]. In these converters the energy is buffered at a voltage close to 400 V (or at least higher than 372 V). The widespread use of this buffering voltage has influenced the performance of available capacitors: Figure 2 shows the usable energy density for a sample of electrolytic capacitors. It is clear from this plot that by storing energy at voltages far from 400 V there is a penalty in the size of the energy buffer. However, storing the energy at 400 V means the 2nd stage has to step down from 400 V to low output voltages, typically tens of volts (12, 19, 24, 48 V, etc.). This large step down ratio tends to compromise achievable efficiency. By using a step down converter in this design, we sacrifice energy buffering density for improvements in achievable switching frequency and efficiency of the converter power stage elements. Energy storage for twice-line-frequency buffering and holdup is stored at a low voltage of approximately 70-80 V in two capacitor banks.

The second stage converter is a two-input, single-output converter which provides isolation and regulation of the output. The inputs to the second stage are the energy buffering capacitors which have twice line frequency ripple on them. The converter also needs to balance the two inputs so that the loads are shared equally, particularly when the buck converters are connected in series. It has to operate with high efficiency during normal operation but also provide the full output power across a wide input voltage range due to hold-up time transient events. The topology selected for this converter is based on the dual-active-bridge concept [10,11]. It provides soft switching for all the transistors and is designed to operate at near 1 MHz switching frequency but can easily operate at a different frequency without disturbing normal operation. In the following sections, each subsystem of the converter will be explained in detail.

II. PFC STAGE

As described previously and shown in Fig. 1, the PFC stage consists of 2 step down converters and a configuration switch network; the detailed structure including the active rectifier, configuration network and buck converters is shown in Fig. 3. The reconfiguration network connects the step down converters in series if the ac input voltage is high (i.e. 170 to 264 Vac RMS) and in parallel if it is low (i.e. 85 to 130 Vac RMS). This reconfigurability reduces both the maximum input voltage and required input voltage range of the two buck converters over the universal ac input range. The nominal output voltage of each of the two converters was chosen to be 72 V (average), which allows the buck-type converter to operate over a sufficient part of the line cycle to meet EN61000 line harmonic requirements.

The step-down converters are resonant transition inverted buck converters, or "RTI" buck converters, as detailed in Fig. 4 [7,12]. This converter has several features that make it suitable for realizing high density and high efficiency: it operates in discontinuous

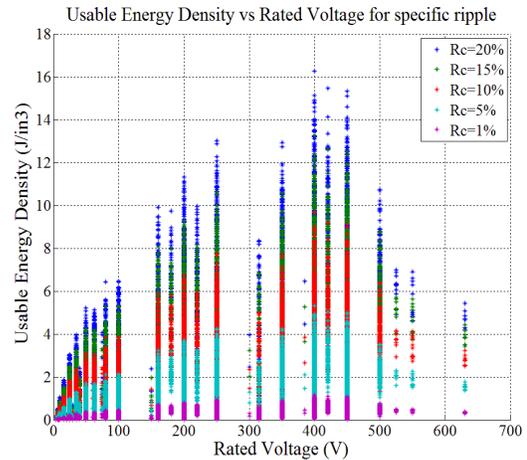


Fig. 2. Usable energy density for electrolytic capacitors at different voltage ripple ratios vs. rated voltage. Usable energy density is the energy density achievable by a capacitor as limited by how much voltage ripple is allowed every cycle. Data obtained from capacitor sellers online for over 1000 capacitors.

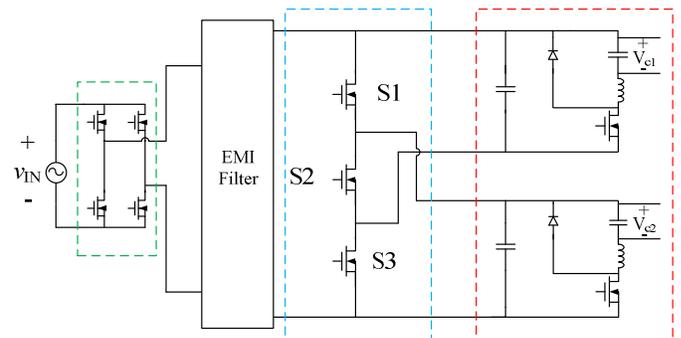


Fig. 3. Details of the PFC stage: active line rectifier (green), configuration switch network (blue) and step-down converters (red). If the input voltage is high, S2 turns on and the inputs to the step-down converters connect in series. If the input voltage is low, S1 and S3 turn on and the inputs to the step down converters are connected in parallel. The output of each step-down converters is connected to an energy buffering capacitor.

conduction mode (allowing for small inductor value and size) and maintains zero voltage switching (ZVS) up to a 2:1 step down voltage ratio, with low-loss "near ZVS" operation at up to a 3:1 step-down conversion ratio. Additionally the single active switch in the inverted buck topology is ground referenced, which simplifies driving it at HF, and by virtue of it being a step down converter the switch voltage stress is smaller than the more traditional boost type. This enables the use of highly efficient and small footprint GaN FETs. Moreover, input current can be (indirectly) controlled through transistor on time, without the need for current sensing [7,12,13].

The first-stage PFC converters each use transistor on-time control to regulate the output. Therefore, its switching frequency varies with operating point. The prototype developed here operates between 1 to 4 MHz, an order of magnitude higher than typical PFC stages, with substantial benefits for required passive component volume and EMI filter size [7,14].

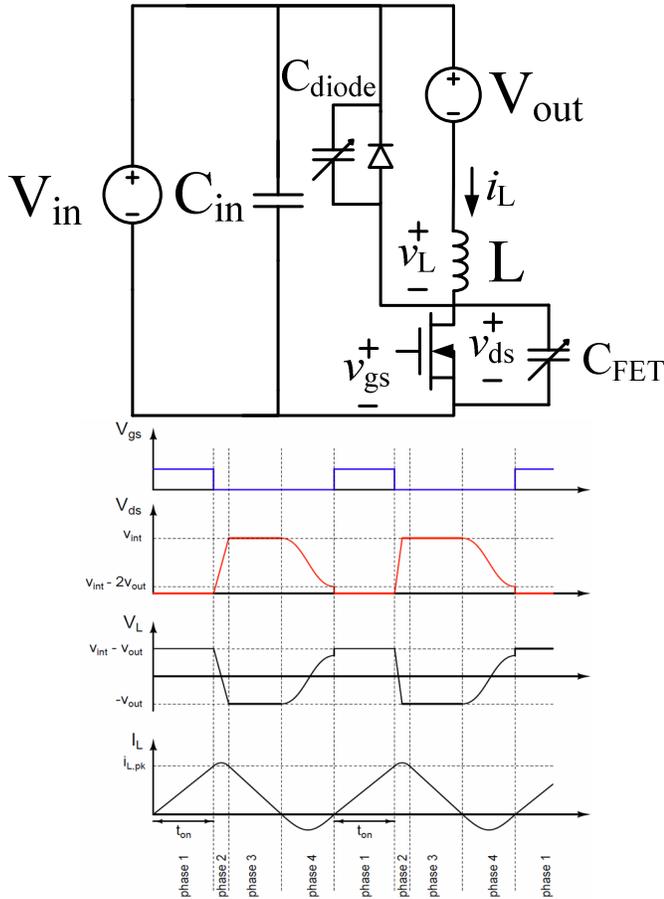


Fig. 4. Resonant transition inverted buck converter and its ideal waveforms. This topology is excellent for miniaturization as it operates in DCM which enables the use of a small inductor. Also, ZVS is maintained over a roughly ~2:1 step down ratio which minimizes losses as switching frequency increases and the power switch is ground referenced.

A. Component Selection of RTI Buck

The RTI buck converter is the building block of the PFC stage. The performance of a single RTI buck converter was evaluated using a tester board. The purpose of the tester board was to rapidly measure efficiency and temperature and have enough flexibility to change components (with possibly different package and/or footprints) and test again. Rigorous analysis narrowed down the components to 3 or 4 devices with similar properties and they were tested in the circuit. Parameters such as temperature rise, efficiency and volume were taken into consideration in choosing the best components for the proposed system. The tester board runs from a dc input supply and the load is a constant voltage load. During PFC operation the converter will process a peak power of 300 W with an average of about 125 W (the exact value depends on the efficiency of the second stage); therefore during the dc-dc testing phase the converter performance is evaluated from 30 to 300 W. Appendix A contains details of the component selection process. Table 1 summarizes the power stage parts list of the RTI buck converters.

Table 1. Finalized part list for RTI buck converter. All capacitors listed in this table are ceramic capacitors.

Part	Name
Transistor MOSFET	3x EPC2025
Diode	MBRB40250TG
Inductor	E-22-3F45, L=5 μ H 5 turns of 46/450 litz wire, 7.5 mils airgap in each core leg, 62 mil spacer between airgap and winding
Input capacitors	3x 1 μ F, 250V 1825 package 2x 0.1 μ F, 250 V 0805 package
Output capacitors	6x 1 μ F, 250V 1812 package 1x 0.1 μ F, 250V 0805 package

B. Input current shaping

During the rigorous testing of each individual block, it was found that the RTI buck converter operates with higher efficiency at lower input voltages. If the input current follows the line voltage, the PFC converter will draw high current at the peak of line voltage, which means it draws the highest amount of power when it is the least efficient. However by changing the current reference the converter can draw higher power when the line voltage is smaller, thus reducing the amount of power processed at peak voltage (which in turn increases converter average efficiency over a line cycle). This input current shaping adds distortion to the line current and is limited by EN61000 regulation. As will be discussed in the experimental results section, there is room to improve efficiency by current shaping before reaching the EN61000 limits. This type of nonsinusoidal current shaping strategy has been utilized to advantage in previous grid-interface converters for both efficiency and waveform considerations [7] as well as for capacitor size reduction [7,15,16].

C. Active rectifier bridge and configuration switch

As shown in Fig. 3 (green outline), an active rectifier bridge is used at the input of the supply to maximize efficiency. STB32NM50N FETs with a typical on-resistance of 0.1 ohms are used to provide low conduction losses and withstand peak input voltages of 500 volts. The gates are driven by Vishay VOM1271 photovoltaic MOSFET drivers with integrated fast turn-off. They are able to turn off the rectifier FETs in under 20 μ s though it takes 1 - 2 ms to turn them on. Because the rectifiers operate at line frequency, this is not a problem. The input voltage is continuously monitored by the processor and compared with the buck converter output voltage. If the input is more than 15 volts higher than the output voltage, the appropriate FETs are turned on. If the voltage difference is less than 8 volts, they are turned off. When the supply is first powered up and no gate drive signals are supplied, the body diodes of the FETs perform as a conventional full bridge rectifier.

The configuration switch network shown in Fig. 3 (blue outline) is used to connect the two buck converters in series or

parallel. Infineon BSC600N25NS3 FETs with an on-resistance of 60 mohms and a Vds of 250 volts are used for this function. S1 and S2 are also driven by Vishay VOM1271 photovoltaic MOSFET drivers but S3 does not require an isolated drive. When no gate drive signals are present, the two buck converters are connected in series by the body diode of S2. This default condition at power up allows time for the control processor to measure the input line voltage and determine if series or parallel operation is required, based on the input line voltage. The appropriate switches are normally turned on when the supply is first started and not changed.

III. ENERGY BUFFERING CAPACITORS

The energy buffering capacitors are chosen selecting the minimum volume capacitance that meets: *i)* the energy buffering requirement, *ii)* the hold-up time requirement, and *iii)* the capacitor RMS current limit. Each constraint will be explained in more detail:

i) Capacitance due to allowed voltage ripple

This requirement varies with topology and application. In this case the ripple is limited by the input voltage range on the second stage converter. Thus, the maximum voltage ripple ratio R_C is:

$$R_C = \frac{V_{max}}{V_{nom}} - 1 \quad (1)$$

where V_{nom} is the nominal voltage or average voltage that the energy is stored at and V_{max} is the maximum voltage allowed by the second stage converter. From here one can determine the capacitance C_{ripple} needed to maintain this ripple and relate it to the amount of energy needed to be buffered every half cycle:

$$C_{ripple} = \frac{E_{buff}}{2R_C V_{nom}^2} \quad (2)$$

where E_{buff} is the twice line cycle energy buffered.

ii) Capacitance due to hold-up time requirement

The second stage converter needs to be able to deliver full dc power P_{dc} to the load during a transient event where the ac input power is cut-off for a duration $t_{hold-up}$. The amount of capacitance $C_{hold-up}$ needed to provide constant dc power to the load during time $t_{hold-up}$ is:

$$C_{hold-up} = \frac{2P_{dc} t_{hold-up}}{(V_{nom} (1 - R_C))^2 - V_{min}^2} \quad (3)$$

where V_{min} is the minimum allowed voltage of the second stage converter.

iii) Capacitor RMS current rating

Electrolytic capacitors typically offer the highest peak energy density when compared to other families of capacitors (such as ceramic, mica, porcelain, tantalum, etc.), and thus are widely

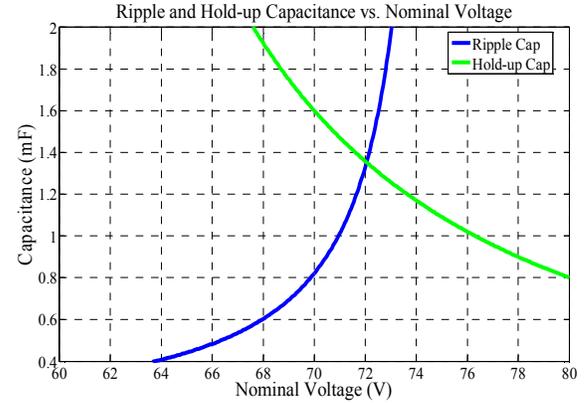


Fig. 5. Plot of ripple and holdup capacitance requirements as a function of V_{nom} . This plot tells us what is the minimum capacitance that meets both ripple and hold-up capacitance spec. The minimum point is shows $C = 1.35$ mF and $V_{nom} = 72$.

used in PFC converters. This advantage comes at a cost: electrolytic capacitors have high equivalent series resistance (ESR) and thus are thermally limited in the amount of current they can carry to support transfer of energy every half cycle. It is typical practice from manufacturers to specify the capacitor's rated RMS current for various frequencies. The required specification of

RMS current of the capacitor varies with application and topology because it is entirely dependent on the capacitor current waveform.

Now one applies these constraints to the design to size our energy buffering capacitors. The second stage converter to be used in this design has an input voltage range of 40-80 V (this is not an absolute range as the devices are rated for higher voltage and hold-up time is a transient event). This translates to a V_{max} of 80 V and V_{min} of 40 V. The energy that we need to buffer E_{buff} is 0.573 J, the full dc power P_{dc} (for each of the two converters) is 125 W, and the hold-up time $t_{hold-up}$ is 20 ms (full 50 Hz line cycle). In order to find the minimum value of capacitance (for each of the two PFC converter blocks) that meets both ripple and hold-up specifications, substitute equations (1) into (2) and (3), and plot (2) and (3) as a function of V_{nom} . This plot is shown in Fig. 5. From Fig. 5, the minimum value of capacitance is the interception of both graphs; in this case the minimum capacitance is 1.35 mF stored at $V_{nom} = 72$ V. (This corresponds to $R_C = 0.0416$ or 4.16% ripple ratio in the equations above.) The RMS current required for the energy buffering capacitors is 1.68 A at 100 Hz (from simulation results of the proposed PFC stage topology).

This analysis reveals that the best energy buffering capacitor will be the smallest capacitor or combination of capacitors rated for 80 V with an RMS current rating greater than 1.68 A at 100 Hz and an equivalent capacitance greater than 1.35 mF. The energy buffering capacitor bank chosen as the best candidate consist of two of the EKYB800ELL681MK40S (each rated for 80 V, capacitance of 0.68 mF and RMS current capacity of 1.47 A) in parallel.

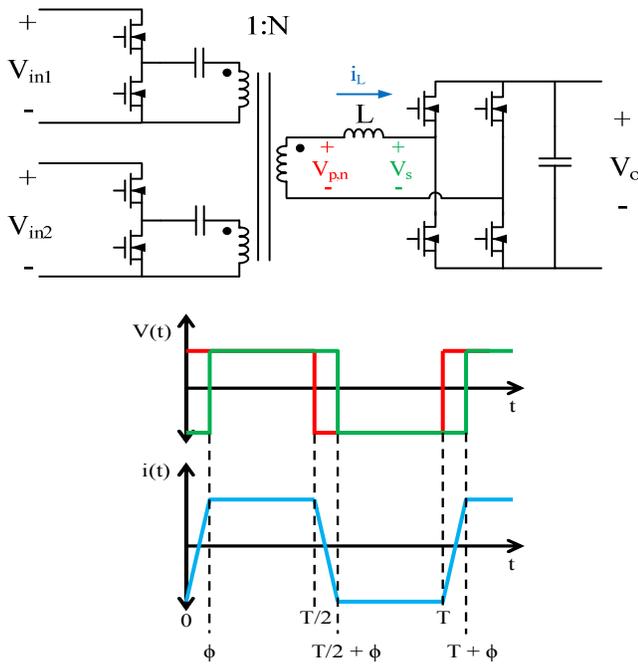


Fig. 6. Second (isolation) stage converter. This converter operates similar to a dual active bridge (DAB) converter. It also provides galvanic isolation, power combining and output regulation. The half bridge inverters on the primary side operate in phase with each other, while the rectifier full bridge at the secondary is phase shifted with respect to the inverters. The phase shift is used as a control handle for output regulation.

IV. ISOLATION STAGE

The isolation stage converter is shown in Fig. 6. This converter operates similarly to a dual active bridge (DAB) [6,7,17], but enables power to be drawn from (and transferred between) two inputs while providing a single output. The relative phase shift between the inverters and the rectifier control the output power delivered. The output power of the converter is described in the following equation:

$$P_o = \frac{N * V_{in} * V_o}{2 * \omega * L} * \Phi * \left(1 - \frac{\text{abs}(\Phi)}{\pi}\right) \quad (4)$$

where N is the 1: N turns ratio of the transformer, V_{in} and V_o are the input and output voltages, ω is the switching frequency in radians, L is the equivalent inductance referred to the secondary (includes transformer leakage and any additional inductance) and Φ is the phase shift (in radians) between the inverters and the rectifier. The trapezoidal current shown in Fig. 5 provides the minimum RMS current for a given output power. If the voltage relationship $N * V_{in} / 2 = V_o$ is not satisfied the current will not be flat topped and the RMS current will be higher. This converter is designed to be very efficient at a nominal input value of voltage and for small deviations around it. This is to account for the twice line frequency ripple on the energy buffering capacitors. However the converter can operate over a wide range of inputs for a transient event such as the hold-up time. For example, by decreasing frequency monotonically the output power can be regulated during a hold-up time event.

Table 2. Finalized part list for the isolated converter. Transformer inductances stated below are referred to the secondary.

Part	Name
Inverter MOSFET	EPC2016C
Rectifier MOSFET	EPC2024
Transformer	E-22-DMR51, $L_{leak} = 80$ nH, $L_{mag} = 8.2$ μ H Primaries: 3 turns of 48/1000 litz wire each, Secondary: 2 turns of 48/1000 litz wire, Winding configuration: PSSP (2 secondaries connected in parallel)
Inductor	Half core Fair-Rite 3061990871 5 turns of 1000/48 litz wire $L = 280$ nH

Another important characteristic of this converter is its zero voltage switching (ZVS) capability. During the switch dead time part of the cycle, the FET's voltage will ring down so that it turns on at a lower voltage. With sufficient switch current, the switch voltage will ring down all the way to zero. The minimum switch current needed for ZVS is given by:

$$I_{SW,min} = \frac{2 * \sqrt{V_{in} * V_o / N}}{Z_o} \quad (5)$$

where Z_o is the characteristic impedance of the transformer equivalent inductance and the switch capacitance. As a consequence, ZVS is lost at light loads. The load range for ZVS can be extended by increasing magnetizing current (through reduced magnetizing inductance) at the cost of efficiency during heavy loads.

The summary of the components used in the isolation stage is shown in Table 2. The design parameters were a nominal input voltage of 72 V, output of 24 V, output power of 250 W and a switching frequency of 575 kHz. Appendix B details the selection criteria for these components.

V. EXPERIMENTAL RESULTS

The PCB, which consists of the full converter including the line rectifier, EMI filter (on the dc side of the rectifier), PFC converter, isolation stage, auxiliary power supply and control circuitry is shown in Fig. 7. This prototype converter provides a "box volume" power density of 34.9 W/in³, which is achieved through the proposed architecture and multi-MHz operation. A breakdown of the volume is shown in Table 3. The RTI buck converter, the energy buffering capacitors and the isolation stage dominate the volume of the system.

Figure 8 shows the full system efficiency for 115 and 230 Vac, 60 Hz input. Figure 9 shows the line voltage and current waveforms and the dc output waveforms for full power and 230 Vac input. The efficiency is 95.02%. Figure 10 shows the line current harmonics relative to their limit as constrained by the EN61000 specification. As stated in section II.B., there is still room for harmonic content to be added before reaching the limit.

Several changes can be made to the control scheme that can improve the efficiency by only changing the microcontroller software. These include changing the average voltage on the buffer capacitors, changing the deadtime on the second stage as a function of power and shaping the input current to our benefit (at the expense of ac input current harmonics). All these values were adjusted empirically to maximize system efficiency. Figure 11 shows the input and output waveforms after the implementation of these changes, while Fig. 12 shows the harmonic current content. Figure 13 shows the final efficiency data after the implementation of the empirical changes. The efficiency at full power is 95.33%. The peak efficiency is 95.58% at 175 W.

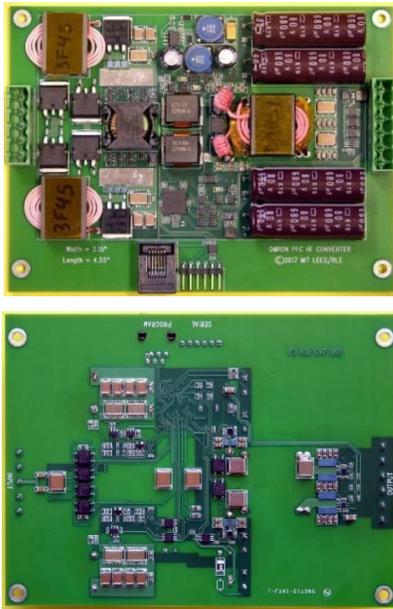


Fig. 7. Top and bottom sides of the full system PCB. There is space for cutouts for the capacitors and magnetics which bring the total board height to 0.5 inches. The height is limited by the diameter of the electrolytic capacitors.

Table 3. Box volume breakdown of the full system. The total height is 0.5 inches. The major contributors are the buck PFC stage, the energy buffering capacitors and the isolated dc/c converter stage.

Item	Area (in ²)	Volume (in ³)	Fraction (%)
EMI Filter	1.216	0.608	8%
Line Rectifier	1.215	0.608	8%
Mode Switch	0.278	0.139	2%
Buck	3.58	1.79	25%
Energy Buffer	3.45	1.725	24%
Control	1.036	0.518	7%
Isolation Stage	2.706	1.353	19%
Control Supply	0.852	0.426	6%
Total	14.333	7.166	100%
Density	34.89	watts/in ³	

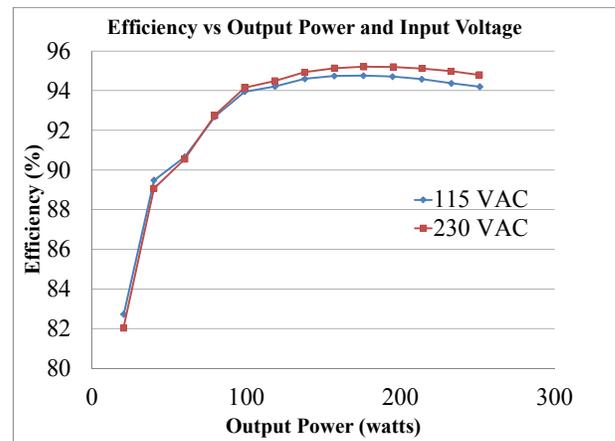


Fig. 8. Full system efficiency at 115 and 230 Vac RMS, 60 Hz input. Efficiency at full power and 230 Vac is 94.8%.



Fig. 9. Line voltage (red), line current (yellow), output voltage (blue) and output current (purple) for the following operating point: input of 230 Vac output voltage of 24 V and output power of 251 W. The power factor is 0.941 and efficiency 95.02%. The line current follows the line voltage.

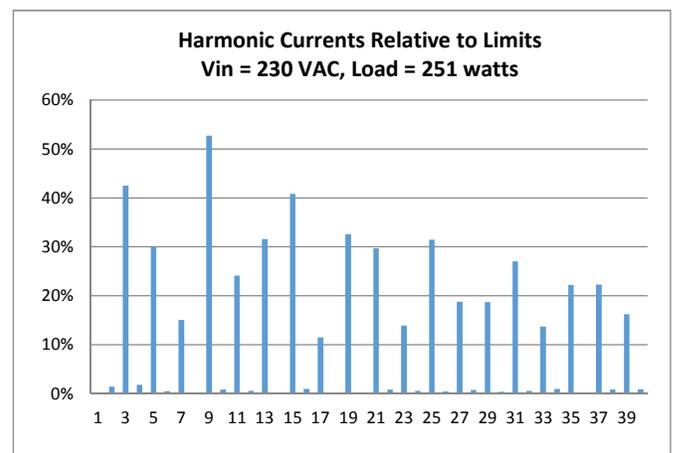


Fig. 10. Harmonic currents relative to the limits stated by EN61000 from the current waveform in Fig. 8. The 9th harmonic is the closest to its limit.

VI. CONCLUSIONS

In this work a universal input single phase power supply is introduced that enables high power density and efficiency under high-frequency (1-4 MHz) operation. The architectural and topology decisions are presented, and a prototype converter is designed, built and tested. The design constraints and trade-offs are discussed. The proposed converter utilizes reconfiguration to reduce the operating range requirements of the first (PFC stage), and facilitate achieving Multi-MHz operation. Active rectification and line current shaping are also used to achieve high efficiency and power density, as is careful selection of circuit topologies to realize the proposed architecture. Overall a high combination of efficiency (>95% from universal input to 24 V dc output) and high power density (34.9 W/in^3) is achieved, while meeting key requirements of such grid-interfaced converters.

ACKNOWLEDGMENT

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APPENDIX A

In this appendix the selection criteria for the RTI buck converter components is discussed in detail. The selection of the MOSFET was based on the soft switching figure of merit $C_{OSS} \cdot R_{ON}$ (output capacitance of the FET times on-resistance from Drain to Source), which is plotted in Fig. 14 against rated voltage. The 300 GaN FET EPC2025 was picked as the appropriate FET, and the tester board was prepared to check if there is an advantage in paralleling these devices. Utilizing 3 FETs in parallel minimizes the loss over the complete operating range. Two FETs provided higher loss at high power while 4 FETs increased the low power loss significantly.

The diode was selected in a similar fashion. A handful of Si Schottky diodes were tested on the tester board and the efficiency of the converter was measured. Ultimately the MBRB40250TG was selected for the final design.

The inductance value is designed to be as small as possible to minimize inductor size while being able to deliver power across a 10:1 power range, in continuous operation (i.e., without bursting). Taking into consideration minimum power (30 W), maximum input voltage (186 V), the inductance needed is approximately $5 \mu\text{H}$. The inductor design considerations are core and winding losses, volume and temperature rise. The inductor was hand-wound using commercially available E shaped magnetic cores and litz wire. A Matlab script was written to sweep through various combinations of core materials, core geometries and winding configurations to find the best designs. The winding losses are calculated using Dowell's Equation (accounting for skin effect and proximity effect) [18] and the core losses are calculated based on fittings of datasheet core loss data and core loss data measured by Hanson, et al [14]. These designs were narrowed down to a handful and they were tested on the tester board. The inductor chosen for the final design uses an E-22-3F45 core, uses 5 turns of 46/450 litz wire, has 7.5 mils of airgap in each



Fig. 11. Line voltage (red), line current (yellow), output voltage (blue) and output current (purple) for the following operating point: input of 230 Vac output voltage of 24 V and output power of 251 W. The power factor is 0.948 and efficiency 95.236%. This data point is taken including all the software changes that increase efficiency. The converter does not draw peak current when the voltage is maximum.

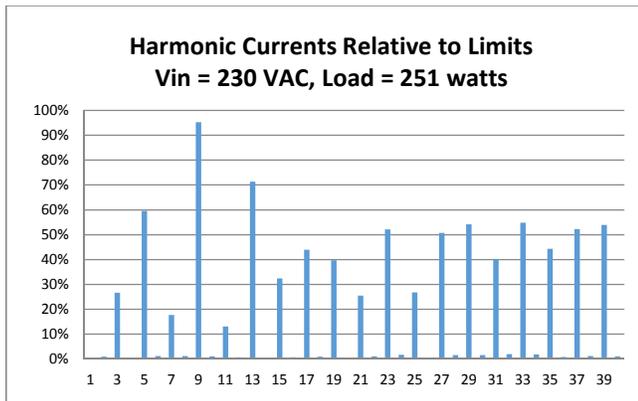


Fig. 12. Harmonic currents relative to the limits stated by EN61000 from the current waveform in Fig. 10. The 9th harmonic is the closest to its limit.

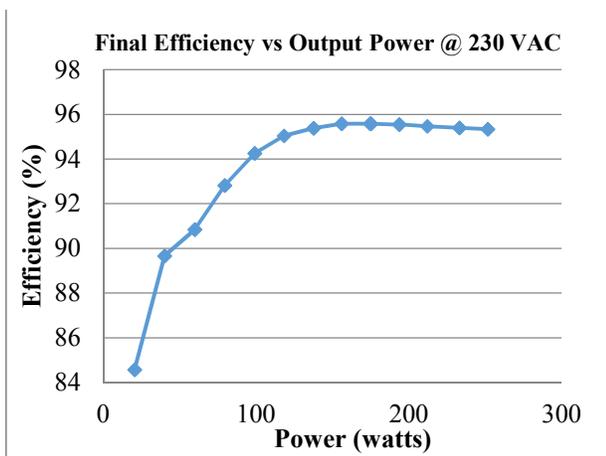


Fig. 13. Full system efficiency at 230 Vac RMS, 60 Hz input after all empirical adjustments have been implemented. Efficiency at full power and 230 Vac is 95.33%.

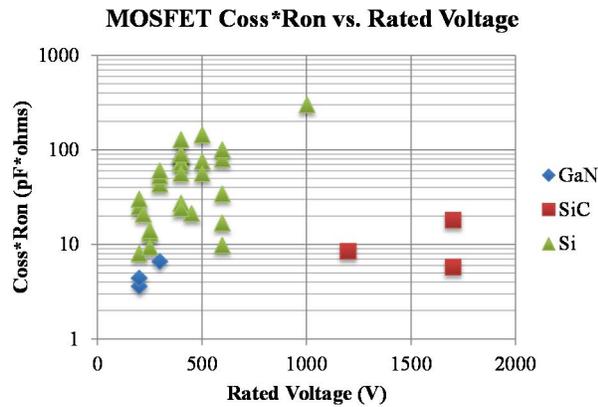


Fig 14. Plot of MOSFET's soft switching figure of merit as a function of voltage. GaN transistors showed the best (minimum) figure of merit.

leg of the core, and a 62 mil spacer between airgap and winding. A summary of the components of the RTI buck converter is shown in Table 1.

APPENDIX B

In this appendix the selection process for the isolated stage is discussed in detail. The MOSFETs were selected in a similar manner to the ones from the PFC block: pick a handful of devices using their datasheet and test them on a tester board. The FETs used in the inverters are EPC2016C and in the rectifier EPC2024.

The transformer is designed in a similar manner as above: using a Matlab script and testing a few designs using a tester board. The Matlab script uses information about core material, core geometry, switching frequency, litz wire winding (diameter and number of strands) and turns ratio to estimate copper [19] and core losses. The transformer used in the final circuit uses two E22 cores of DMR51, which is suitable for the ~1 MHz operation used. Each primary (P) has 3 turns and the secondary (S) has 2 turns. There are two secondary coils, each of two turns, connected in parallel. The transformer is wound PSSP (top to bottom) using 1000/48 litz wire.

The transformer leakage inductance is used to satisfy the operating conditions of the circuit. From equation (4) one can see that there exists an upper bound on inductance value (for a fixed frequency, turns ratio and input/output voltages) that satisfies the output power requirement. To deliver 250 W with a 575 MHz switching frequency, a nominal input voltage of 72 V and an output voltage of 24 V the leakage inductance referred to the secondary is approximately 300 nH. On this circuit additional leakage inductance is needed on top of what the transformer provided. Two rod core inductors were placed on each primary of the transformer. The inductors used were each a half core 3061990871 from Fair-Rite using 5 turns of 1000/48 litz wire (each providing an inductance of about 280 nH).

REFERENCES

[1] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single Phase Power Factor Correction: A Survey," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749-755, May 2003.

[2] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381-1390, May 2008.

[3] G. Moschopoulos, and P. Jain, "Single-Phase Single-Stage Power-Factor-Corrected Converter Topologies," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 23-35, February 2005.

[4] M. Scherbaum, M. Reddig, R. Kennel, and M. Schlenk, "An Isolated, bridgeless, quasi-resonant ZVS-switching, buck-boost single-stage AC-DC converter with power factor correction (PFC)," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 74-81, March 2017.

[5] M. Narimani, and G. Moschopoulos, "A New Interleaved Three-Phase Single-Stage PFC AC-DC Converter With Flying Capacitor," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3695-3702, July 2015.

[6] D. L. O' Sullivan, M. G. Egan, M. J. Willers, "A Family of Single-Stage Resonant AC/DC converters With PFC," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 398-408, Feb. 2009.

[7] S. Lim, D. M. Otten, and D. J. Perreault, "New AC-DC Power Factor Correction Architecture Suitable for High-Frequency Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2937-2949, April 2016.

[8] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A Family of Single-Phase Hybrid Step-Down PFC Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5271-5281, July 2017.

[9] B. Mahdavihah, and A. Prodic, "Low-Volume PFC Rectifier Based on Nonsymmetric Multilevel Boost Converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1356-1372, March 2015.

[10] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft switched high power density dc/dc converter for high power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63-73, Jan./Feb. 1991.

[11] M. H. Kheraluwala, R. W. Gascoigne, R. W. De Doncker, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc/dc converter," *IEEE Transactions on Industry Applications*, vol. 28, no. 6, pp. 1294-1301, Nov./Dec. 1992.

[12] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 805-816, Feb. 2015.

[13] S. Lim, S. Bandyopadhyay, and D.J. Perreault, "High-Frequency Isolated ac-dc Converter with Stacked Architecture," *Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1789-1796, Mar. 2017.

[14] A.J. Hanson, J.A. Belk, S. Lim, C.R. Sullivan, and D.J. Perreault, "Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency," *IEEE Transactions on Power Electronics*, Vol. 31, No. 11, pp. 7909-7925, November 2016.

[15] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of Eliminating Electrolytic Capacitor in AC/DC Power Supplies for LED Lightings," *IEEE Trans. on Power. Electron.*, vol. 24, no. 5, pp. 1399-1408, May 2009.

[16] B. Wang, X. Ruan, K. Yao, and M. Xu, "A Method of Reducing the Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC-DC Drivers," *IEEE Trans. on Power. Electron.*, vol. 25, no. 3, pp. 592-601, Mar. 2010.

[17] A. Burgio, D. Menniti, M. Motta, A. Pinnarelli, N. Sorrentino, and P. Vizza, "A Two-input Dual Active Bridge Converter for a Smart User Network Using Integrated Power Modules," *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov. 2015.

[18] P.L. Dowell, "Effects of eddy currents in transformer windings," *Proc. IEE*, vol. 113, no. 8, Aug. 1966, pp. 1387-1394.

[19] C.R. Sullivan, "Optimal Choice for Number of Strands in a Litz-Wire Transformer Winding," *IEEE Transactions on Power Electronics*, vol. 14, no.2, pp. 283-291, March 1999