

Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure Enabling Adjustable High Step-Down Conversion Ratios

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Abstract—This paper proposes a hybrid electronic and magnetic structure that enables transformers with “fractional” and reconfigurable turns ratios (e.g. 12:0.5, 12:1, 12:2). This functionality is valuable in converters with wide operating voltage ranges and high step-up/down, as it offers a means to reduce copper loss within the transformer while also facilitating voltage doubling and quadrupling. We introduce the principle of operation of the structure and present models for its magnetic and electrical behaviour. An experimental prototype capable of accommodating a widely varying input (120-380 V_{dc}) and output (5, 9, 12V) validates the operating principle and modelling of the proposed structure and achieves conversion efficiencies between 93.4% and 95.7% at 25-36 W.

I. INTRODUCTION

A widespread application of power electronic converters is as chargers for dc loads such as smartphones, tablets, and laptops. Given the portable nature of these devices and their abundance, there is significant interest in miniaturizing the chargers that power them. Such miniaturization is a challenge, however, as it requires both a reduction in the volume of the converter and an increase in efficiency to ensure that tolerable temperature rises occur within the miniaturized package [1].

Advancements in switch technologies, such as the introduction of GaN FETs, have enabled tremendous gains in the size and performance of the active switches used in power electronic converters, but advances in the passive components have lagged. Presently, passive components dominate the size and performance of power electronic converters and therefore present the major bottleneck to miniaturization. While both capacitive and inductive elements limit volume, power-stage magnetic components (i.e. those inductors and transformers that are fundamental to the power transfer mechanism of the converter) present an important limitation on size and efficiency [2].

Many power electronic converters rely on transformers to satisfy isolation safety requirements and to achieve the bulk of their voltage conversion ratio. For example, wall chargers for conventional USB-powered portable devices must interface at their input to the ac grid (up to 375 V peak voltage in regions employing a 240 Vac grid) and must step-down to as low as 5 Vdc at their output, corresponding to a 75:1 voltage conversion ratio. To achieve such step-down, it is typical to employ a transformer with a large turns ratio (e.g. 22:1) [3]. This

demanding specification aggravates the volume and efficiency limitations of the transformer for two key reasons.

Firstly, in applications where the transformer processes low voltages and high currents (as in the output of many converters), it is likely that the copper loss of the transformer far outweighs the core loss, and this imbalance compromises the efficiency of the transformer. For a given transformer conversion ratio (e.g. 22:1), the choice of the number of primary and secondary turns used to implement this ratio provides a means to balance core and copper loss inside the transformer. Specifically, as the number of turns is scaled down, copper loss is reduced at the cost of increased core loss. In applications with low voltages and high currents, this is the desired trade-off. However, this trade-off is fundamentally limited since fractional turns cannot be employed in a conventional transformer – at minimum a single full turn is required. If the transformer losses are not balanced after scaling down to a single-turn on either of the windings, one must either accept the reduced efficiency of the transformer or find another means to optimize loss (typically by increasing the size and window area of the transformer core).

A second limitation of transformers requiring large turns ratios is that placing a high number of turns around a core can in itself be problematic or unfeasible. This is particularly important when planar transformers, which offer tremendous potential for improved fabrication and miniaturization [4]–[6], are employed. In a planar transformer windings are routed as traces on a printed circuit board (PCB), and these traces must adhere to the trace width and spacing fabrication requirements of the PCB. Thus, in addition to meeting current and voltage requirements, the trace width and trace-to-trace spacing must each be wide enough to meet the PCB fabrication requirements. Not only does this manufacturing constraint increase the resistance and copper loss of the transformer, it creates the possibility that a required number of turns cannot be accommodated at all in a given core window width.

Finally, in many power electronic converters where a transformer is employed to achieve large voltage conversion ratios, there is also a need to accommodate wide operating ranges. For example, Universal Serial Bus - Power Delivery (USB PD) wall chargers must typically accommodate universal ac voltage (85 - 265 Vac) at their input, while regulating to

specific voltages between 5 and 20 V_{dc} at their output [7]. In conventional designs, these wide operating ranges are managed by changing the operating point of the regulating converter (e.g. by changing the duty-cycle of a flyback converter). However, the combination of the large voltage conversion ratios and the large variations in conversion ratios represent a significant design challenge that compromises efficiency and limits the ability to miniaturize the system [3]. Similar constraints exist in other wide-output-range applications such as Dynamic Voltage Scaling (DVS) for electronic loads and Adaptive Power Tracking for rf amplifiers.

This paper proposes a hybrid magnetic/electronic structure that realizes a transformer with an effective fractional and reconfigurable conversion ratio. Together, these qualities enable miniaturization of the transformer stage in converters where variable high step-up/down ratios are required. The proposed structure is called a “Variable-Inverter-Rectifier-Transformer” (VIRT), named this way because it fundamentally connects the rectifier stage (or inverter, or both) of a converter to the magnetic structure of the transformer and through this hybridization enables variable conversion ratios. While hybridization of passive and active electronic elements has been used to a limited extent in some applications (e.g., for rf power combining/matching [8], [9] and actively-controlled antennas [10]–[14]) this largely represents an untapped direction in power electronics, with significant potential benefits in many applications.

II. PRINCIPLE OF OPERATION

An example VIRT structure is shown in Fig. 1a. Here, two full-bridge rectifiers are distributed around a magnetic core and connected through two half-turns on the secondary side. The primary winding is not shown but it comprises an arbitrary number of turns wound around the center-post. The two rectifiers are named A and B. Rectifier A comprises the half-bridge cells labelled A1 and A2, and rectifier B, cells B1 and B2. Each half-bridge cell is directly connected to the output bus through the terminals labelled $+V_o$ and GND , for example through power and ground planes that are routed outside the magnetic core.

Each rectifier can be operated in full-bridge (FB), half-bridge (HB), or “zero” mode. For example, if rectifier A is operated in FB mode, then both A1 and A2 are active and switching as a conventional full-bridge rectifier. In HB mode, cell A1 operates as a conventional HB rectifier while A2 is held in the low state. In zero mode, both cells A1 and A2 are held in the low state to provide an effective ac short of that section of the winding.

The principle of operation can be intuitively understood by considering the path of the induced secondary-side current. For example, consider operating in a full-bridge/full-bridge (FB/FB) manner in which rectifiers A and B are both in FB mode and cell A1 is switched in-phase with cell B1. Assume that flux through the core is generated by applying an ac voltage with peak V_p onto the N_p primary turns such that ac current is induced in the secondary winding. When

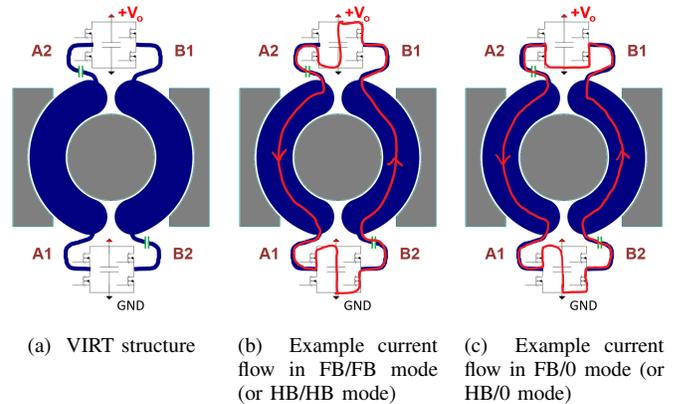


Fig. 1: (a) Illustration of the VIRT structure. The areas in grey represent the cross-section of the magnetic core on the plane where the traces are routed. The traces in blue represent the secondary-side half-turns. Note that the placement of the rectifier schematics reflects their physical location relative to the magnetic core. Blocking capacitors are indicated in green. (b) Example path of induced secondary ac current when operating in FB/FB (or HB/HB) mode and (c) FB/0 (or HB/0) mode.

operating in FB/FB mode, as illustrated in Fig. 1b, the induced current flows such that the output voltage V_o is effectively inserted twice into the secondary loop. Equating the V/N ratios in this case yields $V_o = V_p/(2N_p)$. This is equivalent to the voltage conversion ratio of an $N_p:1/2$ transformer. Now consider operation in the half-bridge/half-bridge (HB/HB) mode where both rectifiers act as half-bridges. The path of induced secondary current is identical to the FB/FB case in Fig. 1b but now only yields a single V_o insertion into the loop due to the voltage-halving action of the half-bridges. Thus, the voltage conversion ratio is changed to $V_o = V_p/N_p$, equivalent to the conversion ratio of an $N_p:1$ transformer. Similarly, by operating in the half-bridge/zero (HB/0) mode as in Fig. 1c, it is possible to achieve a conversion ratio of $V_o = 2V_p/N_p$, equivalent to an $N_p:2$ transformer. The ability to dictate the path of induced secondary side current, and in-turn to choose the effective voltage applied to the secondary loop, enables a transformer with an effective variable turns ratio of $N_p:1/2$, $N_p:1$, and $N_p:2$. Moreover, as will be described in greater detail below, this is done with reduced secondary conduction path length, improving the achievable conduction loss.

III. ELECTRICAL MODEL

To derive an electrical model of the VIRT in Fig. 1a and better elucidate the current and flux patterns in the transformer, we must first develop a magnetic circuit model. To this end, we model the current flow in the system as closed loops around the core as shown in Fig. 2a. In this figure \hat{i}_A and \hat{i}_B represent the currents that flow between the half-bridge cells in rectifiers A and B, respectively. For the purposes of modelling, these currents are drawn as returning outside the core via

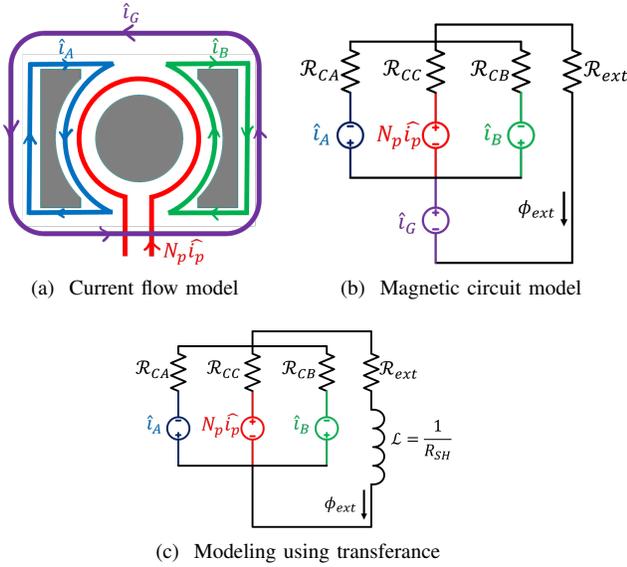


Fig. 2: Derivation of VIRT magnetic circuit model. (a) “Virtual” currents are employed such that all currents form closed loops around the core, (b) Associated magnetic circuit model, (c) MMF associated with \hat{i}_G can be modeled by a transference element \mathcal{L} , which is defined by the resistance of the ground-plane surrounding the transformer, R_{SH} .

the ground plane. Note that in practice one would expect these current components to be equal since the two-half turns and the rectifiers are identical and symmetric, and effectively form a single loop onto which current is induced by flux passing through the center-leg in Fig. 1a. In this case current is not expected to return around the core and so these current components outside of the core are deemed “virtual” - they are invoked for modelling purposes only. Another “virtual” current component \hat{i}_G is included in the model where $\hat{i}_G = \hat{i}_A = \hat{i}_B$ such that the (virtual) outer current components of \hat{i}_A and \hat{i}_B are cancelled. The resulting net current flow in this model is equivalent to the physical current that flows through each half-turn as in Fig. 1.

From this model, it is straightforward to synthesize the magnetic circuit model shown in Fig. 2b. In practice, the magnetomotive force (MMF) associated with the “short-circuit” path of \hat{i}_G is associated with a small induced voltage due to the small resistance R_{SH} of the ground-plane. The relationship between the flux and this MMF can be modeled by a transference element \mathcal{L} as shown in Fig. 2c [15]. In the limit where $R_{SH} \rightarrow 0$, $\mathcal{L} \rightarrow \infty$ and the circuit simplifies to a standard three-winding transformer with a parallel magnetic circuit. Assuming symmetry between the core legs so that $\mathcal{R}_{CA} = \mathcal{R}_{CB}$, the simplified electrical model in Fig. 3 can be derived.

A. Magnetizing inductance

In the “symmetric” operating modes (FB/FB and HB/HB) the magnetizing inductances are ideally $L_A = L_B = N_p^2 / 2(\mathcal{R}_{CC} + \frac{\mathcal{R}_{CA}}{2})$. In the “asymmetric” operating modes

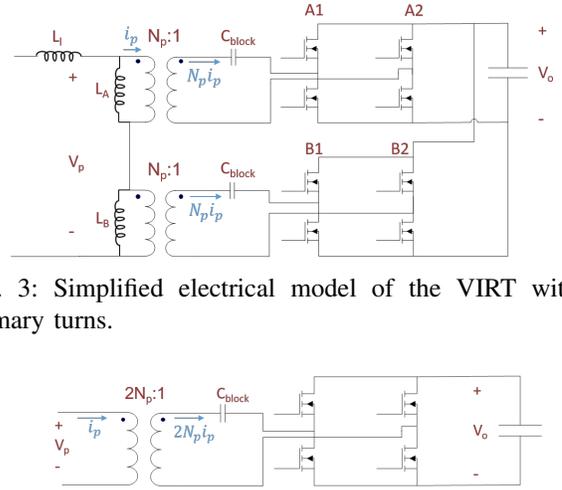


Fig. 3: Simplified electrical model of the VIRT with N_p primary turns.

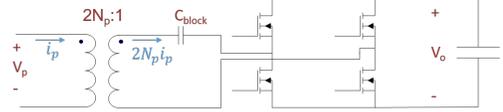


Fig. 4: Conventional $2N_p:1$ transformer connected to a full-bridge rectifier.

(FB/0 and HB/0), the MMF of the winding associated with the zeroed rectifier ideally does not contribute to the magnetizing inductance and this changes the expressions for L_A and L_B . For example, consider HB/0 operation where half-bridge cells A2, B1, and B2 are held in the low state. In the limit where the on-state resistance of the switches is zero and winding and ground plane resistance is negligible, the MMF of the winding is modeled by a transference element which approaches an open circuit (i.e. flux is ideally rejected from this part of the core). Thus, in the “asymmetric” modes, the inductances are ideally changed to $L_A = N_p^2 / (\mathcal{R}_{CC} + \mathcal{R}_{CA})$ and $L_B = 0$.

IV. COMPARISON TO CONVENTIONAL TRANSFORMER

In order to understand the performance gains of the VIRT it is insightful to compare it to the conventional $2N_p:1$ transformer plus rectifier structure in Fig. 4. For ease of comparison it is assumed that all rectifier switches can be soft-switched and conduction loss is the dominant source of loss in the switches. This can be achieved, for example, if the transformers are connected as part of an LLC converter. We treat the symmetric rectifier modes, FB/FB and HB/HB, separately from the asymmetric FB/0 and HB/0 modes since these asymmetric modes do not have a direct analogue to the conventional configuration.

A. FB/FB and HB/HB modes

In the FB/FB and HB/HB modes, the same voltage conversion ratios are achieved as when operating the conventional configuration in FB or HB mode, respectively. For example, when operating in FB/FB mode, and assuming square-wave modulation of the rectifiers for simplicity, the input to each rectifier in Fig. 3 is a square wave with peak V_o . Reflecting these voltages across the transformer in Fig. 3 yields $V_o = V_p / (2N_p)$ as expected from the discussion in Section 2. When operating the conventional $2N_p:1$ transformer in full-bridge mode, the same relationship is derived. This

equivalence is consistent with the idea of transitioning between a $2N_p:1$ transformer and an $N_p:1/2$ transformer: the voltage conversion ratio is not changed when the number of primary and secondary turns are scaled by the same multiple.

Similarly, although the VIRT requires twice the number of switches than the conventional full-bridge rectifier of Fig. 4, the conventional configuration must employ switches that are rated for twice the current. This is a result of the VIRT rectifiers being effectively paralleled in the FB/FB and HB/HB modes, allowing each of them to process half the current delivered to the output. In the conventional configuration, the full output current must be processed by the single rectifier. The net effect of this is that the conduction loss in both configurations is identical for the same transistor area. This too aligns with the expectation that the overall current flow across two transformers with the same voltage conversion ratio should not be impacted by the number of turns used to create that conversion ratio.

Viewing VIRT as an implementation of an $N_p:1/2$ transformer, the trade-off between copper loss and core loss between it and the conventional configuration is also evident. For the same output voltage V_o , both configurations have the same primary voltage V_p but the $2N_p:1$ transformer divides this voltage on twice as many turns as VIRT, reducing the peak flux density in the core and therefore reducing the core loss. Similarly, for the same current i_p in the primary, the $2N_p:1$ transformer has at least twice the dc resistance as the $N_p:1/2$ transformer, and thus experiences increased copper loss.

Note that if the same primary voltage is applied to the VIRT, core loss is fixed between the FB/FB and HB/HB modes. If the same primary current is applied, copper loss is also fixed. Transitioning between the modes does not inherently change the loss of the transformer unless each mode is operated with different primary voltages or currents.

Finally, note that the schematic of Fig. 3 is equivalent to a circuit where the two rectifiers are each connected to a single-turn wound around one of the two outer core legs. This configuration is therefore operationally identical to VIRT with the exception that it comprises longer secondary conduction path lengths. Specifically, in the VIRT the ac current induced onto the secondary windings only traverses the two half-turns, while in the alternate configuration the induced secondary current traverses two “full” single-turns.

B. FB/0 and HB/0 modes

FB and HB operation in the conventional configuration of Fig. 3 matches VIRT operation in the FB/FB and HB/HB modes, respectively. Thus the ability to operate in the FB/0 and HB/0 modes represents additional operating freedom. In this section we focus on HB/0 mode as it enables a voltage conversion ratio that is unachievable in the conventional configuration.

Consider operating in HB/0 mode such that the half-bridges A2, B1, and B2 are in the low state while A1 remains switching. The voltage conversion ratio is $V_o = 2V_p/N_p$, representing a voltage quadrupling over the FB/FB conversion

ratio that is unachievable by the conventional configuration. However, this additional operating benefit comes at the price of increased core loss. As discussed previously, assuming operation in the HB/0 mode with rectifier B zeroed, a short-circuit is effectively created around the right-side core leg which theoretically forces all of the flux generated by the primary to be routed through the left-side core leg. This leg will therefore experience up to twice the peak flux density compared to symmetric operation. This yields an increase in core loss for the same voltage applied to the primary as in the FB/FB and HB/HB cases due to the superlinear dependence of core loss on flux density.

Additionally with rectifier B zeroed, the active rectifier (A) must process the full output current (there is no longer any current sharing between the rectifiers). However, current is still induced through the zeroed rectifier (B) and it carries current comparable to the full output current. Thus, both rectifiers must be rated for the full output current while in the FB/FB and HB/HB modes they need only be rated for half the output current. Note that this detriment is mitigated if one operates in each mode at the same maximum power. For example a FB/FB rating of 5V/10A, HB/HB rating of 10V/5A, and HB/0 rating of 20V/2.5A can all be accommodated by rectifiers with the same current rating.

Finally, as discussed previously, “shorting” the winding by operating rectifier B in zero mode may also change the net magnetizing inductance in Fig. 3. For example, if the core-path reluctances are set by using a fixed gap across all three core legs, and assuming the center-post has twice the cross-sectional area of the side-posts and that the gap dominates the reluctance of the core paths, then $\mathcal{R}_{CA} = 2\mathcal{R}_{CC}$. In this case, if the symmetric operating mode yields a net primary-referred magnetizing inductance L_M then the asymmetric operating mode yields a net primary-referred magnetizing inductance $\frac{2}{3}L_M$. Alternatively, if the gap is only in the center-post, and this gap dominates the reluctance of the core, the magnetizing inductance is theoretically unaffected by the transition to HB/0 mode. The capability to use HB/0 mode to invoke a change in magnetizing inductance may be a useful feature in some resonant topologies where it can provide a mechanism for changing the voltage gain curve for a fixed load [16].

V. EXPERIMENTAL DESIGN

An experimental prototype is developed that supports a wide range of operating conditions as shown in Table I. The input voltage range of 120-380 V_{dc} (peak of universal ac voltage) and an output voltage selectable from among 5V, 9V, and 12V at 5A, 4A, and 3A, respectively, are example operating points at typical voltages and power levels. The demanding step-down ratio and wide-range of these operating points make them well-suited for application of the VIRT structure. Additionally, these points are pedagogically valuable as they represent the general case where the desired output voltage range cannot be achieved by simple voltage doubling or quadrupling. In this case, because the output voltages in the example specification are not integer multiples of one

TABLE I: Example wide range operating points

Parameter	Value
Input voltage range, V_{in}	120-380 Vdc
Adjustable output voltage, V_o (Rated output current, nominal output resistance)	5V (5A, 1 Ω); 9V (4A, 2.25 Ω); 12V (3A, 4 Ω)

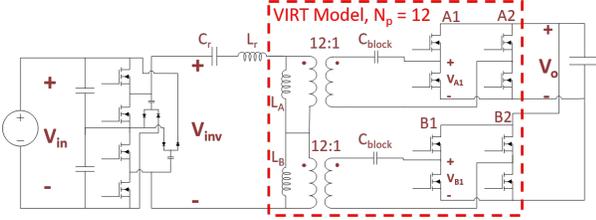


Fig. 5: Stacked-bridge LLC+VIRT converter schematic

another, additional gain variability is required beyond the scaling offered by VIRT. Similarly, choosing to employ VIRT only on the rectifier side for simplicity of demonstrating the technique, a means for dealing with the widely varying input voltage is also required. With these requirements in mind we employ a stacked-bridge LLC converter interfaced with VIRT as shown in Fig. 5. The LLC parameters are listed in Table II and the components used in the experimental prototype are shown in Table III. A labeled picture of the prototype converter is shown in Fig. 6.

A. VIRT Rectifier Implementation

The VIRT employs two full-bridge rectifiers where each switch is operated as a synchronous rectifier. The FB/FB mode, where all the switches are active, is employed for the 5V output while the HB/HB mode, where half-bridge cells B2 and A2 are held in the low state, is employed for the 9 and 12 V outputs. The result of this re-configuration is that the effective dc output voltage that the LLC must regulate is compressed from 5–12 V to 4.5–6 V.

B. VIRT Transformer Implementation

A planar transformer is employed on a two-ounce, four-layer, 0.062", FR4 printed circuit board with an EQ20/PLT+3F36 core. A PCB core thickness of 0.025" provides greater than 2.5 kV isolation between primary and secondary and the rectifier switches are placed on the top layer in order to respect this "vertical" isolation barrier [17]. The rectifiers are located symmetrically around the core and are tightly spaced to minimize the excursion of current outside

TABLE II: LLC parameters

Parameter	Value
Resonant frequency	1.2 MHz
Operating frequency range	470 - 910 kHz
Number of primary turns (N_p)	12
Resonant capacitance (C_r)	3.47 nF
Resonant inductance (L_r)	5.1 μ H
Magnetizing inductance (L_M)	38 μ H

TABLE III: Components used in prototype

Component	Value
Inverter	
GaN FETs	650V/15A GS66504B
Gate drivers	UCC27611
Signal isolators	SI8610
Isolated power	ADUM5010
Balancer diodes	MMBD3004BRM
Balancer capacitors	2x 1uF/450V
VIRT Rectifier	
GaN FETs	30V/60A EPC2023
Gate drivers	LM5113
Blocking capacitors	3x 22uF/16V
Decoupling capacitors	2x 10uF/16V per half-bridge
Output capacitors	6x 22uF/16V
LLC	
Resonant capacitor (split)	4x 3.47 nF; ea. 2x 1500pF/630V/COG + 470pF/450V/COG
Resonant inductors (split)	2x 1.79uH; ea. RM51/3F36, 3 turns 46AWG/180 Litz wire
VIRT transformer	
Core	EQ20+PLT/3F36, 0.006" gap on all legs
Primary windings	Six turns on Layer 3 and 4 connected in series, 0.019" trace width, 0.008" trace-to-trace spacing
Secondary windings	Two sets of half-turns (one set each on layers 1 and 2) connected in parallel
PCB	2oz, 4 layers, 0.063", FR4, 0.025" separation between layers 2 and 3
Control	
Controller	TMS320F28379D

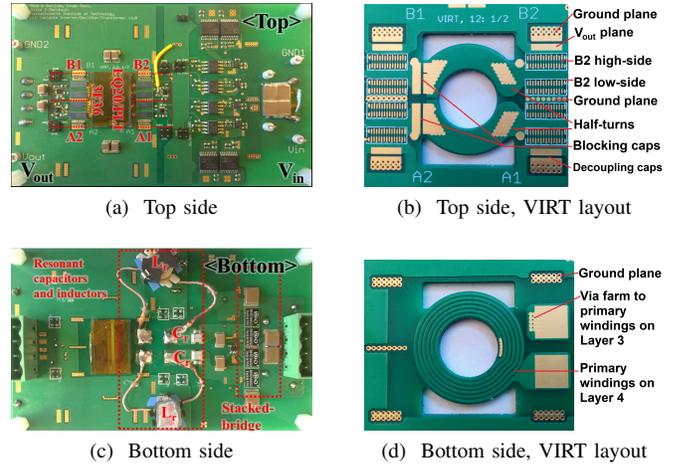


Fig. 6: Labeled experimental prototype, including close-ups of the VIRT layout. The board dimensions are 115 mm x 70 mm.

the core. Output voltage and ground planes are routed outside the transformer to provide a low-resistance path for dc current between the half-bridge cells and the output bus connection at the edge of the board.

C. Inverter Implementation

The stacked-bridge inverter can be operated in two modes to achieve voltage-halving or voltage-quartering using the "Variable Frequency Multiplier" technique as described in [18]

and [19]. The inverter is operated with voltage-halving when the input voltage is between 120 and 190 V, and voltage-quartering when the input voltage is between 190 and 380 V. The result of this re-configuration is that the ac square-wave input to the LLC resonant tank has a peak voltage range of 47.5–95 V. Note that balancer circuits are employed as shown in Fig. 12 to ensure voltage balancing between the input capacitors.

D. LLC Design

The voltage gain of the converter can be expressed in a similar manner to a classic half-bridge LLC,

$$\frac{V_o}{V_{in}} = M_{g,LLC} M_{inv} \frac{N_s}{N_p} \quad (1)$$

Where $M_{g,LLC}$ is the (variable) gain function of the LLC, M_{inv} is the gain of the inverter topology, and N_p and N_s are the number of primary and secondary turns, respectively. In the case of VIRT, N_s/N_p represents the effective transformer turns ratio which is set by the VIRT operating mode,

$$\frac{N_s}{N_p} = \begin{cases} \frac{1}{2N_p}, & \text{FB/FB mode} \\ \frac{1}{N_p}, & \text{HB/HB (or FB/0) mode} \\ \frac{2}{N_p}, & \text{HB/0 mode} \end{cases} \quad (2)$$

M_{inv} is also a controllable quantity due to the stacked inverter topology and the ability to operate in VFX mode,

$$M_{inv} = \begin{cases} 1/2, & \text{Inverter Mode 1} \\ 1/4, & \text{Inverter Mode 2 (VFX)} \end{cases} \quad (3)$$

Due to the re-configurability of the VIRT and the stacked bridge, the LLC effectively interfaces a 47.5-95 V input to a 4.5-6 V output, corresponding to a reduction in the required LLC step-down ratios from 10–76 V/V to 7.92–21.1 V/V. This 2.66 times gain variation can be reasonably accommodated by the LLC resonant tank, while the original 7.6 times gain variation would yield unacceptably large stress on the components of the LLC converter [20].

The LLC is designed using a conventional procedure as described in [20] and the resulting component values are shown in Table II. The key addition to this procedure is that one must now consider the gain curve for each output voltage and output power pair separately since they may each provide a separate effective load resistance to the resonant tank, as discussed in the Section V-E. As is conventional, the LLC is operated below resonance to achieve Zero Voltage Switching (ZVS) on the inverter switches, which operate at high voltage, and Zero Current Switching (ZCS) on the secondary-side synchronous rectifiers, which operate at high current. The selected normalized tank parameters are $Q = 0.146$ and $L_n = 7.45$ (where Q is associated with full load in the HB/HB mode), chosen to yield sufficient gain at all of the operating points while also ensuring primary-side ZVS.

Note that the resonant inductance is achieved in this case by a combination of the primary-referred leakage inductance of

TABLE IV: LLC effective load resistances for the VIRT modes

VIRT mode	Effective load resistance
FB/FB	$R_e = 32N_p^2 R_L / \pi^2$
HB/HB	$R_e = 8N_p^2 R_L / \pi^2$
FB/0	$R_e = 8N_p^2 R_L / \pi^2$
HB/0	$R_e = 2N_p^2 R_L / \pi^2$

the transformer ($\approx 2.1 \mu\text{H}$) and an external inductance ($\approx 3.5 \mu\text{H}$). This external inductance is implemented in a split manner as two series-connected $1.75 \mu\text{H}$ inductors in order to ensure that the inverter is symmetrically loaded. Similarly, the resonant capacitor is implemented as two series 6.94 nF capacitors, each directly connecting to an inverter switching node as shown in Fig. 6d.

E. Effective load resistance for LLC design

The conventional LLC design procedure requires that the load resistance, R_L , be reflected through the output rectifier and across the transformer to synthesize an effective load resistance in parallel with the net primary-side magnetizing branch [20]. Although the VIRT employs multiple rectifiers, a similar method can be used as in the conventional configuration to synthesize the effective load resistance.

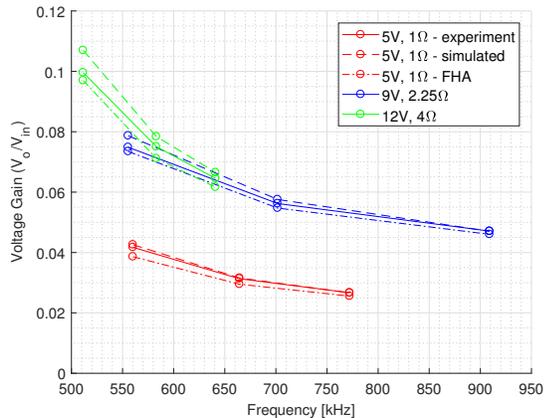
In a conventional LLC design with a single full-bridge rectifier connected to the secondary of an $N_p:N_s$ transformer, the load resistance R_L is mapped to the primary-side magnetizing branch as $R_{e,FB} = \frac{8}{\pi^2} \left(\frac{N_p}{N_s}\right)^2 R_L$. In the case of operating the VIRT in FB/FB mode, the same equation applies except that $N_s = 0.5$, yielding, $R_{e,FB/FB} = \frac{32}{\pi^2} (N_p)^2 R_L$. The effective load resistance in the remaining cases can be similarly computed and their values are listed in Table IV.

VI. EXPERIMENTAL RESULTS

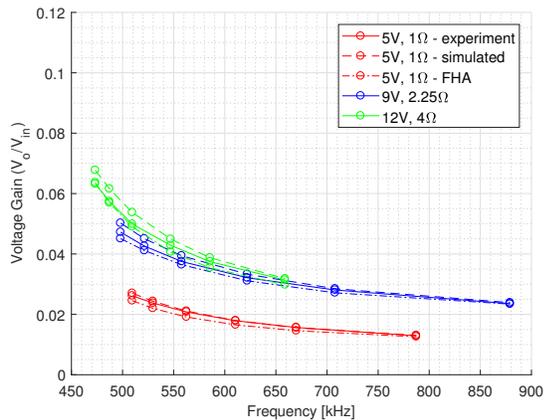
The gain versus operating frequency curves are extracted from the experimental prototype and are compared to an idealized simulation of the circuit in Fig. 5 and a conventional fundamental harmonic approximation (FHA) analysis. The results for Inverter Mode 1 operation are shown in Fig. 7a and Inverter Mode 2 in Fig. 7b. The experimental results are in good agreement with simulation, within 7% of the expected gain at low frequencies and with excellent matching at higher frequencies, indicating that the circuit in Fig. 5 well models the physical system.

Both the experimental and simulated results yield LLC gains that are larger than the results of the FHA analysis, as is expected for operation below resonance [20]. However, FHA remains an effective first-pass design tool for this LLC converter and the use of VIRT does not further compromise its use.

Experimental waveforms demonstrate the inherent symmetry of the rectifiers in the VIRT. For example Fig. 8 shows V_{A1} and V_{B1} (ref. Fig. 5) in the 9V output, 120V input, Inverter Mode 1, HB/HB VIRT mode case, $f_{sw} = 558.5 \text{ kHz}$ with $R_L = 2.25 \Omega$ ($P_{out} = 36W$). The rectifier voltages match closely with only minor differences in the parasitic oscillations



(a) Inverter Mode 1



(b) Inverter Mode 2

Fig. 7: Voltage gain curves for each inverter mode. In all cases there is good agreement between the experimental results and the simulated and FHA results.

that occur during the discontinuous conduction state associated with below-resonance operation of the LLC. This equivalence verifies that the VIRT operates symmetrically and that the “series transformer” model in Fig. 3 is appropriate.

The efficiency of the converter versus input voltage is shown in Fig. 9. The results show that the efficiencies of the different operating conditions are well grouped in each inverter mode, ranging from 94.4–95.7% in Inverter Mode 1 and 93.4–95.2% in Inverter Mode 2, demonstrating the effectiveness of VIRT in enabling good performance over large output voltage variation. The reduction in efficiency in Inverter Mode 2 is attributable to the mode change of the inverter rather than the operation of the VIRT. For example, the 380V Inverter Mode 2 cases excite the LLC resonant tank in a theoretically identical manner as the 190V Mode 1 cases (i.e. V_{inv} are theoretically identical), and in experiment they are observed to yield nearly identical rectifier voltage waveforms, thus suggesting the inverter mode shift as the source of the additional loss.

A. Explicit demonstration of VIRT turns-ratio variability

The experimental results presented above validate the derived model and demonstrate that the VIRT can be deployed

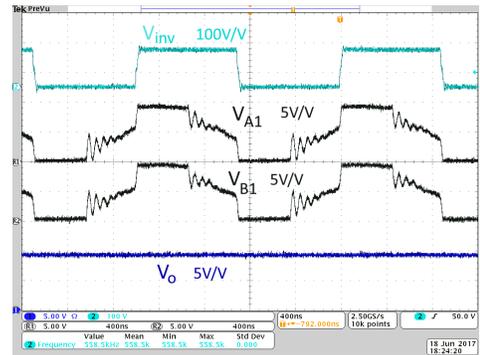


Fig. 8: Voltage waveforms for 9V output, 120V input, Inverter Mode 1, and HB/HB VIRT mode, $f_{sw} = 558.5$ kHz with $R_L = 2.25 \Omega$ ($P_{out} = 36W$). The rectifier voltage waveforms show excellent matching and demonstrate the expected symmetric operation of the A1 and B1 rectifiers.

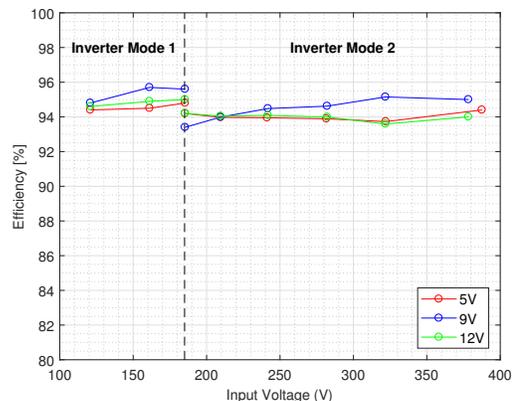


Fig. 9: Power-stage efficiency of the converter measured at full load for each output voltage (25, 36, 36 W, for 5V, 9V, and 12V, respectively). The efficiencies are well grouped for each inverter mode due to the properties of the VIRT.

with other variable-gain “converter blocks,” such as an LLC and an inverter with mode-shifting capability, to realize an architecture capable of wide voltage-conversion capability. Embedded in these results is the voltage scaling that is enabled by the turns-ratio variability of VIRT. For clarity, in this section we explicitly demonstrate the impact of VIRT operation by considering an example case where the gains of the LLC and the inverter are held constant.

Consider the change from FB/FB mode to HB/HB mode. In order to keep the LLC voltage gain constant, Table IV dictates that the resistance in the HB/HB mode must be four times larger than in the FB/FB mode case. To this end, consider an example case where we operate in FB/FB mode with a 120V input, Inverter Mode 1, and a load resistance of 1Ω to achieve an output voltage of 3V. Then, to keep the LLC gain constant in HB/HB mode, we operate with 120V input, Inverter Mode 1, and a load resistance of 4Ω , and expect to achieve output voltage doubling to 6V at the same operating frequency. The results of this comparison are shown in Fig.

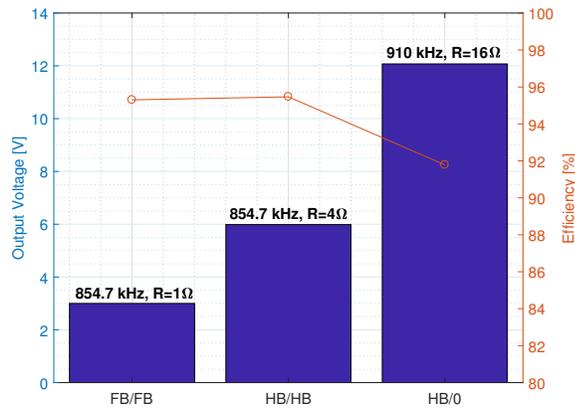


Fig. 10: Comparison of VIRT operating modes with constant effective output resistance, R_e , operating with Inverter Mode 1.

10. Voltage doubling to 6V is achieved in the HB/HB mode and the efficiency remains nearly constant (95.3% vs. 95.4%) as expected from the discussion in Section IV-A.

When operating in the HB/0 mode at the same effective output resistance, voltage quadrupling is also achieved. However the LLC gain curve is changed due to the (approximately) two-thirds reduction in magnetizing inductance explained in Section IV-B. Thus, a larger operating frequency is required to achieve the same LLC gain as in the FB/FB and HB/HB modes. Finally, we observe the reduction in efficiency (91.8%) in this operating range, attributable to the increase in core loss associated with asymmetric VIRT operation. Note however that alternative means of achieving voltage quadrupling may yield similar or worse detriments to efficiency - a detailed comparison to an alternative “converter gain block” must be made to correctly assess the value of HB/0 operation in a particular application.

VII. CONCLUSION

In this work, a hybrid electronic and magnetic structure capable of fractional and reconfigurable conversion ratios is presented. An example of the proposed structure, named VIRT, connects the rectifier stage of a converter to the magnetic structure of a transformer, and reconfigurability is achieved by controlling the operating mode (i.e. FB, HB, or zero) of the rectifier in conjunction with flux paths and current paths used in the transformer. A magnetic circuit model employing “virtual” currents enables derivation of an electrical circuit model, and an experimental prototype verifies the operation of the structure, demonstrating the achievement of fractional and variable conversion ratios. The proposed structure is valuable for applications with wide operating voltage ranges that require large and wide-range step-up/down conversion, such as USB wall chargers, and offers strong potential for miniaturization in these applications.

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REFERENCES

- [1] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, “Design and analysis of thermal management for high-power-density converters in sealed enclosures,” in *Proceedings of APEC 97 - Applied Power Electronics Conference*, vol. 1, Feb 1997, pp. 405–412 vol. 1.
- [2] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, “Opportunities and Challenges in Very High Frequency Power Conversion,” in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2009, pp. 1–14.
- [3] R. Taylor, “Universal AC Input, 5V@2.1 Dual Port Smart USB Charger,” Texas Instruments, Tech. Rep. PMP7389, March 2012. [Online]. Available: <http://www.ti.com/tool/PMP7389#TechnicalDocuments>
- [4] Z. Ouyang and M. A. E. Andersen, “Overview of planar magnetic technology – fundamental properties,” *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4888–4900, Sept 2014.
- [5] S. Lim, A. J. Hanson, J. A. Santiago-Gonzalez, and D. J. Perreault, “Capacitively-aided switching technique for high-frequency isolated bus converters,” in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 98–105.
- [6] M. Chen, K. K. Afridi, S. Chakraborty, and D. J. Perreault, “Multitrack Power Conversion Architecture,” *IEEE Transactions on Power Electronics*, no. 1, pp. 325–340, January 2017.
- [7] “Universal Serial Bus Power Delivery Specification,” Hewlett-Packard Company, Intel Corp., Microsoft Corp., Renesas, STMicroelectronics, and Texas Instruments, Tech. Rep. Rev. 2.0, V1.2., Aug. 2016.
- [8] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, “Distributed Active Transformer - A New Power-Combining and Impedance-Transformation Technique,” *IEEE Transactions on Microwave Theory and Techniques*, Jan. 2002.
- [9] —, “Fully Integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture,” *IEEE Journal of Solid-State Circuits*, March 2002.
- [10] V. F. Fusco and Q. Chen, “Direct-signal Modulation Using a Silicon Microstrip Patch Antenna,” *IEEE Transactions on Antennas and Propagation*, no. 6, pp. 1025 – 1028, June 1999.
- [11] J-C Ke, et. al., “Implementation of a Multi-Beam Switched Parasitic Antenna for wireless applications,” in *IEEE Int. Symp. on Antennas and Propagation*, June 2007, pp. 3368–3371.
- [12] D. V. Thiel and S. L. Smith, *Switched Parasitic Antennas for Cellular Communications*. Norwood, MA: Artech House, 2002.
- [13] A. Babakhani, et. al., “A Near-Field Modulation Technique Using Antenna Reflector Switching,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 188–189.
- [14] A. Arbabian, et. al., “A 90GHz Carrier 30GHz Bandwidth Hybrid Switching Transmitter with Integrated Antenna,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010.
- [15] E. R. Laithevaite, “Magnetic equivalent circuits for electrical machines,” *Proceedings of the Institution of Electrical Engineers*, vol. 114, no. 11, pp. 1805–1809, November 1967.
- [16] H. Hu, X. Fang, F. Chen, Z. J. Shen, and I. Batarseh, “A Modified High-Efficiency LLC Converter With Two Transformers for Wide Input-Voltage Range Applications,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1946–1960, April 2013.
- [17] R. Tarzwell and K. Bahl, “High Voltage Printed Circuit Design & Manufacturing Notebook,” SIERRA Proto Express, Tech. Rep., 2004. [Online]. Available: <http://www.magazines007.com/pdf/High-Voltage-PCDesign.pdf>
- [18] W. Inam, K. K. Afridi, and D. J. Perreault, “Variable Frequency Multiplier Technique for High-Efficiency Conversion Over a Wide Operating Range,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, no. 2, pp. 335–343, June 2016.
- [19] L. Gu, W. Liang, M. Praglin, S. Chakraborty, and J. Rivas-Davila, “Universal line input power factor preregulator using vfx technique,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 1810–1815.
- [20] H. Huang, “Designing an LLC Resonant Half-Bridge Power Converter,” in *Texas Instruments Power Supply Design Seminar SEM1900*, no. TI Literature Number: SLUP263, 2010.