

# A Wide Operating Range Converter Using a Variable-Inverter-Rectifier-Transformer with Improved Step-Down Capability

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**Abstract**—This paper proposes the design of a dc-dc converter for portable charger applications that uses a Variable-Inverter-Rectifier-Transformer (VIRT) with improved step-down capability. The proposed design leverages an improved rectifier structure to achieve high efficiency (up to 96.2 %) across a wide range of input (120 - 380 V) and output voltages (5 - 20 V) at an output power of up to 50 W. The new rectifier configuration incorporates a bypass switch which allows for a full utilization of the effective transformer core area across all modes of operation, improving the core loss of the transformer. Moreover, a hybrid Litz-PCB construction of the VIRT transformer further reduces copper loss by mitigating skin and proximity effects, and enables integration of the LLC converter magnetics into a single component. A hardware prototype of the converter achieves a box power density of 23.2 W/in<sup>3</sup>, and maintains high efficiency and low worst-case power loss across the wide input and output voltage ranges.

## I. INTRODUCTION

In the consumer electronic market, there has been a great interest in miniaturizing chargers that power portable electronics such as smartphones, tablets, and laptops. In parallel with this trend, advances in power semiconductors such as Gallium Nitride FETs have opened up opportunities for miniaturization and improved efficiency of these converters. However, advancement in passive components such as inductors and transformers has not kept pace with that of power semiconductor technology. Consequently, the performance of many power converters, including size and efficiency, is largely determined by passive components, especially magnetic components [1].

In portable charger applications, a transformer with a large turns ratio is often implemented to achieve the large step-down conversion requirement from the high grid voltage to the low voltage levels needed for the output while simultaneously satisfying safety isolation requirements. This type of large step-down, low-output-voltage design often yields a transformer in which copper loss dominates over core loss [2]. In this case, the transformer turns ratio is implemented with the minimum number of turns, typically associated with the secondary winding comprising a single turn. However, if the transformer losses are not optimized after the secondary winding reaches a single turn, one has traditionally had to accept the losses or find some other means to reduce transformer loss such as using a larger transformer core or changing the turns ratio.

Furthermore, converters with these large step-down transformers are often required to accommodate wide operating

ranges. As a notable example, a Universal Serial Bus – Power Delivery (USB-PD) wall charger needs to be designed to accommodate universal ac voltage (85 – 265 V<sub>ac</sub>) from the grid as an input and provide a regulated output voltage between 5 V<sub>dc</sub> and 20 V<sub>dc</sub> [3]. This design requirement imposes a great challenge to implementing a compact, efficient converter design owing to the large, variable step-down ratios and large variations in operating voltages.

This paper explores the use of the recently proposed Variable-Inverter-Rectifier-Transformer (VIRT) structure that enables transformers that provide effective fractional turns and reconfigurable transformation ratio [2]. The effective fractional turns enabled by the VIRT provide a designer with a means to further scale down the absolute number of turns, reducing copper loss in order to optimize the overall transformer loss. The variable effective conversion ratio of the VIRT has been shown to be very promising to accommodate wide operating voltages. However, the proposed structure in [2] still suffers from an increased transformer core loss when operating in asymmetric operating modes in which the core is not fully utilized.

In this work, we implement the VIRT structure with an improved rectifier topology that utilizes a “bypass switch” enabling dramatic core loss reduction in the asymmetric mode associated with high voltage gain operation. Furthermore, a hybrid Litz-PCB construction of the VIRT transformer is implemented, which further improves copper loss of the transformer and provides the benefits of integrated leakage magnetics for the power converter. Section II of the paper introduces the principle of operation of the new VIRT system. Section III and IV of the paper describe the design and implementation of an LLC-based dc-dc converter implementing the proposed VIRT approach, while Section V presents experimental results from the proposed system. Finally, Section VI concludes the paper.

## II. PRINCIPLE OF OPERATION

The proposed VIRT system is designed to operate as part of an LLC converter for a USB PD charger system that can accommodate the wide desired output voltage range (5-20 V) through rectifier mode changes. Fig. 1a shows the proposed VIRT structure implemented with an EQ type core, and Fig. 2 shows electrical models of the proposed structure, respectively. A primary winding around the center post of the core (not shown) generates flux though the center post. Two full-bridge rectifiers named A and B, respectively, are

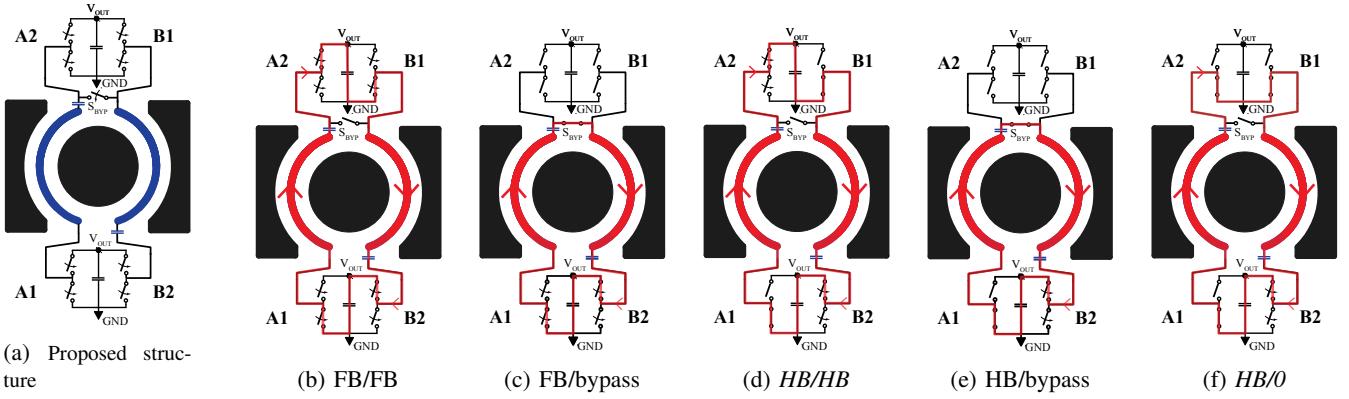


Fig. 1: Proposed VIRT structure with the bypass switch and induced current flows on the secondary side in each operating mode. *HB/HB* and *HB/0* are conventional VIRT modes and are improved by the *FB/bypass* and *HB/bypass* modes, respectively.

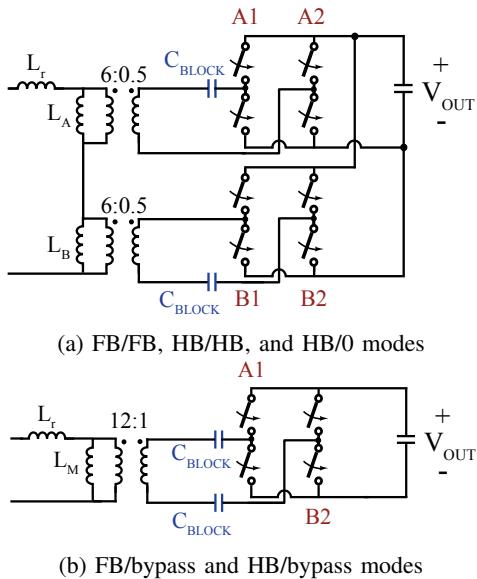


Fig. 2: Electrical models of the proposed VIRT structure in Fig. 1.

distributed around the magnetic core and each connected to a secondary half-turn around the center post. Rectifier A consists of two half-bridge cells labelled A1 and A2, and Rectifier B, cells B1 and B2. Each cell is connected to the output bus terminals,  $V_{OUT}$  and GND through power and ground planes that are routed outside the magnetic core [2]. Finally, the ac node of rectifier cell A2 and rectifier cell B1 are connected via a bidirectional “bypass switch”  $S_{BYP}$  that enables additional operating modes as described below.

With the bypass switch open, the system operates in the same modes as described for the VIRT LLC converter described in [2]. For this case, each rectifier can be operated as a full-bridge (FB), half-bridge (HB), or “zero” mode. When a rectifier is operated in FB mode, both half-bridge cells (e.g. A1 and A2) are active, switching in opposition as a full-bridge. In HB mode, only one half-bridge cell in a full-bridge rectifier is active while the other cell is shorted to ground. In zero mode, both cells are shorted to ground, effectively creating an ac short-circuit path for the induced

TABLE I: Summary of VIRT operation including bypass modes. Detailed derivations for FB/FB, HB/HB, and HB/0 modes are covered in [2].

VIRT mode	Description	Effective Turns Ratio	Mode Type	“Net” Magnetizing Inductance <sup>1</sup>
FB/FB (Fig. 1b)	All switches active	$N_p : 1/2$	Symmetric	$L_M = \frac{N_p^2}{2R_{CC}}$
HB/HB (Fig. 1d)	A2, B2 active A1, B1 short to GND	$N_p : 1$	Symmetric	$L_M$
FB/byp (Fig. 1c)	A1, B2 active Bypass switch on	$N_p : 1$	Bypass	$L_M$
HB/0 (Fig. 1f)	A1, A2, B1 short to GND B2 active	$N_p : 2$	Asymmetric	$\frac{2}{3}L_M$
HB/byp (Fig. 1e)	A1 short to GND B2 active, Bypass switch on	$N_p : 2$	Bypass	$L_M$

current; this has the effect of rejecting ac flux changes through the associated outer core leg.

In this work, we achieve new operating modes through introduction of the bypass switch ( $S_{BYP}$  in Fig. 1a). With the bypass switch closed and all switches of rectifier cells A2 and B1 left open, additional operating modes are available in which Cells A1 and B2 can be utilized together, switching in opposition to operate as a full-bridge rectifier (FB/bypass) or with one of cells A1 and B2 shorting its input to common (GND or  $V_{OUT}$ ) and the other operating as a half-bridge (HB/bypass).

In a USB-PD application where the output voltage may be regulated to any of 5 V, 9 V, 15 V, or 20 V, one can select among the various VIRT modes in Fig. 1b-1f to support the different output voltages. A summary of all VIRT modes including the bypass modes is shown in Table I. “Net” magnetizing inductance<sup>1</sup> in Table I is calculated assuming an equal gap in each of the three core legs, with the outer core legs each having half the cross-sectional area as the center leg; different results would be achieved with a “center-post-only” gap or with different core area or gap distributions. The “effective turns ratio” gives the same ac-dc conversion ratio as would be found in a conventional LLC converter with a single-turn secondary and a single full-bridge rectifier.

As shown in Table I, the HB/0 and HB/bypass modes offer four times larger gain (from ac primary input voltage to dc output voltage) than the FB/FB mode. Thus, it is sensible to

<sup>1</sup>“Net” magnetizing inductance means  $L_A + L_B$  in Fig. 2a and is derived through modeling magnetic circuit as shown in Fig. 3.

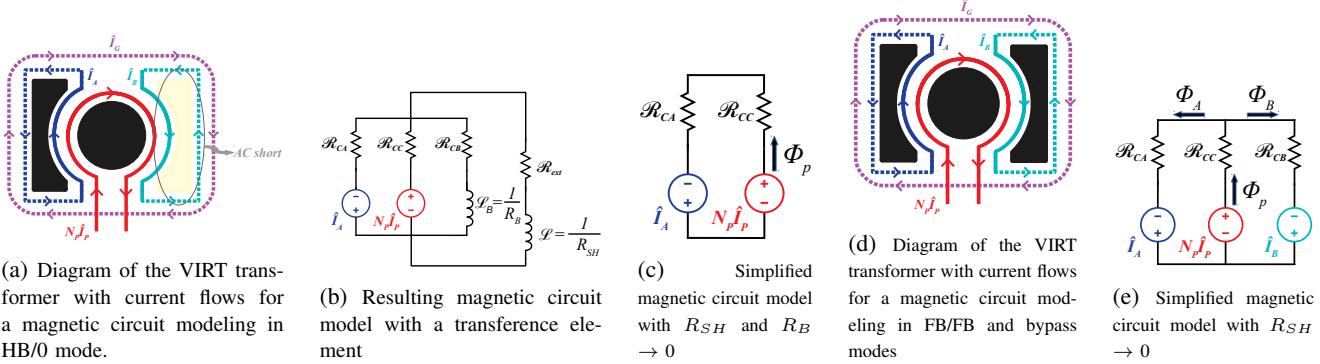


Fig. 3: Magnetic circuit derivation of VIRT model. Solid lines correspond to real components of currents, while dotted components correspond to virtual components of currents invoked for modeling purpose [2].

utilize HB/0 or HB/bypass to achieve 20 V output operating points, and FB/FB to achieve 5 V output operating points. While both HB/0 and HB/bypass modes offer the same effective ac-dc conversion ratio, the HB/bypass mode can achieve lower losses for the same conversion requirement. In HB/0 mode an ac short is effectively created around one leg of the core ideally rejecting the ac flux changes though that section of the core as illustrated in Fig. 3a. This causes the flux through the center post to be routed through only one of the outer core legs as shown in Fig. 3c, increasing the peak flux density through that leg and increasing core loss [2]. The proposed VIRT structure with the bypass switch in Fig. 1a eliminates this issue. The HB/bypass switching mode enables the same gain characteristics to be achieved as HB/0 while maintaining full utilization of the core material.

Note that  $S_{BYP}$  carries bidirectional current when on and blocks bidirectional voltage when off and can be implemented using two MOSFETs. The “bypass” modes enabled by this switch redirect the current path such that it bypasses the rectifier half-bridge cells on one side of the VIRT transformer and configures the un-bypassed half-bridge cells as either a FB or HB as shown in Fig. 1c and 1e, respectively. HB/bypass mode in Fig. 1e utilizes the entire effective core area of the transformer as opposed to HB/0 mode by allowing the flux generated by the primary side current to be routed through both outer legs of the core as shown in Fig. 3e, which in turn achieves full utilization of the outer core legs and hence reduced core loss. Therefore, the bypass switch provides a means to achieve improved system efficiency in the higher output voltage regime while adding only modest complexity to the system.

### III. EXPERIMENTAL DESIGN

In order to verify the benefits of the bypass modes, a reconfigurable resonant dc-dc converter with the proposed VIRT with bypass switch has been designed and built. The dc-dc converter utilizes an LLC resonant tank and stacked half-bridge inverter as shown in Fig. 4. The input voltage is defined by two ranges: 120 - 170 V<sub>dc</sub> and 310 - 380 V<sub>dc</sub>. These correspond to the peak of ac line for low-voltage range (85 - 120 V<sub>ac</sub>) operation and high-voltage range (220 - 268 V<sub>ac</sub>) operation, respectively. A stacked half-bridge structure

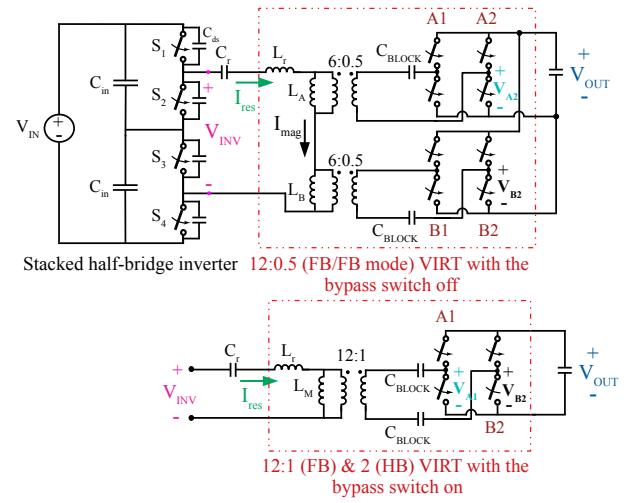


Fig. 4: Circuit schematics for the VIRT with the bypass switch.

uses two different modes to compress the input voltage range as described in Section III-A. The VIRT and LLC work interactively to regulate the output voltage,  $V_{OUT}$ , to 5 V (25 W rating), 9 V (36 W rating), 15 V (45 W rating), and 20 V (50 W rating), respectively. These specifications correspond to those for a USB-PD charger [3].

#### A. Stacked Half-bridge Inverter

By use of the Variable-Frequency Multiplier (“VFX”) technique, a stacked half-bridge structure can operate with two different modes to compress the ac voltage range seen by the transformer. This technique yields an ac square waveform at the inverter output with an amplitude that is half (Mode 1) or quarter (Mode 2, “VFX”) the dc input voltage  $V_{IN}$ . The design benefits by utilizing Mode 1 in the low voltage input range (120 - 170 V) and Mode 2 in the high-voltage input range (310 - 380 V), respectively, as shown in Fig. 5 [4]. Due to this input voltage compression, for a range of  $V_{IN}$  of 120 - 380 V, the peak square-wave voltage amplitude range the LLC resonant tank and transformer has to handle is only 120 - 190 V. Furthermore, a stacked half-bridge inverter structure makes it easier to achieve the primary-side zero voltage switching (ZVS) by effectively reducing capacitive

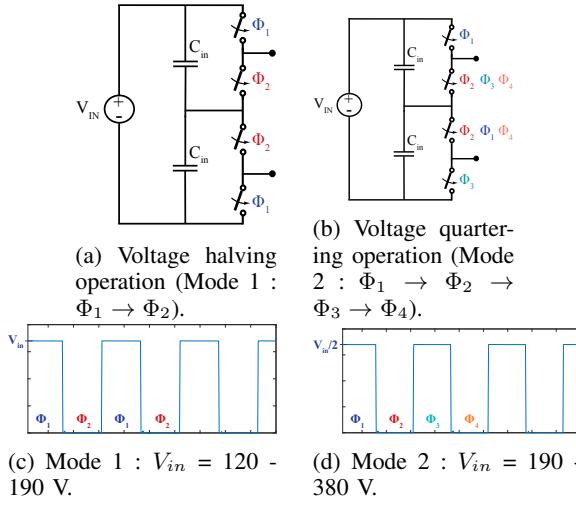


Fig. 5: Operations of the stacked half-bridge structure. Note that each  $C_{in}$  holds  $\frac{1}{2}V_{IN}$ .

TABLE II: Minimum and maximum LLC voltage gains ( $M_{g,LLC}$ ), effective load resistances ( $R_{eff}$ ), and quality factors ( $Q_e$ ) for all operation modes of the VIRT with the bypass switch

	<b>FB/FB</b>	<b>FB/bypass</b>	<b>HB/bypass I</b>	<b>HB/bypass II</b>
$R_{load}$ ( $\Omega$ )	1	2.25	5	8
$V_{OUT}$ (V)	5	9	15	20
$P_{OUT}$ (W)	25	36	45	50
Minimum $M_{g,LLC}$ (V/V)	1.26	1.14	0.95	1.26
Maximum $M_{g,LLC}$ (V/V)	2.00	1.80	1.50	2.00
$R_{eff}$ ( $\Omega$ )	467	263	146	233
$Q_e$	0.10	0.17	0.31	0.19

energy associated with the device output capacitances. More details on achieving ZVS on the inverter are covered in Appendix B.

### B. LLC Resonant Tank Design

In order to design a LLC resonant tank in the proposed DC-DC VIRT system, additional voltage gain from the stacked half-bridge inverter and VIRT rectifier needs to be taken into account. The voltage gain of the DC-DC VIRT system can be expressed as shown in Equation (1).

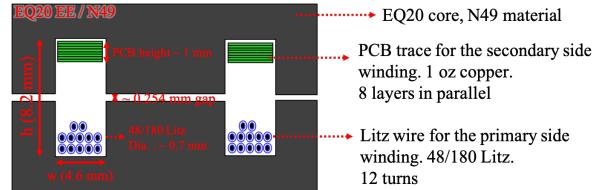
$$\frac{V_{out}}{V_{in}} = M_{g,LLC} M_{inv} \frac{k}{n}, \quad (1)$$

where  $M_{g,LLC}$  is the voltage gain of the LLC resonant tank,  $M_{inv}$  is the voltage gain of the stacked half-bridge inverter,  $n$  is the physical turns ratio of the transformer, and  $k$  is the voltage gain of VIRT rectifier stage, respectively.

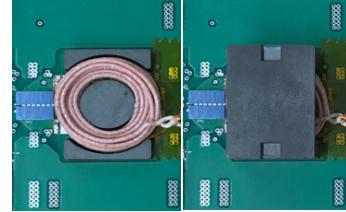
$M_{inv}$  is  $\frac{1}{2}$  in VFX Mode 1 and  $\frac{1}{4}$  in VFX Mode 2 [4]. Note that Mode 1 is utilized for the low-range  $V_{IN}$  associated with U.S. and Japan ac voltages (120 - 170 V) and Mode 2 for the high-range  $V_{IN}$  (310 - 380 V) associated with European ac voltages.  $n$  is the physical turns ratio of the transformer, 12 in our proposed design. Finally,  $k$  is  $\frac{1}{2}$  for FB/FB mode, 1 for FB/bypass mode, and 2 for HB/bypass mode.

TABLE III: LLC resonant tank design

Resonant Frequency ( $f_{res}$ ) MHz	$f_{sw}$ range (kHz) FHA analysis	Number of primary-side turns ( $N_p$ )	Magnetizing Inductance $L_m$ ( $\mu H$ )	Resonant Inductance $L_{res}$ ( $\mu H$ )	Resonant Capacitance $C_{res}$ (nF)
1.15	680 - 1300	12	20.5	5.5	3.3



(a) Diagram of the hybrid transformer construction.



(b) Picture of the hybrid transformer construction.

Fig. 6: Hybrid Litz-PCB construction of VIRT transformer.

Shown in Table II are minimum and maximum LLC voltage gains ( $M_{g,LLC}$ ), effective load resistances ( $R_{eff}$ ), and quality factors ( $Q_e$ ) for all the operation modes of the VIRT with the bypass switch. Note that the range of  $M_{g,LLC}$  is from 0.95 to 2 across all the operation modes owing to the input and output voltage compression from the stacked half-bridge inverter and VIRT rectifier, respectively. This results in a max-to-min gain ratio  $\frac{M_{g,LLC,max}}{M_{g,LLC,min}} = 2.11$ . If one instead were to use a conventional LLC converter with a half-bridge inverter and single full-bridge rectifier, the max-to-min gain ratio  $\frac{M_{g,LLC,max}}{M_{g,LLC,min}}$  would have been 12.7, placing an unacceptable stress on the LLC resonant tank to reach all operating points. This reduced range of the LLC voltage gain ensures efficient performance of the LLC converter. Finally, the LLC resonant tank design parameters have been set as shown in Table III through the loss optimization process with the fixed resonant inductor which is entirely replaced by a leakage inductance of the transformer as discussed in Section III-C. More details on designing LLC converter with VIRT and achieving ZVS on the primary-side inverter are available in Appendix A and B.

### C. Hybrid Litz-PCB Transformer Construction

Planar magnetics have gained increasing popularity owing to miniaturization and ease of fabrication [5]–[7]. We have adopted a hybrid construction [8], in which the primary winding is built with a litz wire and the fractional-turn secondary is constructed in a planar fashion with printed windings. This approach, shown in Fig. 6, can further improve performance of the transformer as compared to a fully planar design while achieving miniaturization. This improved performance comes from a reduced primary-copper loss as a planar construction of the high-turns-count primary tends

TABLE IV: List of main components in the DC-DC VIRT with the bypass switch

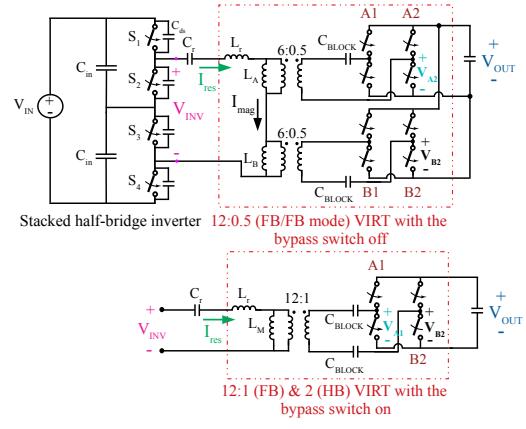
Stacked Half-Bridge Inverter	
GaN FETs	EPC2050 (350 V / 25 A)
Gate drivers	LMG1210
Isolated power	ADUM5210
Balancer diodes	MMBD3004BRM
Balancer capacitors	10 $\mu\text{F}$ (1812) / 450 V
VIRT Rectifier	
Rectifier switches	TPN2R703NL (30 V / 45 A)
Gate drivers	LM5113
Bypass switches	EPC2023 (30 V / 90 A)
Gate driver (bypass)	UCC27611
Isolated power and digital signals (bypass)	ADUM5210
Blocking capacitors	22 $\mu\text{F}$ (0805) / 25 V
Decoupling capacitors	25 $\mu\text{F}$ (0508) / 25 V per half-bridge
Output capacitors	22 $\mu\text{F}$ (1210) / 25V

to have poor performance owing to PCB manufacturing constraints such as trace width and trace-to-trace spacing. Therefore, a carefully selected Litz wire enables both higher packing factor and lower copper loss by both increasing packing factor and mitigating skin and proximity effects.

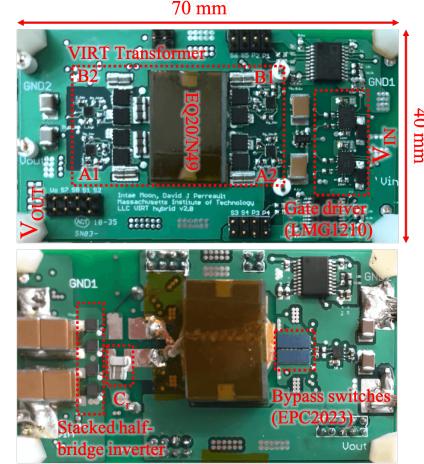
This approach can also be employed to directly provide high-voltage insulation (about 2.5 kV in this application [9]) between primary and secondary. Specifically, one can use a triple-insulated litz wire [10] to meet the voltage insulation requirement of the transformer, which in a fully planar transformer must be met by having a circuit board spacing between the primary and secondary windings; this spacing challenge becomes even worse if interleaving of the transformer is desired. Furthermore, one can retain the high control over the interconnect parasitics and losses on the high-current secondary side afforded by a planar construction as described in the next paragraph.

Shown in Fig. 6 is the proposed hybrid transformer configuration. A litz wire design of 180 strands of 48 AWG is chosen as the optimal design through LitzOpt software tool [11]; this tool allows a user to choose an optimal litz wire design and optimize copper loss in transformers with multiple windings for arbitrary current waveforms. For the secondary winding, 8 paralleled layers of a 1 oz copper PCB trace are used. In order to prevent the fringing field effects (e.g., from the gap) and undesirable changes in current distribution across the PCB layers, a gap-to-winding clearance exceeding 25% of the total window width (corresponding to  $h$  in Fig. 6a) is used [12]<sup>2</sup>. Furthermore, the voltage insulation requirement [9] is met by placing the primary and secondary windings as far as possible from each other. Such placement of the windings results in minimized interwinding capacitances and large leakage inductance ( $5.5 \mu\text{H}$  in this case). The leakage inductance eliminates the need for an additional physical inductor to form the LLC tank, helping to achieve an efficient, compact design.

<sup>2</sup> [12] treats the E-I core case, instead of the E-E core case, but it is estimated that the difference in the result would not be severe, especially as  $h$  is significantly larger than  $w$ .



(a) Circuit schematics for the VIRT with the bypass switch.



(b) Top and bottom sides of the PCB.

Fig. 7: Circuit schematic and prototype picture of the proposed design.

#### IV. PROTOTYPE SYSTEM CONSTRUCTION

Table IV shows the list of main components in the proposed VIRT-based dc-dc converter, and Fig. 7 shows the converter schematics and pictures of the prototype VIRT system with the bypass switch. The bypass switch is implemented with two “back-to-back” FETs (EPC2023 GaN FETs) such that it can carry bidirectional current and block bidirectional voltage. Owing to the hybrid construction and use of VIRT to realize fractional turns and reconfigurable conversion ratio (i.e. 12:0.5, 12:1, and 12:2 in this application), a relatively small size core (EQ20) is utilized as shown in Fig. 6. Furthermore, the hybrid transformer design not only removes need for an additional physical resonant inductor, but also allows for the bypass switches to be placed on the bottom side of the board in the direct vicinity of the transformer such that the current path can be minimized without violating the voltage insulation requirement between the primary and secondary windings. Consequently, the proposed system achieves a high “box” power density of  $23.2 \text{ W/in}^3$ .

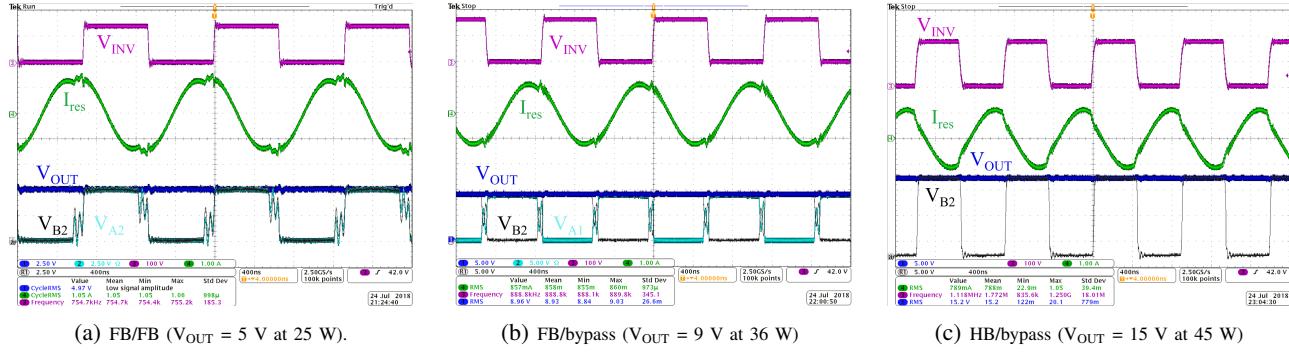
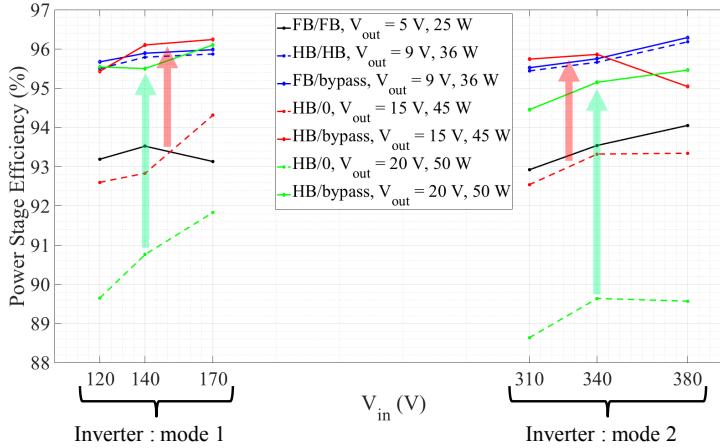
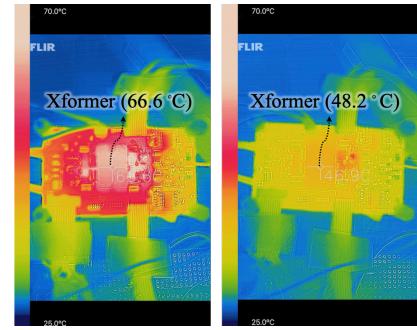


Fig. 8: Experimental waveforms validating FB/FB, FB/bypass and HB/bypass operations.



(a) Power Stage efficiency comparison between the bypass modes (solid lines) and conventional VIRT modes (dotted lines)



(b) Thermal pictures validating the improved performance in HB/bypass mode : HB/HB mode (left) and HB/bypass mode (right) at  $V_{IN} = 170$  V,  $V_{OUT} = 20$  V, and  $P_{OUT} = 50$  W

Fig. 9: Power stage efficiency comparison and thermal pictures around the VIRT transformer taken during HB/0 and HB/bypass modes : the performance improvements brought by the bypass switches are experimentally verified.

## V. EXPERIMENTAL RESULTS

Fig. 8 shows experimental waveforms in three key VIRT operating modes: FB/FB (Fig. 8a), FB/bypass (Fig. 8b), and HB/bypass (Fig. 8c) modes; these results validate the proposed VIRT system modeling and design. As shown in Fig. 9a, the bypass modes described in Fig. 1c and 1e result in much more efficient operation compared to the conventional VIRT modes of operation [2] described in Fig. 1d and 1f.

The efficiency improvement is substantial in HB/bypass mode compared to HB/0 mode due to full utilization of the core area which results in reduced transformer loss as shown in Fig. 9b. A part of the efficiency improvement is also attributable to reduced circulating currents in HB/bypass mode. This reduction is due to HB/bypass mode having a larger “net” magnetizing inductance compared to HB/0 mode as shown in Table I, due to the transformers being constructed with a gap across all three core legs. Note that the number of active switches and the number of always-on switches are the same for both zero and bypass modes. However, the bypass switches can be optimized for minimal  $R_{on}$  as their switching characteristics are irrelevant. Therefore, in HB/bypass mode, a small portion of the efficiency improvement comes from

the fact lower resistance always-on switches (i.e. bypass switches) are utilized. On the other hand, in FB/bypass mode, an efficiency improvement compared to HB/HB mode is associated with these always-on switches.

The power loss associated with a conventional HB/0 mode ranges from 3 W to 6.5 W across the 45 W and 50 W  $P_{out}$  operations and are disproportionately high compared to the power losses from the rest of the VIRT modes. With the bypass modes, the power losses in HB/0 mode are dramatically reduced below 3 W, compressing the range of power losses across all the modes of VIRT operation and keeping worst-case temperature rises of the converter similar for different operating conditions.

## VI. CONCLUSION

The proposed VIRT design with bypass switch enables additional flexibility in use of the magnetic core as compared to the previously-proposed VIRT design. The combination of VIRT-with-bypasses and stacked half-bridge inverter with VFX operating mode dramatically reduces voltage conversion stress on an LLC resonant tank and ensures its high performance across wide input and output voltage ranges. With the proposed bypass switch for VIRT rectifier, the DC-DC VIRT

system has shown much improved performance especially in high output voltage and power operations (e.g. 15 V at 45 W and 20 V at 50 W) compared to the conventional VIRT mode (HB/0), dramatically reducing the temperature raise of the converter at the rated power and enabling low loss across all operating conditions. Furthermore, the hybrid Litz-PCB transformer in the proposed design has enabled smaller overall footprint and reduced copper loss, which is promising for a high power density, high performance, DC-DC stage with wide input and output voltage ranges.

## APPENDIX

### A. LLC Resonant Tank Design

Note that an effective resistance  $R_{eff}$  in an LLC resonant converter can be calculated as

$$R_{eff} = \frac{8}{\pi^2} \left( \frac{n}{k} \right)^2 R_{load}, \quad (2)$$

where  $k$ , the voltage gain of the VIRT rectifier, is  $\frac{1}{2}$  for FB/FB mode, 1 for FB/bypass mode, and 2 for HB/bypass mode [13]. Likewise, quality factor  $Q_e$  is defined as

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_{eff}}, \quad (3)$$

From Equations 2 and 3, it is clear that HB/bypass mode used for 15 V output at 45 W has the smallest  $R_{eff}$  and, therefore, becomes the bottleneck for achieving ZVS on the stacked half-bridge inverter, specifically, when  $V_{in} = 380$  V such that the capacitive energy associated with the device output capacitances is maximized. Therefore, this operating condition is used to compute the number of the primary-side turns  $N_p$  with the single physical secondary-side turn, where  $N_p = M_{g,unity} M_{inv} \frac{kV_{in}}{V_{out}} \simeq 12.67$ , where  $M_{g,unity}$ , the unity gain of the LLC resonant tank, is 1,  $M_{inv}$ , the voltage gain of the stacked half-bridge inverter stage, is  $\frac{1}{4}$  for Mode 2,  $k$  is 2,  $V_{in} = 380$  V, and  $V_{out} = 15$  V. For a symmetric construction of the transformer, the primary-side turns  $N_p$  has been selected as an even number, 12. Note that in FB/FB mode the VIRT transformer effectively achieved 12:0.5 turns ratio whereas a conventional transformer achieves same step-down ratio with 24 turns on the primary-side winding.

The LLC resonant tank design parameters have been set as shown in Table III through the loss optimization process with a fixed resonant inductor which is entirely replaced by a leakage inductance of the transformer. Using the fundamental harmonic approximation (FHA), a resonant current  $I_{res}$  and magnetizing current  $I_{mag}$  can be computed at any give operating condition of the application. Using the computed circuit currents, one can compute the estimated power loss including conduction loss of the switches, transformer loss, and VIRT rectifier capacitor loss. More details on the loss computation are available in [14].

In order to choose optimal LLC parameters, one should consider two bottleneck operating conditions: (i) 15 V  $V_{out}$ , 380 V  $V_{in}$ , and 45 W  $P_{out}$  in HB/bypass mode for ZVS and (ii) 20 V  $V_{out}$ , 120 V  $V_{in}$ , and 65 W  $P_{out}$ , rated in HB/bypass mode for the maximum temperature rise, respectively. Shown

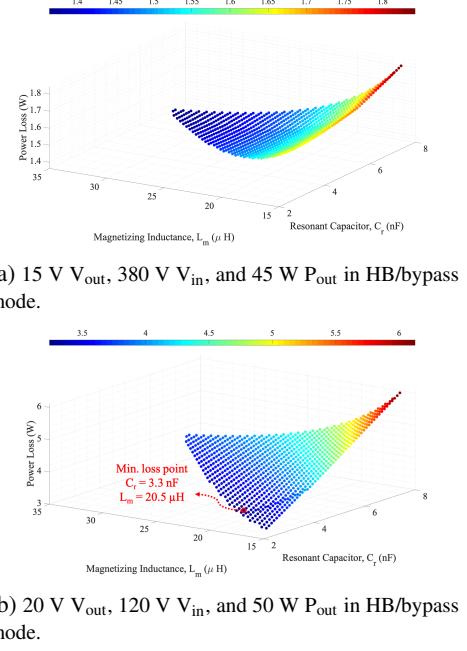


Fig. 10: Power Loss vs  $L_m$  vs  $C_r$  with  $L_r = 5.5$   $\mu$ H and  $N_p = 12$ . Note that (a) is the bottleneck operating condition for achieving ZVS and (b) for maximum temperature raise.

in Fig. 10a and 10b are estimated power losses for these two bottleneck operating conditions with  $L_r = 5.5$   $\mu$ H and  $N_p = 12$  plotted over wide range of magnetizing inductance  $L_m$  and resonant capacitance  $C_r$ . In order to generate the plots, MATLAB script is written such that combinations of  $L_m$  and  $C_r$  for each operating condition that satisfies ZVS conditions (discussed in Appendix B) are plotted. Therefore, one can first obtain all the valid combinations of  $L_m$  and  $C_r$  for (i) as in Fig. 10a. Then, estimating power loss for each of these obtained combinations for (ii), one can figure out the loss-optimized combination:  $L_m = 20.5$   $\mu$ H and  $C_r = 3.3$  nF.

### B. LLC Zero Voltage Switching

Shown in Fig. 11 are the voltage gain and ZVS curves for  $V_{out} = 15$  V and  $P_{out} = 45$  W. In the plot,  $V_{out}$  vs  $f_{sw}$  for the chosen  $V_{in}$  from a low-range voltage (120 - 170 V) and high-range voltage (310 - 380 V) is plotted along with a desired output voltage since  $V_{out} = V_{in} M_{g,LLC}(f_{sw}, Q_e, L_n) M_{inv} \frac{k}{L_r}$ , where  $L_n = \frac{L_m}{L_r}$ . Note that a fundamental harmonic approximation (FHA) for the square waveform onto the LLC resonant tank has been made. Nonetheless, these voltage gain curves show reasonable accuracy for operations in the vicinity of the resonant frequency  $f_{res}$ .

In order to ensure ZVS on the primary-side inverter in an LLC converter, one needs to ensure that the input impedance  $Z_{in}$  looking into the resonant tank is inductive such that the resonant current  $I_{res}$  lags behind the applied voltage  $V_{INV}$  in this case [13].

$$Z_{in} = |Z_{in}| e^{j\Phi_z}, \quad (4)$$

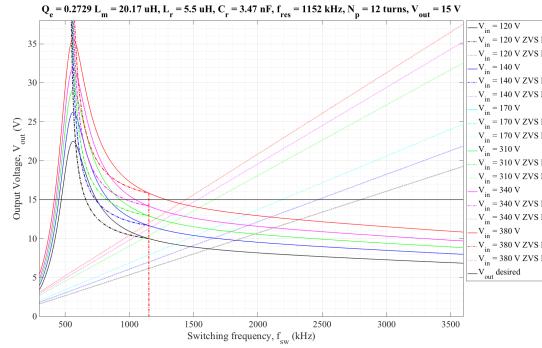


Fig. 11: Voltage gain and ZVS curves for HB/bypass mode ( $V_{out} = 15$  V and  $P_{out} = 45$  W).

where  $-\pi/2 \leq \Phi_z \leq \pi/2$  and  $Z_{in}$  is inductive for  $\Phi_z > 0$ , capacitive for  $\Phi_z < 0$ , and resistive for  $\Phi_z = 0$ . Note that  $\Phi_z$  is a function of the switching frequency  $f_{sw}$ . In Fig. 11, ZVS I curve serves as a border between the capacitive and inductive regions such that the region above the ZVS I curve is the inductive region of  $Z_{in}$  and the region below it is the capacitive region. Finally, for operation above the series resonance point it is guaranteed that  $Z_{in}$  is always inductive. The proposed DC-DC VIRT system is designed to operate in an inductive region for all operating conditions of the proposed design.

In addition to making sure  $Z_{in}$  is always in an inductive region for ZVS, one needs to ensure there is a sufficient inductive energy associated with the current through the magnetizing inductance  $I_m$  during the deadtime. Note that switches in the stacked half-bridge inverter are labeled  $S_1$  -  $S_4$  as shown in Fig. 7a. In Inverter mode 1,  $I_m$  should charge up the  $C_{ds}$  of  $S_1$  and  $S_4$  and discharge the  $C_{ds}$  of  $S_2$  and  $S_3$  before the body diode conduction of  $S_2$  and  $S_3$ . In Inverter Mode 2,  $I_m$  needs to charge up the  $C_{ds}$  of  $S_1$  and discharge the  $C_{ds}$  of  $S_2$  before the body diode conduction of  $S_2$  in one cycle. In the other cycle of Inverter Mode 2,  $I_m$  needs to charge up the  $C_{ds}$  of  $S_4$  and discharge the  $C_{ds}$  of  $S_3$  before the body diode conduction of  $S_3$ . Therefore, Equation (5) must be met in order to achieve ZVS on the primary-side inverter.

$$\frac{1}{2}(L_m + L_r)I_{m,peak}^2 \geq \frac{1}{2}n_{cap}C_{eq}(k_{inv}V_{in})^2, \quad (5)$$

where  $I_{m,peak} = \frac{2nV_{out}}{k\pi^2 f_{sw} L_m}$  (FHA),  $C_{eq} = C_{ds} + C_{par}$ ,  $n_{cap} = 4$  in Inverter mode 1 and 2 in Inverter mode 2 and  $k_{inv} = \frac{1}{2}$ . In order to plot a ZVS II boundary as shown in Fig. 11 Equation (5) can be further transformed as follow;

$$V_{out} \geq \sqrt{\frac{n_{cap}C_{eq}(k_{inv}V_{in})^2}{L_m + L_r} \frac{k\pi^2 f_{sw} L_m}{2n}}, \quad (6)$$

where  $k$  is the gain of the VIRT rectifier defined in Equation (1). This ZVS II boundary, which is based on the energy requirement for sufficient charge and discharge, sets

the minimum output voltage the DC-DC VIRT system can achieve at certain switching frequency  $f_{sw}$  with the given LLC parameters in order to achieve ZVS on the primary-side inverter. Note that this energy requirement is met in all VIRT operations of the proposed design since as shown in Fig. 11 which corresponds to the bottleneck operating condition for achieving ZVS.

Note that both  $C_r$  and  $C_{in}$  can be ignored in an energy conversion analysis since they are much larger than the device capacitances  $C_{ds}$ .  $C_{eq}$  includes parasitic capacitances  $C_{par}$  in addition to  $C_{ds}$ .  $n_{cap}$  is 4 for Inverter mode 1 and 2 for Inverter mode 2 due to the fact that 2 device capacitors are charged up and 2 other device capacitors are discharged in one cycle of Inverter mode 1 whereas only one device capacitor is charged and one other capacitor is discharged in one cycle of Inverter mode 2 as illustrated in Fig. 5.

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