

©1999 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Evaluation of Critical Current Density of Nb/Al/AIO_x/Nb Josephson Junctions Using Test Structures at 300 K

Karl K. Berggren, Michael O'Hara, Jay P. Sage
M.I.T. Lincoln Laboratory, 244 Wood St., Lexington, MA 02173-9108

A. Hodge Worsham
Northrop Grumman STC, 1350 Beulah Rd, Pittsburgh PA 15235-5080

Abstract—We have designed and fabricated test structures that allow the determination of the critical current density and processing run-out of low T_c Josephson junctions based only on room-temperature measurements. We demonstrated that the 300 K tunneling conductance of a junction barrier is proportional to the critical current at 4.2 K. This testing technique greatly reduced the time required to characterize a process wafer. In one demonstration we tested hundreds of devices across a 150-mm-diameter wafer in less than an hour. In another we used a selective niobium anodization process with only two mask levels to determine the critical current density of a Nb/AIO_x/Nb trilayer within a day of its deposition. We have also used automated probing stations to decrease testing delays further and thus to improve process cycle time.

I. INTRODUCTION

Nb/Al/AIO_x/Nb trilayer superconducting tunnel junctions have become the *de facto* standard for low- T_c superconducting electronics. The greatest challenge in fabricating trilayer junctions lies in controlling the targeting and uniformity of the tunneling barrier. This difficulty is greatly amplified by a problem inherent to fabrication of any cryogenic electronic circuit: how does one achieve control of a low-temperature device parameter based on process-monitoring measurements made at room temperature? In this paper we address this question as it pertains to Josephson-junction-based electronics.

We have fabricated two types of test structures designed to determine the electrical properties of Josephson junctions using measurements made at room temperature. We have also developed a processing technique that rapidly produces simple structures for testing, allowing a trilayer to be characterized in a few days, before effort is expended on a lengthy fabrication process.

Most past studies of normal tunneling behavior at any temperature range have focused on Al/AIO_x/Al [1][2] or Pb/AIO_x/Al [3] structures. Studies on Nb/Al/AIO_x/Nb trilayers have been used in the past to study the chemistry of the barrier [4]. Our study examined the 4.2K and 300K behavior of Nb/AIO_x/Al/Nb tunnel junctions and provides an empirical

relation for establishing 4.2 K behavior based on 300 K tests. The process-dependence of this law was established by comparison of data from two processes with different J_c and V_g and different trilayer fabrication methods. This test methodology could be used to complement and improve on low-temperature surveys of J_c targeting and uniformity [5].

The central distinguishing characteristics of our study were: 1) the use of test structures that allowed accurate determination of R_n despite lead resistance, even at room temperature, and 2) the use of an extremely rapid process, termed a "short-loop", that allowed the determination of J_c in a matter of only a day or two of processing time. We will first describe the two test structures used, then we will present our result and an outline of the short-loop process; finally we will conclude with discussion and analysis of the results.

II. DESCRIPTION OF EXPERIMENTS

Studies that have examined the electrical characteristics of a tunneling barrier have traditionally used superconducting leads to eliminate spurious resistance from the measurements. The junction resistance was then measured and results were compared to the theoretical predictions. In the regime where the junction bias is much less than the height of the tunneling barrier, tunneling junctions are known to behave like ohmic resistors: the junction resistance can be written as $R_b = \rho_b/A$ where ρ_b has units of $\Omega \mu\text{m}^2$ and is called the specific barrier resistivity.[†] The problem of determining ρ_b from measurement made with resistive leads requires careful test-structure design.

A. Determining ρ_b

Fig. 1a shows the cross-bridge Kelvin resistor (CBKR) test structure which has been used to measure contact resistance in semiconductor-metal contacts [6] and to study tunneling resistance as a function of temperature [2]. In this test structure the current flowed in a straight path from the bottom to the top lead, while the voltage was measured perpendicular to the direction of current flow; to first order the potential drop in the leads was not measured. These test structures were fabricated using the Lincoln Laboratory doubly-planarized all-refractory technology for superconductive electron-

Manuscript received September 14, 1998.

Opinions, interpretations, conclusions, and recommendations are those of the authors and not necessarily endorsed by the United States Air Force.

This work was sponsored by the United States Air Force Research Laboratory Sensors Directorate under Air Force contract F19628-94-C-0097 and by the Department of Defense under Air Force contract F19628-95-C-0002.

[†] This is sometimes referred to as the specific contact resistivity, a term we avoid as the term "contact" is ambiguous in this case.

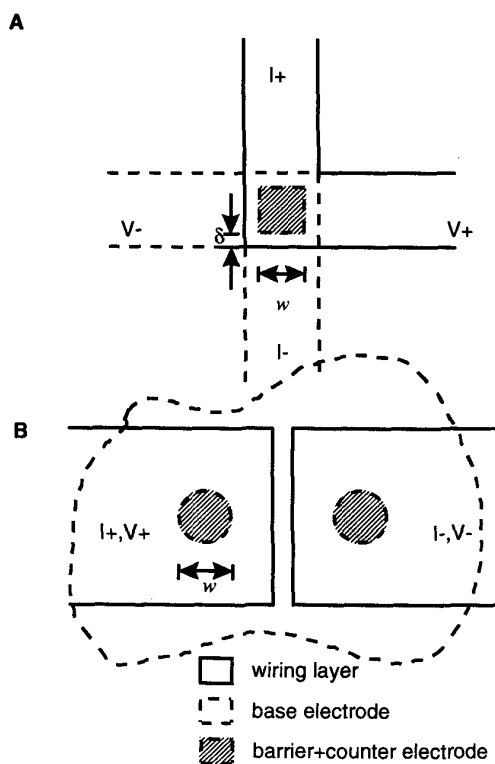


Fig.1 Schematic diagrams showing layout of test structures used in this experiment. A) CBKR test structures allowed determination of the resistance of the barrier and thus J_c by measuring the voltage using probes perpendicular to the direction of current flow. B) Two-lead test structures, using two junctions in series, allowed determination of J_c based on room-temperature measurements after only three photolithography steps. The lead resistance was subtracted from the measurement by comparing the resistance of test structures differing only in the barrier area. The base electrode in this test structure is unpatterned, and is represented in the figure as an amorphous outline.

ics (DPARTS) process [7]. Fig. 1b shows a test structure consisting of two Josephson junctions in series. These test structures were fabricated using 10- μm -diameter and 5- μm -diameter circular junctions. The difference of the two resistance values was taken in order to eliminate the lead resistance. We refer to this test structure as a two-junction series array (TJSA). These junctions were fabricated using the Northrop-Grumman anodization- [8] and etching-based processes [9].

In the case of the CBKR test structures the barrier resistance, R_b , can be expressed as $R_b(w) = \rho_b / (\pi(w - w_o)^2)$, where w is the nominal linear edge dimension of the junction and w_o is the sizing error of the junction. By measuring $R_b(10 \mu\text{m})$ and $R_b(5 \mu\text{m})$ and solving the two equations thus formed for ρ_b , we get

$$\rho_b = \left[\frac{(5\mu\text{m})\sqrt{R_b(5)R_b(10)}(\sqrt{R_b(5)} + \sqrt{R_b(10)})}{R_b(5) - R_b(10)} \right]^2 \quad (1)$$

The TJSA test structures measured the barrier resistance indirectly. The measured resistance of each test structure was $R_b(w) = 4\rho_b / \pi(w - w_o)^2 + R_l$ where R_l is the lead resistance and in this case w refers to the junction diameter. R_b was measured for 5- μm -diameter and 10- μm -diameter junctions: neglecting the sizing error, which was $\sim 0.2 \mu\text{m}$ for these junctions, we can solve for ρ_b :

$$\rho_b = \frac{\frac{\pi}{4}(R_b(5) - R_b(10))}{\left(\left(\frac{1}{5\mu\text{m}} \right)^2 - \left(\frac{1}{10\mu\text{m}} \right)^2 \right)} \quad (2)$$

B. Determining J_c

J_c was determined using a slightly different method for the two types of test structures. In the first experiment, using the CBKR test structures, the junctions were measured in a poorly shielded Dewar, using a four-point method: the presence of trapped flux in the junctions partially suppressed the critical current, which then could not be measured directly. Instead, the junction I-V characteristics were analyzed digitally to give the gap voltage, V_g , and the normal resistance, R_n , of the junction. I_c was then determined by using the empirical relation

$$I_c = \frac{0.68V_g}{R_n} \quad (3)$$

The accuracy of this relation had been previously verified using measurements in which care had been taken to avoid trapped flux. This I_c is 9% lower than that predicted by the Ambegaokar-Baratoff relation for 4.2K niobium junctions [10]. J_c was then determined by assuming a fixed spatial sizing error of the Josephson junctions, so that $I_c(w) = J_c (w - w_o)^2$. Then by measuring I_c for 10- and 5- μm junctions, J_c was calculated as follows:

$$J_c = \left[\frac{\sqrt{I_c(10)} - \sqrt{I_c(5)}}{5\mu\text{m}} \right]^2 \quad (4)$$

In the TJSA experiment the zero-field I_c was determined by measuring the maximum I_c obtained while varying the flux coupled into a SQUID until at least a full period of I_c modulation had been observed. Assuming the two junctions in the SQUID were well balanced, the I_c of the junctions was just $1/2$ the I_c of the SQUID.

III. RESULTS

Fig. 2 shows the observed correlation between the specific barrier resistivity measured at room temperature and the J_c determined from I-V measurements at 4.2 K. The relationship in the two cases was not identical; the difference between the two methods suggests a difference in either the tunneling barriers, the test structures, or the method used to measure I_c . Of course there were small differences in each of these factors

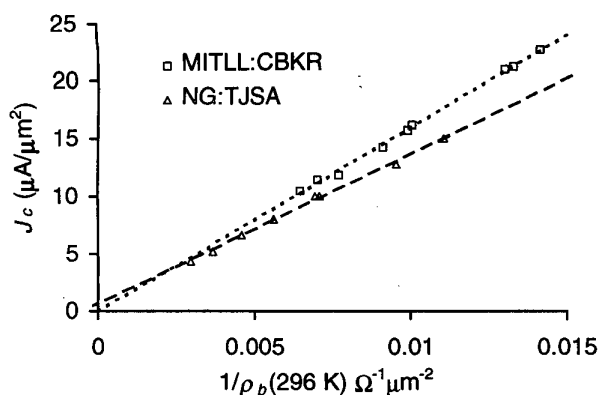


Fig. 2. Correlation between J_c measured at 4.2 K, and the specific barrier resistivity determined at 300 K, using two different fabrication processes and different test structures, one at MIT Lincoln Laboratory (MITLL) using CBKR test structures, the other at Northrop-Grumman (NG) using TJSA test structures. The MITLL data shown was corrected for parasitic lead resistance using a theoretical model of the test structures. Uncorrected data exhibited greater scatter and deviation from the NG data.

so it is impossible at this point to sort out exactly which contributed the most to the difference observed in Fig. 2.

IV. DESCRIPTION OF SHORT-LOOP PROCESS

The short-loop process was particularly helpful when used in conjunction with the TJSA room-temperature J_c test method. This process required only two levels of lithography and about one day of processing time.

Fig. 3 shows the sideview of the process. First, a trilayer was deposited on a clean oxidized Si wafer. The deposition differed from the standard trilayer only in the thickness of the counter electrode: since anodization was used to define the junction areas, we reduced the mechanical stress caused by the Nb_2O_5 by keeping the counter-electrode thickness to under 500 Å. Junction areas were defined by a selective niobium anodization process [11] as shown in Fig. 3a and b. The second mask level defined the wiring level of niobium using image reversal lithography and liftoff (Fig. 3c). A niobium etching process could also be used for this step.

Due to junction edge effects, test structures fabricated using the short-loop process was not appropriate for determining J_c of junctions with high sub-gap leakage: the enhanced perimeter-dependent current of the leakage effects could not be sorted out from the decreased perimeter-dependent current caused by over-anodization.

V. ANALYSIS AND DISCUSSION

Putting analysis of contributing errors aside for the moment, we first ask the question: why should the specific barrier resistivity prove to be such a good predictor of low-temperature tunneling critical current? Past studies have

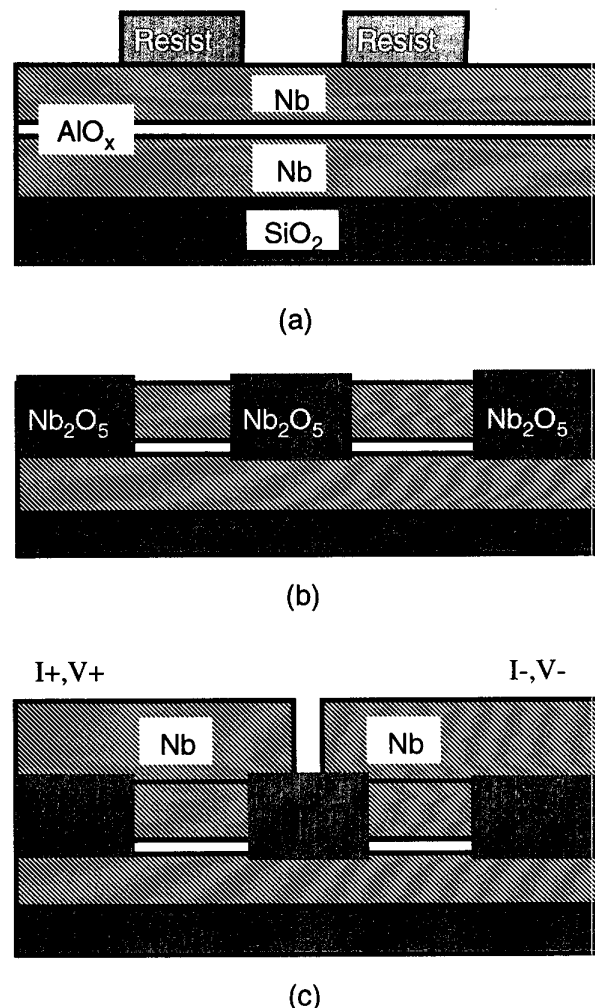


Fig. 3. Schematic diagram showing steps in the short-loop process presented in the text.

found that the barrier height, ϕ , is typically $\sim 1 \text{ eV} \gg k_b T$ at 300K [4]. Because most excitations occur within $k_b T$ of the Fermi energy, thermal excitations over the barrier do not contribute to the tunneling conductance. The remaining temperature effect, due to temperature-induced variation in the occupation of states well below the barrier, is expected to be small and so it is likely that the room temperature conductance will be only slightly modified by cooling to 4.2 K. This reasoning explains our finding that there was a strong correlation between the room temperature tunneling conductance and the 4.2 K normal conductance of the barrier.

Now we turn back to the question of why the test methods we used were able to determine small tunneling resistances in the presence of substantial lead resistance. For the CBKR test structures, the requirement that the resistive voltage drop in the lead margin (see Fig. 1) around the junction be much less than the voltage drop in the barrier itself leads to the condition $\rho_b/R_s \gg \delta w$, where R_s is the sheet resistance in the lead. This condition can be understood by noticing that

when δ is small there is less potential drop in the current lead, and so there is less error in the measurement. Also, when the junction size, w , is decreased, the barrier resistance goes up as $1/w^2$ while the lead resistance goes up only as $1/w$, so smaller junction dimensions should tend to emphasize the junction resistance and reduce the effect of the lead resistance.

The accuracy of the CBKR test structures can be calculated in a manner similar to the numerical calculation given by Loh et al. [12], who treat the case where one of the metal layers (either base-electrode or wiring layer) is assumed to have zero resistance. We implemented a 2-dimensional model of the CBKR test structures based on a finite element analysis of Poisson's equation. The error in the test structures was thus compensated for and removed from the measurement.

The TJSA test structures included two potential sources of systematic error: 1) if the junction area is uncertain, perhaps due to a sizing bias, the calculation of ρ_b is called into question, and 2) there is a small area of lead around the 5- μm -diameter junction where the current must pass to get to the junction that is not present in the 10- μm -diameter junction (because the leads have the same dimensions in the two cases, but the 5- μm -diameter junction is smaller). This additional lead resistance cannot be compensated for by subtracting the two junction areas, but this contribution is only a fraction of a square. Neither of these two effects should greatly impact the reproducibility of the J_c vs. ρ_b correlation shown in Fig. 2, but might explain some of the remaining difference between the two processes.

There were two additional sources of systematic measurement error that deserve mention: 1) Because the counterelectrode was on top of the barrier, it was impossible to avoid adding the resistance of the counterelectrode to that of the barrier in the measurement. For the DPARTS process, however, the measured resistance will exceed the actual barrier resistance by only $\sim 0.25\%$ due to this effect. 2) From other experiments we know that in the DPARTS process, the barrier is non-uniform, specifically that a low- J_c region exists around the outer $\sim 0.5 \mu\text{m}$ of the junction. This will effectively increase the lead margin, δ , and lower the accuracy of the measurements. This effect was not included in the calculations of lead resistance error that went into the data shown in Fig. 2.

VI. CONCLUSIONS

The central result of this work is that J_c can be accurately determined based on measurements made only at room temperature. This was achieved by first determining the specific barrier resistivity at room temperature by two methods, and then correlating the measured resistivity to J_c determined at 4.2K. This result greatly facilitates improved control over junction critical currents: it allows the processing engineer to test junctions before processing is completed and eliminate wafers that are out of the target J_c range. Furthermore, by periodic testing of devices during processing, one can detect

device parameter shifts during fabrication due to damage of the wafers by a tool or process. We have also presented a short-loop process that can be used in conjunction with the test structures described to determine the J_c of a trilayer in a matter of a day or two of processing time. By demonstrating room-temperature monitoring of the 4.2 K behavior of Josephson junctions, these results reduce the difficulty inherent in processing devices for cryogenic Josephson junction electronics.

ACKNOWLEDGMENT

We would like to thank G. Selfridge, J. Wood, D. Baker, J. Reinold, and D. Young for assistance in processing. We would also like to thank T. Weir, G. Fitch, and S. Cann for help with testing and analysis. Finally we would like to acknowledge the frequent helpful suggestions and discussions with other members of the Analog Device Technology Group, especially A. Anderson, D. Oates, T. C. L. G. Sollner, and L. Johnson.

- [1] J. C. Fisher and I. Giaever, "Tunneling through thin insulating layers," *J. Appl. Phys.*, vol. 32, pp. 172-177, 1961.
- [2] Thomas E. Hartman and Jay S. Chivian, "Electron tunneling through thin aluminum oxide films," *Phys. Rev.*, vol. 134, pp. A1094-A1101, 1964.
- [3] W. F. Brinkman, R. C. Dynes, and J. M. Rowell, "Tunneling conductance of asymmetrical barriers," *J. Appl. Phys.*, vol. 41, pp. 1915-1921, 1970.
- [4] D. J. Adelerhof, E. P. Houwman, D. Veldhuis, J. Flokstra, and H. Rogalla, "Conductance studies on different types of Nb/Al_xO_y(/Al)/Nb Josephson tunnel junctions," *Physica B*, vol. 165&166, pp. 1581-1582, 1990.
- [5] Xiaofan Meng, Huaming Jiang, Anupama Bhat, and Theodore Van Duzer, "Precise control of critical current and resistance in a Nb/AlO_x/Nb Integrated Circuit Process," ISEC '97 extended abstracts, vol. 2, pp. 164-166, 1997.
- [6] Stephen J. Proctor, Loren W. Linholm, and Jeffrey A. Mazer, "Direct measurements of interfacial contact resistance, end contact resistance, and interfacial contact layer uniformity," *IEEE Trans. on Elect. Dev.*, vol. 30, pp. 1535-1542, 1983.
- [7] Karl K. Berggren, Earle M. Macedo, David A. Feld, and Jay P. Sage, "Low T_c superconductive circuits fabricated on 150-mm-diameter wafers using a doubly planarized Nb/AlO_x/Nb process," *unpublished*, 1998.
- [8] Joonhee Kang, Donald L. Miller, John X. Przybysz, and Michael A. Janocko, "Fabrication of 12-bit A/D converter using Nb/AlO_x/Nb Josephson junctions", *IEEE Trans. on Magnetics*, vol. 27, pp. 3117-3120, 1991.
- [9] D.L. Miller, J.X. Przybysz, A.H. Worsham, and E.J. Dean "Flux quantum sigma-delta analog-to-digital converters for rf signals," *unpublished*, 1998.
- [10] See for example M. Tinkham, "Introduction to Superconductivity", (McGraw-Hill, Inc., New York, NY), 2d ed. pp. 200-201 (1996)
- [11] H. Kroger, L.N. Smith, and D.W. Jillie, "Selective niobium anodization process for fabricating Josephson tunnel junctions," *Appl. Phys. Lett.*, vol. 39, pp 280-282, 1981.
- [12] William M. Loh, Stanley E. Swirhun, Tim A. Schreyer, Richard M. Swanson, and Krishna C. Saraswat, "Modeling and measurement of contact resistances," *IEEE Trans. on Electronic Devices*, vol. 34, pp. 512-524, 1987.