Improved Critical-Current-Density Uniformity by Using Anodization

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Abstract—We discuss an anodization technique for a Nb superconductive-electronics-fabrication process that results in an improvement in critical-current-density J_c uniformity across a 150-mm-diameter wafer. We outline the anodization process and describe the metrology techniques used to determine the NbO_x thickness grown. In the work described, we performed critical current I_c measurements on Josephson junctions distributed across a wafer. We then compared the J_c uniformity of pairs of wafers, fabricated together, differing only in the presence or absence of the anodization step. The cross-wafer standard deviation of J_c was typically $\sim 5\%$ for anodized wafers but $> 15\%$ for unanodized wafers. This difference in J_c uniformity is suggestive of an in-process modification from an unknown cause that is blocked by the anodic oxide. It is interesting that small junctions do not see an improvement in I_c uniformity-apparently the anodization improves only the J_c uniformity and not the variation in junction size. Control of J_c is important for all applications of superconductive electronics including quantum computation and rapid single-flux quantum (RSFQ) circuitry.

Index Terms—Anodization, critical-current-density, Josephson junctions.

I. INTRODUCTION

CONTROLLING the critical-current-density J_c uniformity across a wafer is a major challenge in the Nb Josephson junction fabrication process. Typically, the J_c variation across a 150-mm-diameter wafer is $> 15\%$ for current densities ranging from 0.1–20 kA/cm^2. Highly uniform J_c is desired for producing low cross-chip J_c variation as well as producing a higher quantity of chips per wafer at a given critical-current-density. Past results suggested that anodization of the junction region improves J_c uniformity across a wafer but this suggestion has never been supported with direct comparisons [1]–[3]. In this paper, we address our efforts to incorporate anodization into our standard Nb process and we study its effects on J_c uniformity by directly comparing anodized wafers with unanodized wafers.

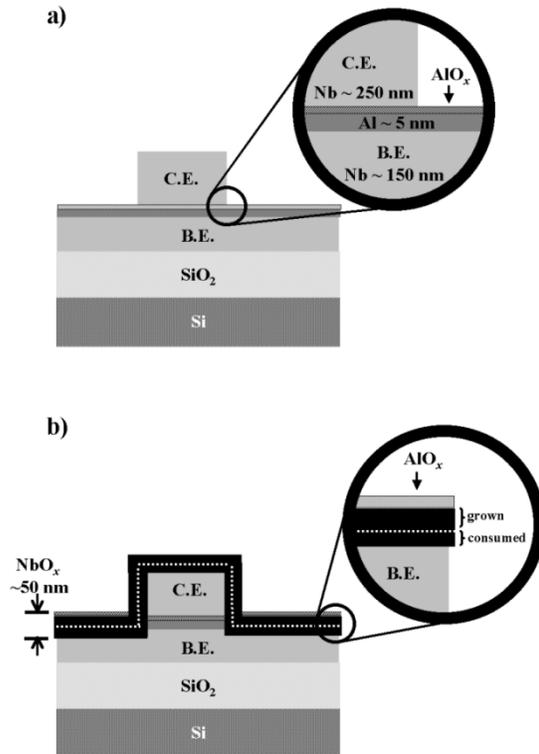The Josephson junctions were fabricated in a class-10 cleanroom facility at MIT Lincoln Laboratory. We used our standard

Fig. 1. a) Nb Josephson junction after counter-electrode (C.E.) etch but immediately prior to anodization. Inset shows the AlO_x tunneling barrier region. b) Junction region after anodization. The surface of the counter- and base-electrode (B.E.) is converted to a metal-oxide layer approximately 50 nm thick. The dotted line shows the original surface. Inset shows amount of anodic oxide grown and consumed. The anodic oxide causes the surface to swell up and out slightly during growth.

doubly planarized all-refractory technology for superconductive electronics process [DPARTS] [4]. The substrates were 150-mm-diameter prime silicon wafers, thermally oxidized to produce a 500-nm-thick SiO_2 layer. The $Nb/Al/AlO_x/Nb$ trilayer was then deposited, followed by patterning of the Nb counter-electrode (C.E.) using optical projection lithography. Reactive ion etching (RIE) of the counter-electrode was performed in a load-locked chamber using SF_6 gas. Because we felt that after RIE the junction region could be vulnerable to chemical, plasma and/or other damage from subsequent processing steps (shown in Fig. 1(a), we anodized the wafer to form a 50-nm-thick protective metal-oxide layer around the junction perimeter. Fig. 1(b) shows that after anodization the junction region is "sealed" from the outside environment by

a thick NbO_x layer. The remaining steps of the process were modified slightly to account for the presence of this layer, as described in Section II.

We first outline the anodization procedure and its incorporation into the standard Nb superconducting device fabrication process. We then discuss metrology methods used to determine the thickness of niobium oxide grown. We follow with a discussion of the effects of anodization on critical-current-density uniformity, presenting room-temperature normal-state resistance measurements of junctions. Finally we conclude with discussion and analysis of our results.

II. ANODIZATION PROCESS DESCRIPTION

The modification of the fabrication process to include anodization consisted of three steps: 1) the development of the anodization process; 2) the integration of the anodization step into the existing DPARTS process; and 3) the development of metrology methods for process control. In this section we describe work in each of these areas.

A. Anodization Process

Anodization is an electrolytic process in which a metal, in our case niobium, serves as the anode in a suitable electrolyte. When a current passes through the Nb film in the electrolytic solution, the surface of the Nb is converted to its oxide form. This oxidation progresses from the solution inward, toward the metal, with the final thickness determined by the applied voltage. The metal-oxide layer serves as a protective barrier to further ionic flow [5]. Anodization processes of this sort have been used extensively in the past for the fabrication of Nb Josephson junctions [1], [6]–[10].

For our process, anodization followed the RIE of the counter-electrode and stripping of photoresist, so the anodization was unmasked. Anodization was performed in an electrolytic solution of tartaric acid ($HOOC(CHOH)_2COOH$) and ammonium hydroxide (NH_4OH). 400 g of tartaric acid powder were added to a recirculating bath of an approximately 5L volume of deionized water. Then a 28–30% NH_4OH solution was added incrementally until the measured pH was 5.1 ± 0.1 (the total volume of NH_4OH solution added was > 300 ml). The anodization process proceeded as follows: (1) A Pt wafer (cathode) in the electrolytic solution was grounded while the Nb device wafer (anode) was connected to a power supply. (2) The voltage output of the power supply was ramped, from 0 V to 20 V, maintaining an initial constant current of 0.225 A through the wafer. The overall ramp time was approximately 50 sec. (3) The voltage was then held constant at 20 V. During the voltage hold time, the current through the wafers dropped exponentially as the NbO_x layer densified. (4) When the current level reached 10% of its initial value, the power supply was abruptly switched off. The total immersion time was approximately 1.5 minutes. After anodization, the wafers were cleaned using deionized water in a dump-rinser and spin-rinser dryer.

B. Process Integration

Subsequent process steps were modified to account for the NbO_x layer. The NbO_x layer made it difficult to etch through

TABLE I
OPTICAL CONSTANTS OF NB AND NbO_x. INDEX OF REFRACTION n AND ABSORPTION COEFFICIENT k VALUES VS. WAVELENGTH FOR NB FILM AND 95 NM THICK NbO_x FILM

	Nb		NbO_x	
λ(nm)	n	k	n	k
400	2.644	3.144	2.565	2.785×10^{-3}
425	2.707	3.262	2.565	1.666×10^{-3}
450	2.788	3.362	2.479	0
475	2.871	3.439	2.454	0
500	2.943	3.500	2.433	0
525	3.000	3.550	2.416	0
550	3.038	3.596	2.401	0
575	3.059	3.643	2.388	0
600	3.065	3.697	2.376	0
625	3.058	3.760	2.365	0
650	3.041	3.834	2.354	0
675	3.018	3.920	2.345	0
700	2.992	4.018	2.336	0
725	-	-	2.327	0
750	-	-	2.32	0
775	-	-	2.313	0
800	-	-	2.306	0

the base-electrode and to gain contact through a via to the base- and counter-electrode. We modified the RIE etching process for the base-electrode slightly from that of the other Nb layers by performing it at a substrate temperature of 80°C (compared to 50°C for the other Nb layers). This elevated temperature was needed to etch through the 50 nm NbO_x layer. We also observed an etch undercut profile due to the anodic oxide (see Fig. 3(a)).

To achieve contact through the anodic layer at the base of the via (between the base-electrode/wiring layer and counter-electrode/wiring layer) we relied on the 25% over-etch of the PECVD deposited oxide and the pre-sputter of the wiring layer to promote adhesion between the base-electrode and wiring layer. To achieve contact to the counter-electrode, we used the polishing from chemical mechanical planarization (CMP) and the pre-sputter prior to wiring deposition to remove the NbO_x grown on the top of the counter-electrode.

C. Thickness Metrology

Determining NbO_x layer thickness is critical for both process control of anodization and for all subsequent dielectric metrology. In our process, film thicknesses are typically measured by using spectral reflectometry, for which the optical constants and thickness of all underlying films are required. Data available in the literature for bulk and thin-film Nb and NbO_x was found to be inadequate: it could not determine the anodic film thickness accurately from spectral reflectometry or ellipsometry. We therefore needed to determine the index of refraction n and absorption coefficient k of the underlying Nb and NbO_x as a function of wavelength.

To determine the optical constants of NbO_x we first needed an independent measure of the film thickness. We used scan-
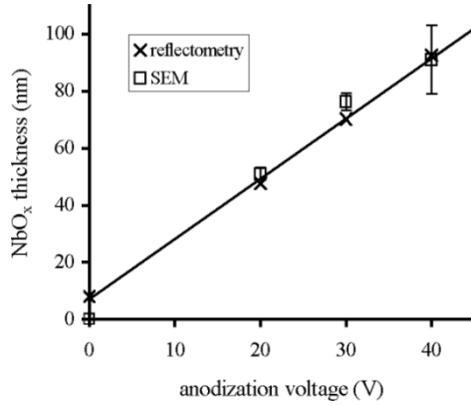
Fig. 2. NbO$_x$ film thickness for given anodization voltage. Film thickness is determined both by reflectometry measurements and SEM images. The solid line represents the best-fit line to the reflectometry data.

ning electron microscopy (SEM) images to determine the film thickness. We then determined the optical properties of the Nb and NbO$_x$ film using a Hitachi U-4000 spectrophotometer with a 12-degree absolute-reflectance attachment. The resulting reflectance data was used to extract the index of refraction n and absorption coefficients k as a function of wavelength for a Nb layer and 95-nm-thick NbO$_x$ layer. The results are given in Table I. NbO$_x$ data varied by a few percent depending on the thickness of the oxide; the range of Cauchy coefficients was from $A_n = 2.169$ to $A_n = 2.236$ and from $B_n = 0.047$ to $B_n = 0.05$ while A_k and B_k were zero (the range is too small to be important for our purposes therefore we simply used Cauchy coefficients of $A_n = 2.169$ and $B_n = 0.047$). For Nb the Cauchy coefficients were $A_n = 3.20$, $B_n = -0.086$ and $A_k = 4.625$ and $B_k = -0.25$. We then compared the film thicknesses extracted from fitting spectral reflectometry data to measurements from SEM images for a variety of anodization voltages and found agreement, as shown in Fig. 2. Finally, optical reflectometry and SEM data were compared to ellipsometric analysis at 632 nm and agreement was also obtained.

As mentioned previously, we used SEM images to estimate NbO$_x$ thickness and transmission electron microscopy (TEM) images to inspect the anodic film. A SEM image of NbO$_x$ grown on a Nb layer is shown in Fig. 3(a). We estimate the thickness of the NbO$_x$ layer to be ~ 50 nm for an anodization voltage of 20 V. Sample preparation and TEM imaging of Josephson junctions was performed by MCNC and TEM Analysis Inc. Prior to imaging, the junctions were tested at liquid helium temperatures (4.2 K) and found to have good quality ($V_m > 50$ mV). TEM images of the anodized junction region is shown Fig. 3(b).

Comparing anodized/unanodized wafer pairs for wafers with 50 nm of NbO$_x$, we determined from step-height measurements that the thickness of anodized wafers was typically 30 nm greater than unanodized wafers. From this we conclude that approximately 20 nm of Nb was consumed in the growth process.

III. EFFECT OF ANODIZATION ON CRITICAL-CURRENT-DENSITY UNIFORMITY

In order to determine the effect of anodization on the electrical characteristics of our junctions, we looked at their normal-state
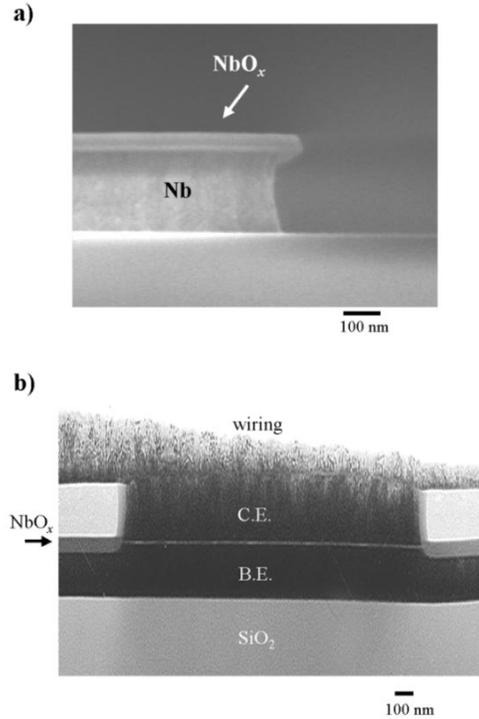

Fig. 3. a) SEM image of NbO$_x$ grown on Nb layer. b) TEM image of an anodized junction showing clearly the sealing of the junction edge by NbO$_x$. Note the clean interface between the counter-electrode and wiring layer where the NbO$_x$ has been removed by CMP.

resistance R_n at room temperature. We calculated the critical current I_c of a junction from the R_n measurements for a large quantity of junctions distributed across an entire wafer using an automatic probing station. From these measurements we determined critical-current-density uniformity for several anodized/unanodized wafer pairs where, for each pair, the trilayers were fabricated together.

A. Room Temperature Measurements

Room temperature measurements using specially designed test structures were used to determine the overall critical-current-density across the wafer. We employed four-point cross-bridge Kelvin resistor (CBKR) structures to determine the normal-state resistance R_n of the Josephson junction. Previous studies have shown that the critical current of a junction can be accurately determined from the room-temperature R_n measurements [11]. The room-temperature R_n was measured using an automated probing station (Ruckers and Kolls 683 A Semi-Automatic Wafer Prober). In order to prevent damaging our junctions, we took two precautions: First, to prevent electrostatic discharge (ESD) damage, the probing station pins were grounded before making contact to the junction pads. Second, we used the "make before break" method before applying current through the junction. This method consisted of introducing a resistive path parallel to the junction such that the current ran mainly through this resistor. This current path to the junction was then opened so current then flowed through the junction. This method prevented voltage from building up across the junction during the measurement.
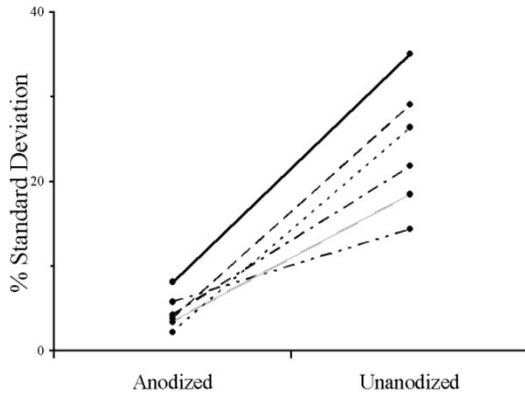
Fig. 4.   Comparison of cross-wafer critical-current-density standard deviation of anodized/unanodized wafer pairs. The wafers shown have J_c values ranging between 10^2 A/cm^2 and 10^3 A/cm^2. Lines connect data points on wafers whose trilayers were deposited together.

From the R_n values obtained at room temperature, we determined the approximate value of the critical current I_c of the junction. From the known junction area ($10 \times 10\ \mu$m^2, we then extracted the J_c value. Fig. 4 shows the J_c percent standard deviation across a wafer for six wafer pairs. Each pair was fabricated together, the only difference being the presence or absence of anodization. The percent standard deviation of J_c was typically $\sim 5\%$ for anodized wafers but $> 15\%$ for unanodized wafers. Overall, unanodized wafers had a factor of ~ 3 higher standard deviation compared to anodized wafers. Error in room-temperature R_n measurements due to the finite lead resistance and sizing errors could not account for this difference in critical-current-density uniformity [11].

IV. ANALYSIS AND DISCUSSION

Our results suggest that there exists in-process modification of J_c that is avoided or diminished by anodization. The wafer pairs we examined were simultaneously subjected to the same highly uniform oxidation process involved in producing the tunneling barrier, therefore making it unlikely for one wafer to differ significantly in J_c uniformity from the other. Isolating the cause of the modification remains difficult since many subsequent processing steps are required to produce useful junctions. Possible sources of damage or contamination of the junction barrier include: stress in the Nb film, plasma, and/or chemical sources (photoresist/developer, phosphoric acid, CMP slurry). Clearly, anodization reduces cross-wafer I_c spreads of large junctions ($> 2 \times 2\ \mu$m^2) suggesting that the anodic oxide layer retards attack of the junction. However, from separate room temperature and low temperature measurements, we have determined that anodization does not improve cross-wafer spread of small junctions ($< 2 \times 2\ \mu$m^2) since small junction I_c is mainly dominated by sizing variation rather than J_c variation and anodization does not appear to affect sizing variation.

V. CONCLUSION

Our central work involves the development and incorporation of an anodization process into an existing Nb superconducting fabrication process and demonstrating its effect on J_c uniformity. We initially developed the anodization procedure, then determined how to modify the existing standard process to include the anodization step. This work required thickness metrology development involving spectral reflectometry measurements, SEM/TEM imaging and step-height profile measurements. From the normal-state resistance measurements of junctions, we then determined the critical-current-density across anodized/unanodized wafer pairs. Our results show that anodization allows for higher J_c uniformity across anodized wafers than unanodized wafers. This enables us to produce the small ($< 1\%$) J_c cross-chip variation that is required for RSFQ circuits, and to increase the quantity of chips per wafer with the desired J_c.

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