Low-Power CMOS Rectifier Design for RFID Applications

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***Abstract*—We investigate theoretical and practical aspects of the design of far-field RF power extraction systems consisting of antennas, impedance matching networks and rectifiers. Fundamental physical relationships that link the operating bandwidth and range are related to technology dependent quantities like threshold voltage and parasitic capacitances. This allows us to design efficient planar antennas, coupled resonator impedance matching networks and low-power rectifiers in standard CMOS technologies (0.5-μm and 0.18-μm) and accurately predict their performance. Experimental results from a prototype power extraction system that operates around 950 MHz and integrates these components together are presented. Our measured RF power-up threshold (in 0.18-μm, at 1 μW load) was 6 μW $\pm$ 10%, closely matching the predicted value of 5.2 μW.**

***Index Terms*—Antennas, circuit theory, CMOS analog integrated circuits, rectifiers.**

I. Introduction

REMOTELY powered devices have become increasingly important over the past few years. One of the most important applications is radio frequency identification (RFID). RFID technology looks set to have far reaching implications for the global supply chain [1]. Other applications include bionic implants and low-power sensor networks. In these systems, RF power is transmitted by a "primary" or "reader" to one or many "secondaries" or "tags". The tags can be completely passive [2], [3], i.e., with no onboard batteries, or semi-passive, with a backup battery to supply some power [4]. The tags contain an antenna to capture RF energy, a rectifier to extract dc power from it, and processing and communication circuitry that runs off this dc power.

The first step in getting any remotely powered system to work is powering it up. The rectifier in these systems must extract enough dc power from incident electromagnetic radiation for the device to function [2], [5], [6]. Rectification is hard when the incident power levels are low. All rectifiers have an unresponsive dead zone at low voltage amplitudes and active dead-zone reduction techniques are difficult to implement since no power supply has been created yet. Fundamentally this is because rectification is a nonlinear operation and all physical systems and devices look linear for small signal amplitudes. We have examined the problem analytically, via simulations, and verified our predictions in a practical experimental system that operates near theoretical performance bounds.

This paper is organized as follows. In Section II, we discuss the basic theory of far-field power extraction systems. Sections III and IV describe, respectively, the design of low-power CMOS rectifiers and antenna and impedance matching networks for a UHF power extraction system. Section V develops a generic model of the power-extraction system that can be used to predict its performance. We summarize our experimental results in Section VI and compare them to predictions. Section VII summarizes our overall conclusions.

II. Theoretical Performance Bounds

To get good power-up range, we must improve the power-conversion efficiency of the rectifier at low input power levels. The rectifier dead zone severely decreases this efficiency when input voltage amplitudes are low. An impedance transformation that increases the impedance (and thus the RF voltage amplitude) at the rectifier input terminals is thus desirable. Networks of passive reactances can transform impedances, but over a limited range of frequencies. We want to maximize this bandwidth in order to ensure robust operation of the tag.

The resonant frequency of RFID tags often shifts considerably in the field because of their local environment (presence of conductive or dielectric materials, temperature variations and so on). A certain fraction of tags are thus never read. Tags should be designed to have intrinsically large bandwidths to minimize this problem. Since different parts of the world use different frequency bands for RFID, wide bandwidth is also necessary for global operation of the tags. Increased communication speed (data rates) between the reader and tags also become possible with increased bandwidth. However, a tradeoff exists between impedance-transformation ratio and bandwidth. In this section, we describe how this tradeoff affects the performance of our system.

A. Impedance Transformations

Theories of impedance matching seek to maximize the power transferred to a load from a source by using a lossless matching network. Consider matching the source impedance Z_0 to a parallel *RC* network with quality factor $Q_L = \omega R_p C_p$ over the required operational bandwidth B. Such networks are good models of rectifier input impedance Z_{in} at frequencies low enough for parasitic inductances to be neglected. The parallel resistance R_p includes both parasitic losses and power actually delivered to the load. Similarly, C_p consists of both linear and nonlinear components. Therefore, R_p and C_p depend on input signal level and the output (load). However, in this discussion we shall linearize the problem and assume that

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the input impedance is constant. This simplification is valid when rectifier efficiency is low, i.e., for small input signals. In particular, it is usually a reasonable approximation at signal levels corresponding to the power-up threshold[1] of the tag. The input impedance in this important case will thus be dominated by linear parasitic components and not by the rectifier itself.

The first design goal is to maximize R_p: this minimizes the RF power required for a given voltage swing at the rectifier input terminals. The antenna (which provides the source impedance Z_0) must now be matched to Z_{in} to maximize power transfer to the rectifier. Bode and Fano [7]–[9] analyzed a general version of this problem by assuming that Z_0 was purely resistive. Defining the reflection coefficient seen by the source as $\Gamma(\omega)$, they showed that

$$\left| \int_0^\infty \ln\left(|\Gamma(\omega)|\right) d\omega \right| \leq \frac{\pi \omega_0}{Q_{L0}} \tag{1}$$

where ω_0 is the center frequency of the matching bandwidth of interest, and $Q_{L0} = \omega_0 R_p C_p$. Equation (1) expresses the fundamental gain-bandwidth-like constraint of this problem. For a given load, if one wants a "high gain" matching network (one that realizes a very low $|\Gamma|$) one can only realize it over a narrow bandwidth.

Throughout this paper, *we shall assume that the power spectral density received by the tag antenna is uniform over a bandwidth B*. This is a reasonable approximation if $B \ll \omega_0$, (i.e., the fractional bandwidth is low). We want to maximize the range of ω where $|\Gamma(\omega)| \leq |\Gamma_m|$, where $|\Gamma_m|$ is the maximum allowable reflection coefficient magnitude. Since the area under the $\Gamma(w)$ curve is fixed, by (1), for a given load, the way to get maximum bandwidth is by having $|\Gamma(\omega)| = |\Gamma_m|$ over a bandwidth B, and be completely mismatched ($|\Gamma| = 1$) everywhere outside it. This ensures that $\ln(|\Gamma|) = 0$ everywhere outside one's desired bandwidth and contributes nothing to the integral in (1). In this case

$$\int_0^\infty \ln\left(|\Gamma(\omega)|\right) d\omega = B \ln\left(|\Gamma_m|\right) \tag{2}$$

giving one a theoretical upper bound on the achievable impedance matching bandwidth

$$B \leq \frac{\pi \omega_0}{Q_{L0}} \frac{1}{\ln\left(\frac{1}{|\Gamma_m|}\right)}. \tag{3}$$

Since $\ln(0) \to -\infty$ and the integral in (1) is finite, one cannot have a perfect match, where $\Gamma = 0$, unless $B = 0$, i.e., only at a finite number of frequencies. Secondly, the higher the Q of the load, the harder it is to match over a wide bandwidth. We assume that B is defined by a maximum allowable reflection coefficient magnitude $|\Gamma_m|$.

Most existing RF power extraction systems rely on a simple first-order impedance matching network where an inductive antenna resonates out the input capacitance of the rectifier (an L-match). We want to find out how the resultant bandwidth compares with the Bode–Fano limit. It can be shown that in this case, if $Q - L0 >> 1$, we get [10]

$$B = \frac{2\omega_0}{Q_{L0}} \frac{1}{\sqrt{\frac{1}{|\Gamma_m|^2} - 1}}. \tag{4}$$

The ratio of the bandwidths in the ideal (Bode–Fano limiting) case and the first-order LC match case (at the same value of $|\Gamma_m|$) is given by

$$f_b\left(|\Gamma_m|\right) = \frac{B_{\text{Bode–Fano}}}{B_{L-\text{match}}} = \frac{\pi}{2} \frac{\sqrt{\frac{1}{|\Gamma_m|^2} - 1}}{\ln\left(\frac{1}{\Gamma_m}\right)}. \tag{5}$$

The function $f_b(|\Gamma_m|)$ is plotted in Fig. 1. As expected, it is always greater than 1. The minimum value is $f_{b,\min} = 3.90$, which occurs at $|\Gamma_m| \approx 0.451$. Thus, we lose at least a factor of 4 in bandwidth over the theoretical limit when a simple L-match is used. More complicated matching networks perform better by making the reflection coefficient-bandwidth tradeoff in (4) more gentle. Interestingly, the related problem of impedance matching a resonant antenna to a resistive source impedance also leads to (5) [11].

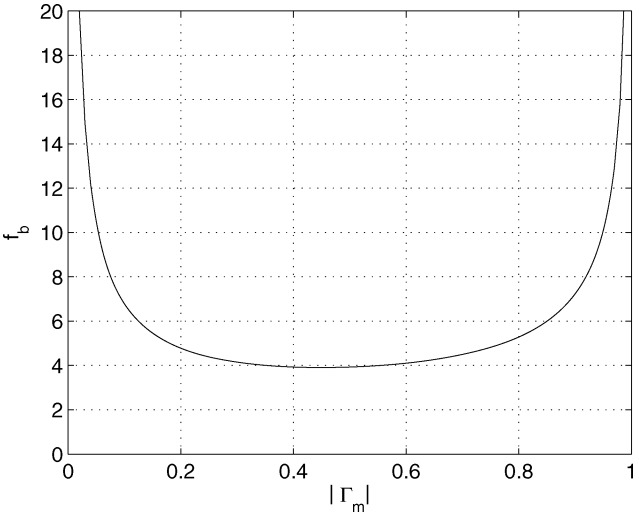

Fig. 1. Plot of f_b, the ratio of the maximum possible bandwidth to that achieved by a first-order impedance matching network, as a function of $|\Gamma_m|$.

B. Performance Bounds

We now consider passive far-field RF power extraction systems. If the radiation density around the receiving antenna is P_{rad}, the available power P_A at its terminals is given by

$$P_A = G_r P_{\text{rad}} \frac{\lambda^2}{4\pi} \tag{6}$$

where G_r is the tag antenna's gain and λ is the wavelength in the medium. R_p, the real part of the rectifier input impedance consumes the power delivered by the antenna. P_{diss}, the power dissipated in R_p, is

$$P_{\text{diss}} = \frac{V_{\text{in}}^2}{2R_p} \tag{7}$$

[1]The power-up threshold P_{th} is defined as the minimum available power at the antenna terminals that the rectifier needs for supplying enough power to the load.

where $V_{\rm in}$ is the amplitude of the RF voltage across the load. The maximum possible value of $P_{\rm diss}$ for a given electromagnetic field intensity is clearly P_A. This corresponds to an antenna impedance matched to the load. In general $P_{\rm diss} = (1 - |\Gamma|^2)P_A$, where $|\Gamma|$ is the magnitude of the reflection coefficient looking in from the antenna terminals. From (6) and (7), and writing the input admittance as $Y_{\rm in} = 1/R_p + jY_p$, $V_{\rm in}$ is given by

$$V_{\rm in} = \sqrt{\frac{(1 - |\Gamma|^2)\, G_r P_{\rm rad} Q_L \lambda^2}{2\pi Y_p}} \tag{8}$$

where $Q_L = Y_p R_p$. We want to increase $V_{\rm in}$ for given $P_{\rm rad}$. Normally G_r cannot be increased since tags have no *a priori* information about the spatial location of readers; thus their antennas must be nearly isotropic. Increasing physical size of the tag prevents us from lowering the operating frequency (i.e., increasing λ). As previously stated, what remains is to increase R_p, i.e., increase Q_L and decrease Y_p.

We define the input voltage amplitude when $P_A = P_{\rm th}$, the power-up threshold, to be $V_{\rm to}$, the threshold/turn-on voltage of the rectifier; its value depends on rectifier design and the load. The power-up threshold is a function of the operating bandwidth B. From (7), the threshold $P_{\rm th0}$ required to power up at a *single* frequency ω_0 where $|\Gamma| = 0$ is given by

$$P_{\rm th0} = V_{\rm to}^2 C_p \frac{\omega_0}{2Q_{L0}} \tag{9}$$

where the imaginary part of $Y_{\rm in}$ corresponds to a capacitor of value C_p. The power-up threshold for nonzero operating bandwidth is given by

$$P_{\rm th} = \frac{V_{\rm to}^2}{2R_p\,(1 - |\Gamma_m|^2)} = \frac{P_{\rm th0}}{1 - |\Gamma_m|^2}. \tag{10}$$

The minimum possible value of $P_{\rm th}$ for some fixed bandwidth B is given by the Bode–Fano criterion (from 3):

$$P_{\rm th,min} = \frac{P_{\rm th0}}{1 - \exp\left(-\frac{2\pi\omega_0}{BQ_{L0}}\right)} = \omega_0 C_p V_{\rm to}^2 F_1\left(\frac{B}{\omega_0}, Q_{L0}\right) \tag{11}$$

where

$$F_1\left(\frac{B}{\omega_0}, Q_{L0}\right) = \frac{1}{2Q_{L0}\left(1 - \exp\left(-\frac{2\pi\omega_0}{BQ_{L0}}\right)\right)}.$$

As Q_L increases, F_1 and $P_{\rm th}$ decrease monotonically. However, F_1 eventually saturates at $B/(4\pi\omega_0)$. $P_{\rm th,min}$ then becomes dependent only on the fractional bandwidth B/ω_0, not on Q_{L0}. Intuitively, the ideal Bode–Fano matching network is such that the loss of energy off resonance due to reflections as Q_L increases is compensated for by the increased voltage amplification at resonance provided by the high Q_L.

When a simple *L*-match is used instead, $P_{\rm th}$ is given by

$$P_{\rm th} = P_{\rm th0}\left[1 + \left(\frac{BQ_{L0}}{2\omega_0}\right)^2\right] = \omega_0 C_p V_{\rm to}^2 F_2\left(\frac{B}{\omega_0}, Q_{L0}\right) \tag{12}$$

where

$$F_2\left(\frac{B}{\omega_0}, Q_{L0}\right) = \frac{1 + \left(\frac{BQ_{L0}}{2\omega_0}\right)^2}{2Q_{L0}.}$$

If $V_{\rm to}$ and C_p are fixed, $P_{\rm th}$ decreases monotonically as Q_L increases when the Bode–Fano limit is reached. If an *L*-match is used instead of the previous ideal Bode–Fano matching network there is an optimal value of Q_{L0} that minimizes $P_{\rm th}$. This is given by

$$Q_{L0,\rm opt} = \frac{2\omega_0}{B} = \frac{2}{\left(\frac{B}{\omega_0}\right)} \tag{13}$$

where B/ω_0 is the fractional bandwidth. The relationships of (10) and (11) are plotted in Fig. 2. Intuitively, in the *L*-match case, the loss of energy off resonance due to reflections as Q_L (R_p) gets higher is not compensated for by the increased amplification at resonance provided by the high Q_L.

In general, impedance matching only starts to become an issue for bandwidths large enough to make ω_0/B comparable with Q_L. Thus, the fractional bandwidth B/ω_0 is important in determining the performance of power extraction systems. Broadband power extraction systems are more difficult to build efficiently than narrowband ones.

C. A Note on the Antenna

Application of the Bode–Fano criterion requires a purely resistive source impedance. We have so far assumed this, but antennas cannot satisfy this requirement. All antennas have reactive components to their terminal impedances because of near field energy storage. Only the impedance of a propagating wave in an unbounded medium can be purely real. This means that, conceptually, we should consider our purely resistive source impedance for applying the Bode–Fano criterion to be the wave impedance of the propagation medium ($Z_0 = 377\ \Omega$ for vacuum). Thus, the impedance matching network as we define it includes the antenna, which also acts as an impedance transformer.

D. Optimization Metric

One needs a metric to optimize rectifier performance. Equations (11) and (12) define the power-up threshold as a function of various system parameters. Our approach is based on the observation that, for a particular technology, Q_{L0} of the rectifier input impedance tends to remain constant as device size and the number of stages vary in the rectifier. Since B and ω_0 are fixed by system requirements and the F-functions in (11) and (12) are fixed, the designer only controls $V_{\rm to}$ and C_p. A suitable metric is thus $V_{\rm to}\sqrt{C_p}$. This quantity, which we shall call the optimization metric (OM), is proportional to $\sqrt{P_{\rm th}}$; the lower its value, the better.

Rectification curves can be used to find $V_{\rm to}$; it is the input amplitude $V_{\rm in}$ that corresponds to the load operating point $(V_{\rm min}, I_{\rm min})$. Here $V_{\rm min}$ is the minimum supply voltage required by the circuits on the tag to function, and $I_{\rm min}$ is the supply current drawn in this condition. Calculating $V_{\rm to}$ amounts to inverting the rectifier's nonlinear input–output

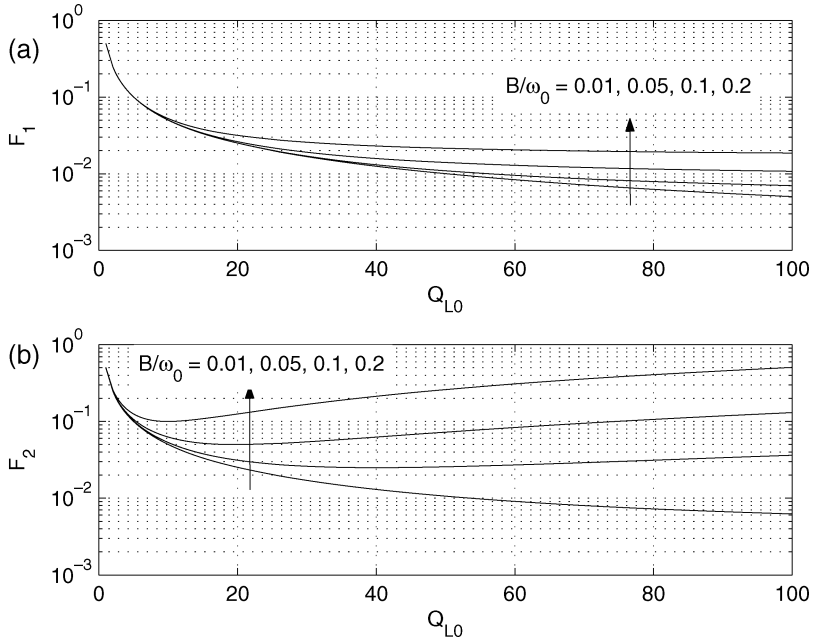

Fig. 2. Functions (a) F_1 and (b) F_2 plotted versus Q_{L0} for different values of fractional bandwidth B/ω_0.

TABLE I
CMOS PROCESS PARAMETERS

Parameter	AMI 0.5μm	UMC 0.18μm
Minimum MOS length	0.5μm	0.18μm (normal V_T) 0.24μm (low V_T)
NMOS V_T (nominal)	0.65V	0.31V (normal V_T) 0.02V (low V_T)
PMOS V_T (nominal)	-0.95V	-0.46V (normal V_T) -0.23V (low V_T)
Poly sheet resistance	25$\Omega/\square$ (non-silicided)	8$\Omega/\square$ (silicided)
Linear capacitors	poly-poly (0.9fF/μm^2)	metal-metal (1.0fF/μm^2)
Gate oxide capacitance	2.4fF/μm^2	8.4fF/μm^2

function $V_L = G(V_{\rm to}, I_L)$ for $V_L = V_{\rm min}$ and $I_L = I_{\rm min}$. Electromagnetic simulations or experimental results can be used to estimate C_p. Since $V_{\rm to}$ is a function of V_L and I_L, OM is load dependent. For a given load, OM is inversely proportional to $\sqrt{\eta}$, where η is the rectifier efficiency.

In practice C_p will be increased by extra package and bond pad capacitances which don't obey our constant-Q assumption. Fortunately, their losses are usually small enough that they don't significantly affect R_p, so the single-frequency power-up threshold is fixed and OM still helps us to optimize rectifier performance. However, by increasing the Q seen at the rectifier input, these elements make operating over a finite bandwidth B more difficult.

III. CMOS RECTIFIER DESIGN

For many power extraction applications, such as RFID, minimizing cost is a primary goal. Hence, we want to use standard CMOS processes for our design. Use of the AMI 0.5-μm CMOS process with parameters shown in Table I is assumed in this section. These processes generally do not support Schottky diodes, so all-MOS rectifiers become important and are now studied.

A. Rectifier Topologies

When input amplitudes are low, a single rectifier stage does not usually produce high enough dc output voltage V_L. A number of rectifier stages can be cascaded in a charge pump-like topology to increase V_L. The RF inputs are fed in parallel into each stage through pump capacitors C_P, and the dc outputs add up in series to produce V_L. This is shown schematically in Fig. 3. Each stage contains rectifying elements like transistors and/or diodes. Increasing the number of stages decreases $V_{\rm to}$ but increases C_p. Thus, there is usually an optimum number of stages for a given topology that minimizes the rectifier OM.

B. Four-Transistor Cell

We designed several MOSFET-based rectifier structures in standard CMOS processes. The most efficient topology was found to be the self-driven synchronous rectifier shown in Fig. 4(a). We call this structure the four-transistor cell. It performs better than diode-based rectifiers when Schottky diodes with low turn-on voltage are not available. V_P and $\overline{V_P}$ are complementary (differential) ac signals, and the rectified dc voltage is $V_H - V_L$.

The operation of the four-transistor cell is easily understood if V_P and $\overline{V_P}$ are assumed to be large enough to turn the transistors on and off. The transistors then operate as switches. During half of the switching cycle, V_P is high and $\overline{V_P}$ is low. In this case $M1$ and $M4$ are on and $M2$ and $M3$ are off. Current flows into V_H through $M4$ and out of V_L through $M1$. During the other half of the cycle, $M1$ and $M4$ turn off and $M2$ and $M3$ are on, but the current flow at V_H and V_L has the same direction as before. Thus, a dc voltage is developed across a load connected between V_H and V_L. In general, $V_{\rm DC} = (V_H - V_L) = (2V_{\rm RF} - V_{\rm drop})$, where $V_{\rm RF}$ is the ac voltage amplitude of V_P or $\overline{V_P}$ and $V_{\rm drop}$ represents losses due to switch resistance and reverse conduction.

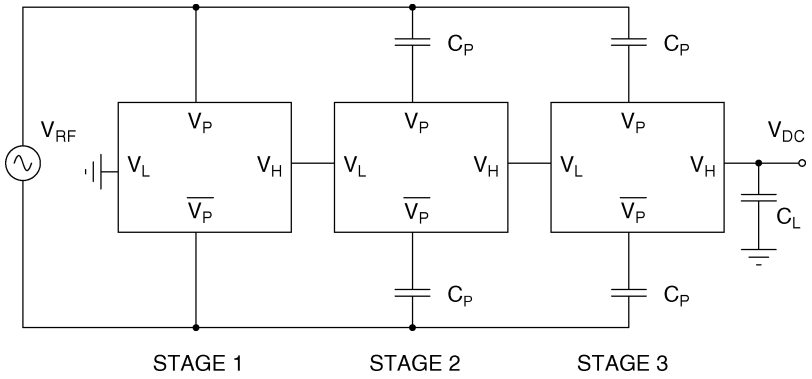

Fig. 3. Rectifier formed by cascading N rectifying cells in series. For power extraction applications $V_{\rm RF}$ is generated by an antenna and impedance matching network.

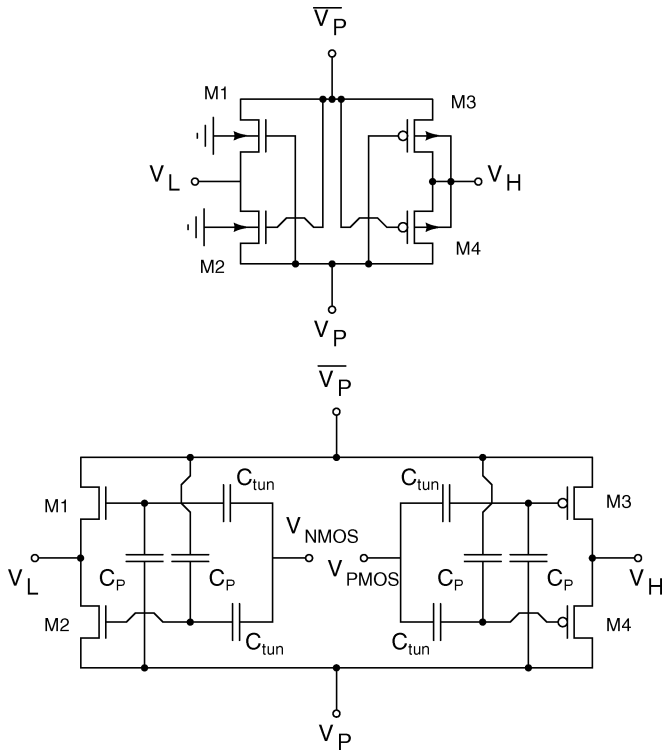

Fig. 4. Four-transistor cell using (a) normal MOS transistors and (b) floating-gate MOS transistors.

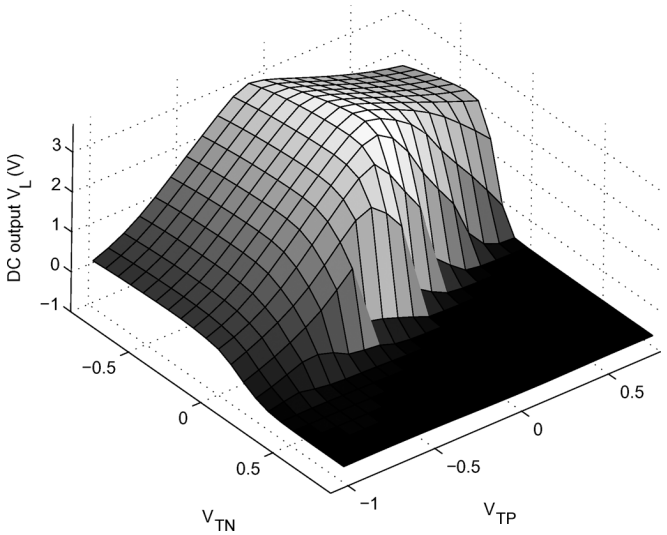

Fig. 5. Effects of experimentally changing the effective nMOS and pMOS threshold voltages $V_{\rm TN}$ and $V_{\rm TP}$ in a 0.5-μm rectifier by using floating gates.

Unwanted parasitic bipolar transistors can cause latch-up when MOS rectifiers are implemented in CMOS processes [5]. However, our rectifiers do not suffer from this problem. This is mainly because our operating frequencies are greater than the f_T of these parasitic devices. In addition, at our operating power levels, RF voltage and current amplitudes are relatively small. To further reduce the chances of latch-up, we used standard layout techniques, such as physically separating the nMOS and pMOS transistors and using guard rings for isolation.

C. Cascading Rectifier Cells

The maximum value of $(V_H - V_L)$ that can be obtained from a single four-transistor cell is limited to $2V_{\rm RF}$, where $V_{\rm RF}$ is the input RF amplitude. To obtain larger values of $V_{\rm DC}$, N cells can be cascaded in series as shown in Fig. 3. V_P and $\overline{V_P}$ for the first stage are directly connected to $V_{\rm RF}$. Succeeding stages are capacitively coupled to $V_{\rm RF}$ through C_P, allowing $V_{\rm DC}$ to build up at the output. The circuit behaves as a charge pump voltage multiplier.

One expects the output dc voltage of the Nth stage to be $V_{\rm DC} = N(2V_{\rm RF} - V_{\rm drop})$. In practice $V_{\rm DC}$ is lower because $V_{\rm drop}$ increases in the later cells. The primary cause is increased body bias on the nMOS transistors.[2] The rectifier output impedance $R_{\rm out}$ is the sum of the output impedances of all previous stages and thus increases down the cascade. In addition, the stages do not have to be identical, and loads can be connected at multiple locations. The output impedance of a stage can be decreased by making the transistors in it wider, which decreases their on-resistance. Large initial stages are useful for driving loads like digital circuits which have liberal minimum supply voltage requirements. Typical analog circuits, by contrast, have strict $V_{\rm DD}$ requirements and should be driven from later stages.

[2]A standard n-well CMOS process is assumed here.

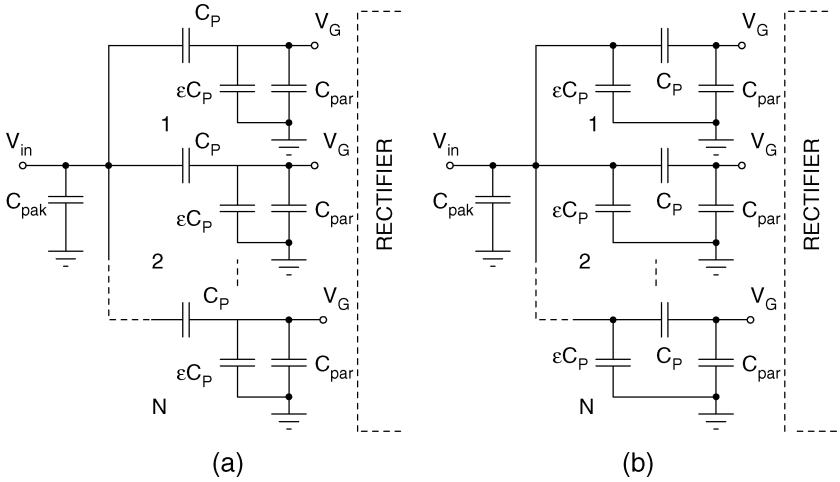

Fig. 6. Circuit model used to find optimum pump capacitance C_P when the RF signal $V_{\rm in}$ is fed to the (a) top and (b) bottom plate of C_P.

D. Floating-Gate Rectifier

To investigate the effect of transistor threshold voltage variations on rectifier performance, we replaced each simple rectifier cell with the floating-gate version shown in Fig. 4(b). This circuit allows us to independently program nMOS and pMOS threshold voltages $V_{\rm TN}$ and $V_{\rm TP}$ by depositing charge on the floating gates. We utilized bidirectional electron tunneling through the thin poly-poly oxide layers in C_{tun} for this purpose. In addition, bias voltages $V_{\rm nMOS}$ and $V_{\rm pMOS}$ can be used to fine-tune $V_{\rm TN}$ and $V_{\rm TP}$. Experimental results are shown in Fig. 5 for a five-stage rectifier.

We see that an optimum $(V_{\rm TN}, V_{\rm TP})$ pair exists that maximizes the output dc voltage at a given input RF power level. At high threshold voltages, the transistors do not switch on completely, leading to high rectifier output resistance and low output voltage. Conversely, at very low threshold voltages, the transistors do not switch off completely, leading to unwanted reverse current flow, again lowering the output voltage. The optimum threshold voltages (at zero body bias) are observed to be $V_{\rm TN} \approx 0.1$ V and $V_{\rm TP} \approx -0.3$ V.

Floating-gate rectifiers tradeoff lower transistor threshold voltage with increased input capacitance and layout area. Most CMOS processes do not provide two polysilicon layers, making floating gates impossible. Also, the programming process is slow and potentially impacts circuit reliability. We built working UHF versions but used them primarily for experimental demonstration of the presence of optimum transistor threshold voltages. Since their actual benefits are unclear, floating-gate rectifiers are not discussed further.

E. Optimization

In this section, we describe a procedure to optimize pump capacitor and transistor sizes and number of rectifier stages to minimize OM. To simplify the problem, stages are assumed to be identical. The pump capacitor C_P in Fig. 3 directly affects circuit performance. Consider the capacitance model shown in Fig. 6. The bonding pad and package capacitances are independent of the size of the rectifier circuit (i.e., the number of stages), and lumped together into $C_{\rm pak}$. $C_{\rm par}$ is the total parasitic capacitance to ground at the input of each stage that is independent of C_P. $C_{\rm par} \propto W$, the transistor width, since it is due to transistor parasitics. The capacitance between the bottom plate of C_P and ground is ϵC_P, and there are N rectifying stages. Fig. 6 shows two cases: the RF input is connected to either the top or bottom plate of C_P.

Consider the top plate case first. The RF amplitude at the transistor gates V_G is the actual input that the rectifier receives. V_G is lower than $V_{\rm in}$, the theoretical input amplitude, because of the capacitive voltage divisions shown in Fig. 6. In this case

$$\alpha = \frac{V_G}{V_{\rm in}} = \frac{C_P}{C_{\rm par} + (1+\epsilon)C_P}. \tag{14}$$

For optimization using OM, $C_{\rm pak}$ is ignored for reasons discussed earlier. The input capacitance seen by the RF input is thus given by

$$C_p = NC_P \frac{C_{\rm par} + \epsilon C_P}{C_{\rm par} + (1+\epsilon)C_P}. \tag{15}$$

Similarly, for the bottom plate case, one gets

$$\alpha = \frac{C_P}{C_P + C_{\rm par}}$$
$$C_p = NC_P \left[\epsilon + \frac{C_P C_{\rm par}}{C_{\rm par} + C_P}\right]. \tag{16}$$

The resultant rectifier OM$\propto \sqrt{C_p}/\alpha$. As C_P increases, α and C_p both increase, but by different amounts, resulting in an optimum value of C_P that minimizes the OM when $C_{\rm par}$ is fixed. Fig. 7 shows calculated values of rectifier OM as a function of C_P for different values of $C_{\rm par}$ and $\epsilon = 0.15$. The two feed methods give similar results around the minimum. Not surprisingly, the optimum C_P value increases as the devices get bigger and $C_{\rm par}$ increases. Fortunately, the curves are rather flat around the optimum. We thus fix C_P in the 150–250-fF range for our designs.

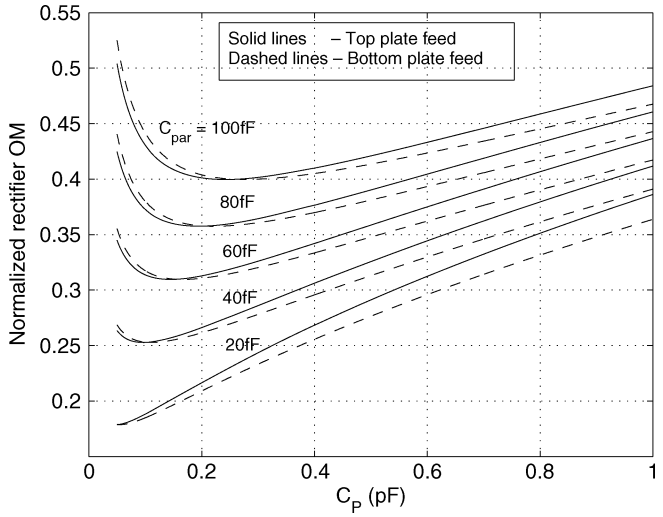

Fig. 7. Calculated effect of pump capacitor C_P sizing on rectifier OM in the AMI 0.5-μm process. Values have been normalized.

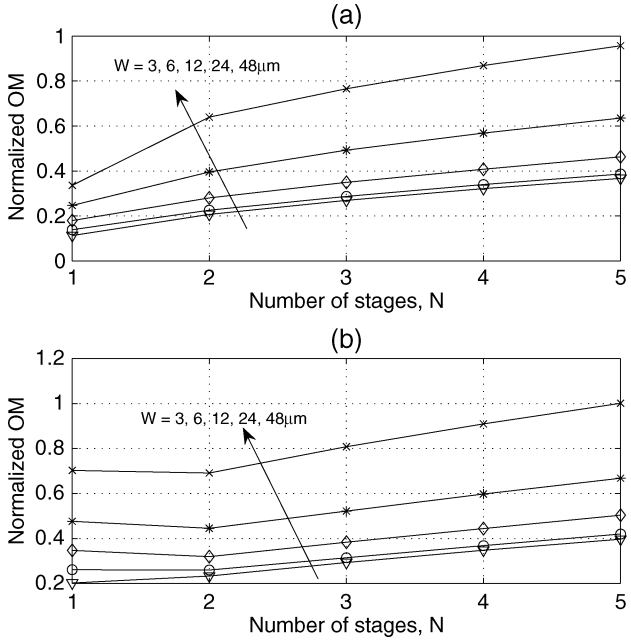

Fig. 8. Relative performance of 0.5-μm CMOS rectifiers with different device sizes W, number of stages N and load voltage requirements V_L. L is fixed at 0.6 μm. (a) $V_L = 1V$, $I_L = 2\ \mu A$; (b) $V_L = 2V$, $I_L = 2\ \mu A$

Optimization of transistor sizes is based on simple scaling relationships. Bigger W/L means bigger parasitic capacitance and smaller series resistance. The main contributor to series resistance is the gate resistance R_G; as W increases, more gate fingers can be used, so R_G decreases. Thus, the Q remains roughly constant, while R_p decreases. L is kept fixed at the minimum allowed value in the process and W is varied to change the device size. The voltage drop per stage scales as $\log(L/W)$ for subthreshold operation, and as $\sqrt{L/W}$ above threshold, and thus is a weak function of device size.

The optimal device sizing and number of stages is now found by calculating OM values. OM curves are found for rectifiers with various device sizes, number of stages and load voltage requirements. The results are shown in Fig. 8 for a fixed 2 μA load current. The optimum number of stages depends on the rectifier dead zone and is likely to increase with process scaling. This is because advanced processes have low threshold voltages; each stage efficiently builds up small voltage increments, resulting in a lower dead zone. However, increasing V_L requirements always degrade OM. Thus, tag circuits must be designed to operate on the lowest possible power supply rails. Our final design was designed for a 2 μA load at 1 V and had three stages with all the devices sized $W/L = 6\ \mu\text{m}/0.6\ \mu\text{m}$.

F. 0.18-μm Rectifier

In this section we describe a rectifier designed in the UMC 0.18-μm CMOS process and discuss some issues not considered so far. Relevant process parameters are shown in Table I. Moving to the more advanced process improves performance in several ways. The lower transistor threshold voltages reduce the turn-on voltage V_{to} of the rectifier and also allow circuits on the tag to operate at reduced V_{DD}, thereby reducing power consumption. A 0.5-V power supply becomes sufficient, even for analog components [12]. Secondly, lower polysilicon sheet resistance and availability of high-Q metal–metal capacitors lowers parasitic input resistance at the rectifier terminals. Finally, layout area decreases significantly.

The optimization strategy described in this section suggests that a two-stage rectifier is optimal in this case (a nominal load of 4 μA at 0.5 V was assumed). Low-V_T transistors are used since they significantly reduce the turn-on voltage of the rectifier. Interestingly, the use of zero-V_T transistors, which have even lower threshold voltages, worsens performance and increases the rectifier turn-on voltage. Increased reverse leakage is the problem. This matches our earlier observation of an optimum transistor V_T (see Fig. 5).

We also implemented a backscatter modulator. The modulator consists of a 50-fF capacitor that can be switched in and out in parallel with the RF terminals using a nMOS switch. The transistor is sized such that a voltage of 0.4 V on MOD, the gate terminal, is enough to turn it on. Since the ripple-filtering load capacitor C_L at the output of the rectifier does not have to be linear, it is implemented using nMOS capacitors to reduce layout area. Gate-oxide capacitance density C_{ox} increases as technology scales, reducing the layout area of C_L. The value of C_L has to be chosen to guarantee normal circuit operation even when the RF power from the tag is not available for a time t_{low}. The maximum value of t_{low} may occur either during communication in either direction and depends on the protocol being used. If we assume that most of the load on the rectifier is digital circuitry, the minimum allowable value of C_L is given by

$$C_{L,\min} = C_{\text{sw}} \frac{t_{\text{low}}}{T_{\text{clk}} \ln\left(\frac{1}{\alpha}\right)} \tag{17}$$

where C_{sw} is the total capacitance being switched between V_{DD} and ground by the digital load, T_{clk} is the on-board clock frequency and $(1-\alpha)V_{\text{DD}}$ is the amount by which V_{DD} drops after t_{low}. The clock period T_{clk} is usually proportional to t_{low}. For example, since $I_L = C_{\text{sw}} V_{\text{DD}}/T_{\text{clk}}$, a nominal load of 4 μA at 0.5 V corresponds to $C_{\text{sw}} = 8$ pF when $T_{\text{clk}} = 1\ \mu$s. If we assume that the minimum acceptable value of $\alpha = 0.8$ and $t_{\text{low}} = 2T_{\text{clk}} = 2\ \mu$s, we get $C_{L,\min} = 71.7$ pF. This value

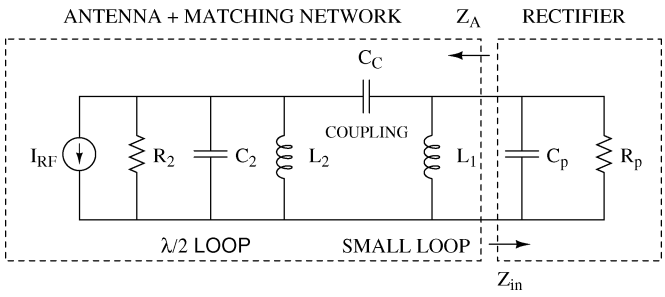

Fig. 9. Equivalent circuit of the rectifier (chip), antenna and impedance matching network.

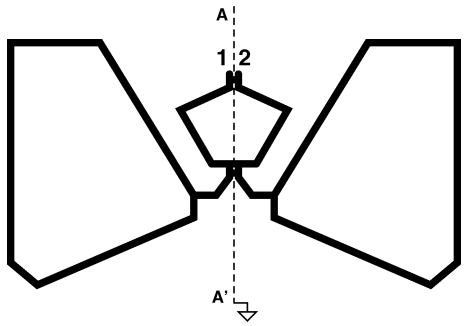

Fig. 10. Physical structure of the final tag antenna. The rectifier chip is fed differentially from ports 1 and 2.

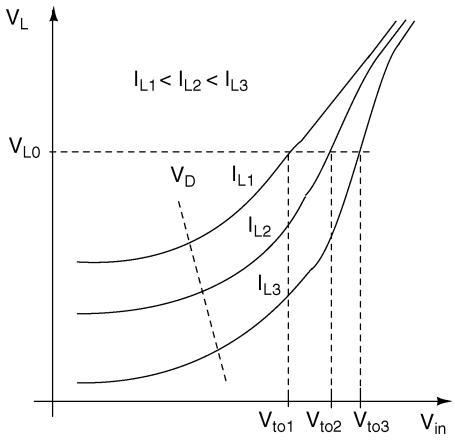

Fig. 11. General rectifier input–output voltage curves for different values of load current.

was used in our design. An over-voltage protection circuit consisting of a chain of diode-connected transistors to ground was also added at the rectifier output node.

IV. Antenna Design

A. Coupled Resonators

An effective way of improving impedance matching bandwidth is to use coupled resonators. The idea is to use resonant circuits of a particular type—either series or parallel—and couple them using impedance inverters (gyrators) known as *K* and *J* inverters [9]. Impedance inverters (lumped or distributed) transform parallel resonances to series resonances and vice versa. Coupling several resonators in this way splits their resonant frequencies and produces a higher order bandpass response in the reflection coefficient. We have used this idea in our matching network design to approach the Bode–Fano limit more closely than a simple *L*-match can.

B. Antenna and Matching Network

We created an antenna that was impedance matched to the rectifier through two coupled resonators. The rectifier input impedance at frequencies of interest is capacitive and can be represented as C_p in parallel with a resistance R_p. To create the first resonator, C_p was resonated with a parallel inductor L_1. This created the first (parallel) resonant circuit shown in Fig. 9. The antenna itself acted as the second resonant circuit. We used a parallel resonant half wavelength loop antenna because of its simplicity and relatively small area. The antenna is represented in Fig. 9 by the $R_2 - L_2 - C_2$ resonant tank. The two resonators—the chip and the antenna—were coupled using a J-type impedance inverter (i.e., C_C couples the two resonators) to obtain a second-order impedance matching network.

It can be shown that second-order matching networks have approximately double the bandwidth of first-order networks such as *L*-matches [13]. Increasing the matching network order beyond two was not attempted since the resultant bandwidth increments rapidly diminish. In fact, infinite-order networks can only do as well as the Bode–Fano limit.

Fig. 10 shows the physical structure of the tag antenna. The antenna is planar and uses a single metal layer on a printed circuit board. The small loop creates L_1; the large loops produce R_2, L_2, and C_2. The transmission lines connecting the inner loop with the larger ones produce the coupling capacitance C_C. These short lengths of line look capacitive because the resonant antenna terminating it looks almost like an open circuit. During fully differential operation, the line of symmetry AA' acts as a virtual ground plane. The entire antenna can be regarded as the combination of two single ended antennas back to back. The antenna feeds the rectifier chip differentially (between terminals 1 and 2) though a short length of coplanar strips line. The total size of the antenna is about $2.8'' \times 1.7''$, and the simulated gain is 1.5 dBi at 900 MHz. The radiation pattern is similar to that of a half-wave dipole, with minima perpendicular to the AA' axis.

An important practical advantage of our antenna compared to a simple dipole is that it provides a dc short between the rectifier input terminals. The virtual RF ground plane AA' between them can be tied to chip ground (substrate), thereby grounding both input terminals at dc and providing ESD protection.[3]

V. System Modeling

In this section, we develop an semi-empirical model of the nonlinear power-extraction system that provides insight and allows its performance to be estimated quantitatively.

A. Rectifier Model

The input–output voltage curves of a rectifier have the general shape shown in Fig. 11 for different values of load current I_L. The curves get closer together as the input voltage am-

[3]The rectifier architecture shown in Fig. 3 needs to be slightly modified: like the other stages, the first stage should also be capacitively coupled to the input RF signal using C_P.

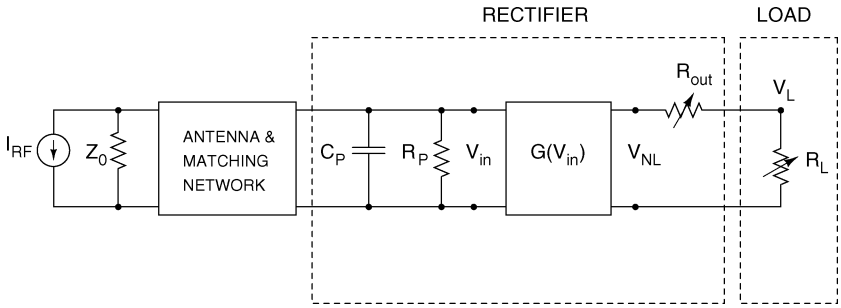

Fig. 12. Model of RF power extraction system.

plitude increases because the rectifier's output impedance drop $I_L R_{\rm out}$ increases. Integrated circuits behave like nonlinear resistive loads; $V_{\rm min}$ is the minimum allowable supply voltage.

In general the rectification curves shown in Fig. 11 are functions of frequency. However, this frequency dependence shall be ignored since it is much weaker than the frequency dependence of the properties of the antenna and impedance matching network. The power extraction system model is then shown in Fig. 12. The rectifier voltage gain $G(V_{\rm in})$ is given by the slope of the curves in Fig. 11. It is small for small $V_{\rm in}$, increases to approximately N (the number of rectifier stages), and decreases slowly for large $V_{\rm in}$ because of two reasons: body effect and increased reverse (off-state) leakage. $R_{\rm out}$ represents the output resistance of the rectifier and is a strongly decreasing function of $V_{\rm in}$. It is roughly equal to $N \times R_{\rm on}$, where $R_{\rm on}$ is the on-resistance of a single switch. We find rectification curves from circuit simulations; the quantities $G(V_{\rm in})$ and $R_{\rm out}(V_{\rm in})$ can then be calculated and approximated by parameterized functions.

B. Load Model

As the load current supplied by the rectifier increases, the input quality factor decreases since an additional loss mechanism has appeared in the system. We assume no load voltage regulation and divide the load current I_L into analog and digital parts, as follows:

$$\begin{aligned} I_L &= I_a + I_d \\ &= I_{b0}\left(1 - \exp\left(-\frac{V_L}{a}\right)\right)(1 + bV_L) + \beta C_T V_L \end{aligned} \quad (18)$$

where I_{b0} is a nominal analog bias current, a, b and β are constants and C_T is the total load capacitance being driven by the digital circuitry. The parameters a and b roughly correspond to transistor parameters $V_{\rm dsat}$ and λ, the Early effect constant. The effective load resistance $R_L = V_L/I_L$ is now added to the rectifier output resistance $R_{\rm out}$ and transformed to an effective shunt resistance $R_{\rm eff}$ loading the input terminals of the rectifier and lowering the Q, as follows,

$$R_{\rm eff} = \frac{R_{\rm out} + R_L}{2\left[G(V_{\rm in})\right]^2}. \quad (19)$$

The $2[G(V_{\rm in})]^2$ term arises from inverting the rectifier's ac input to dc output curve while conserving RMS power. The resultant quality factor of the rectifier input is then

$$Q_L = \frac{Q_{L0}}{1 + \frac{R_p}{R_{\rm eff}}} \quad (20)$$

where Q_{L0} is the no-load quality factor set by R_p and the input capacitance C_p. Q_L decreases as the input RF amplitude increases and $R_{\rm eff}$ decreases. The loading due to $R_{\rm eff}$ acts as a natural gain control feedback loop for the system. Finally, the power-conversion efficiency of the rectifier is given by

$$\eta = \frac{V_L I_L}{P_A}. \quad (21)$$

The model equations can now be iterated to find self-consistent solutions for the input voltage $V_{\rm in}$, the no-load voltage V_{NL} (i.e., for $I_L = 0$) and the load voltage V_L as the available RF power P_A is varied. The iteration procedure, which must be repeated for every value of P_A, starts by assuming that $Q_L = Q_{L0}$, the small signal value, and calculating the resultant value of $V_{\rm in}$. The function $G(V_{\rm in})$ can now be evaluated, allowing V_{NL} to be found. The dc operating point (V_L, I_L) and the resistances R_L and $R_{\rm eff}$ can now be found numerically since both $R_{\rm out}(V_{\rm in})$ and the *I–V* characteristics of the load are known. The value of Q_L is modified based on this value of $R_{\rm eff}$ and a new value of $V_{\rm in}$ results. The cycle is repeated till the value of $V_{\rm in}$ converges.

The effect of changing the type of load can also be evaluated. For example, suppose the load is a linear resistor R_L and there are three rectifier stages. Assume the following parameter values: $R_L = 500$ kΩ, $Q_{L0} = 60$, $C_p = 1.2$ pF, $\omega_0 = 2\pi \times 900$ MHz and $B = 2\pi \times 1$ MHz (this bandwidth is low enough that the type of matching network used is irrelevant). The predictions of the model of Fig. 12 with (19), (20) and (21) are shown as dashed curves in Fig. 13. The existence of a "dead zone" for V_L at low values of available power P_A is seen in the flat response of V_L with P_A when P_A is low.

Experimental results from a UHF power extraction system having similar parameter values to those used in the model are shown as solid curves in Fig. 13. We see that our model fits experimental data reasonably well. In order to obtain this data, we set up the power-extraction system at a fixed distance from a transmitting antenna. The transmitted frequency was also held constant (at 900 MHz) during the experiment. The available power P_A was changed by varying the transmitted power level. In order to obtain an accurate estimate of P_A, actual path loss was measured at the operating frequency using a network analyzer and subtracted from the transmitted power.

VI. Experimental Results

A. Rectifier Testing

We have fabricated rectifier designs in standard CMOS processes with 0.5- and 0.18-μm minimum feature size. Performance in both technologies has been characterized. However,

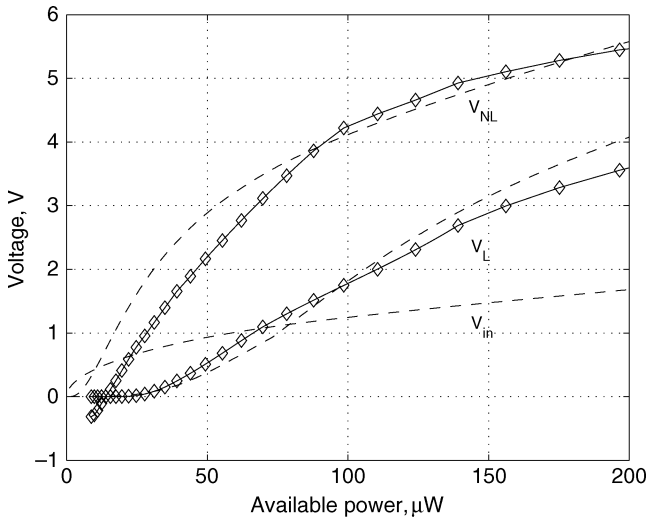

Fig. 13. Rectifier power-up characteristics predicted by the model (dashed lines) versus experimental results (solid lines). The AMI 0.5-μm CMOS technology was used.

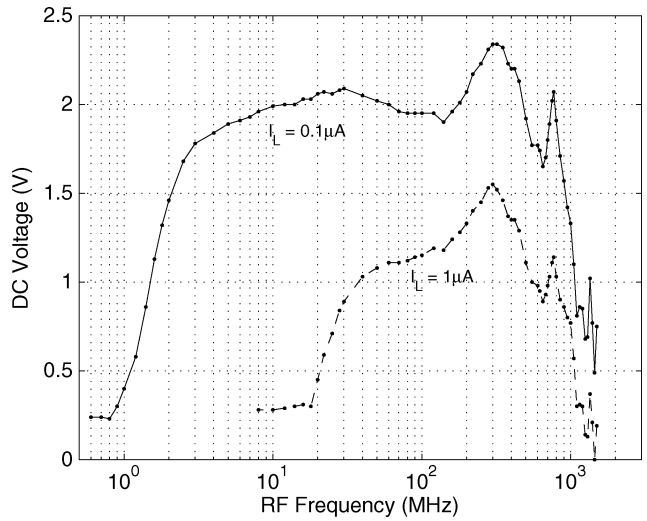

Fig. 14. Measured frequency response of a three stage rectifier in 0.5-μm CMOS for different values of load current I_L. The low-frequency input amplitude was 1.1 V.

certain experimental results are only shown for one technology. This is because their trends (though not absolute values) were similar in both cases. Best performance numbers were obtained in the 0.18-μ process.

Fig. 14 shows the measured frequency response of a three-stage 0.5-μm rectifier for various values of load current I_L. Impedance mismatch between the 50-Ω output impedance of the signal source and the input impedance of the rectifier was reduced by using a 10-dB resistive attenuator. Oscillations in the output voltage seen in Fig. 14 are due to the residual mismatch. The rectifier response itself is bandpass; it has a lower cutoff frequency and high-frequency roll-off and is approximately constant in between. The low-frequency cutoff occurs when the impedance of the pump capacitor C_P becomes comparable to that of the load. The high-frequency cutoff occurs when bond wire and parasitic inductances resonate with the rectifier's input capacitance.

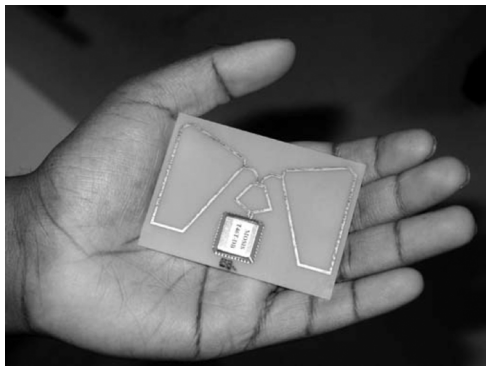

Fig. 15. Photograph of completed power extraction system.

The input impedance of the 0.5-μm rectifier with and without chip packaging was found using a network analyzer. The bare rectifier, directly wire bonded to a printed circuit board, had an input impedance of $Z_{\rm in} = (41 - j650)\ \Omega$ at 900 MHz. This corresponds to a capacitance of $C_{\rm rect} = 0.27$ pF. The relatively large resistive component, which increases the power-up threshold, is due to the high sheet resistance ($\approx 25\ \Omega/\square$) of the nonsilicided polysilicon used in transistor gates and capacitor plates in this process. The input quality factor is $Q_{L0} = 15.9$, corresponding to a parallel resistance $R_p = 10.3$ kΩ. At the power-up threshold, the rectifier efficiency is low and this is the main loss mechanism. We thus estimate the power-up threshold for single-frequency operation ($|\Gamma| = 0$) to be

$$P_{\rm th} \approx \frac{V_{\rm to}^2}{2R_p}. \tag{22}$$

For $I_L = 2\ \mu$A and $V_L = 1$ V (i.e., a 2 μW load), simulations predict $V_{\rm to} = 1.12$ V for a three stage rectifier. Thus, we estimate $P_{\rm th} = 61\ \mu$W. Similar calculations for the 0.18-μm rectifier result in $R_p = 8.2$ kΩ, $V_{\rm to} = 0.36$ V when $I_L = 4\ \mu$A and $V_L = 0.5$ V (2 μW load), and a predicted power-on threshold of 8 μW. If the load is reduced to 1 μW ($I_L = 2.5\ \mu$A at $V_L = 0.4$ V), $V_{\rm to}$ decreases to 0.29 V and the power-on threshold to 5.2 μW.

The rectifiers were also tested in leadless chip carrier (LCC) packages. The input capacitance now increased; however R_p was almost unchanged since the package was relatively lossless in this frequency range. Thus, the package did not affect the power-up threshold over narrow bandwidths; however, it made broadband operation more difficult by increasing Q_L. It can be shown that Q_L increases by a factor of approximately $(1 + C_{\rm pack}/C_{\rm rect})$, where $C_{\rm pack}$ is contributed by the package and $C_{\rm rect}$ by the rectifier.

B. System Testing

We designed power extraction systems for UHF RFID applications around 950 MHz using the principles developed so far. The antenna was fabricated by a commercial printed circuit board vendor. The rectifier was enclosed in a LCC package. A photograph of the completed system is shown in Fig. 15. The total size was $2.9'' \times 2.0''$, most of which was occupied by the antenna.

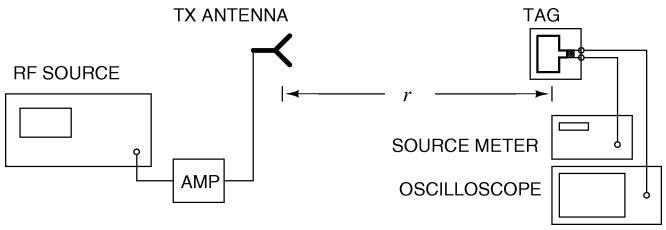

Fig. 16. Setup used for testing the power extraction system.

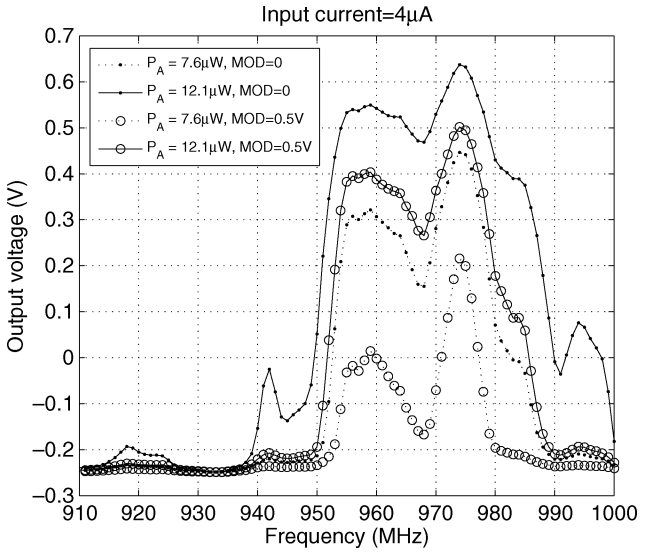

Fig. 17. Measured frequency response of the 0.18-μm tag for different available power levels P_A with the modulation input MOD turned on and off. The load current was $I_L = 4$ μA. All received power levels are uncertain by approximately $\pm 10\%$.

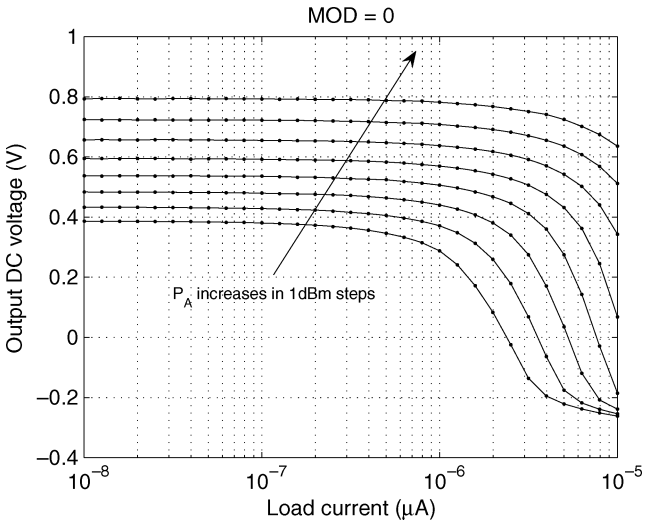

Fig. 18. Measured load curves of the 0.18-μm tag. Load current I_L is varied from 10 nA to 10 μA for available power levels P_A ranging from -24.7 ± 0.5 dBm (3.4 μW $\pm$ 10%) to -17.7 ± 0.5 dBm (17.2 μW $\pm$ 10%).

TABLE II
PERFORMANCE SUMMARY

Parameter	AMI 0.5μm	UMC 0.18μm	
Nominal load	2μA, 1V (2μW)	4μA, 0.5V (2μW)	2.5μA, 0.4V (1μW)
No. of rectifier stages	3	2	2
Rectifier turn-on voltage (simulated)	1.12V	0.36V	0.29V
Power-up threshold (simulated)	61μW	8μW	5.2μW
Power-up threshold (measured)	62μW$\pm$10%	8.5μW$\pm$10%	6μW$\pm$10%
Overall system efficiency at threshold	3.2$\pm$0.3%	23.5$\pm$2.4%	16.7$\pm$1.7%
Theoretical free-space range (900MHz, 36dBm EIRP)	8m$\pm$5%	21.6m$\pm$5%	25.7m$\pm$5%

The test setup is shown in Fig. 16. An RF source was used to generate a sine tone at the frequency of interest. This was then amplified by an external amplifier and fed into the transmit antenna. The tag was located a distance r away from the transmitter; a Keithley source meter was used to monitor its output dc voltage and sink the load current to be delivered. The distance r was varied between 1 m and 3 m while taking the measurements. Since an anechoic chamber was unavailable, the path loss at each position of the tag was directly measured to estimate the received power level. An antenna with known gain and placed at the same positions as the tag was used for this purpose. We estimate the accuracy of this calibration procedure to be on the order of ± 0.5 dB ($\pm 10\%$) in received power level.

Fig. 17 shows the measured frequency response of the system for P_A varying between 7.6 $\pm$ 10% and 12.1 μW $\pm$ 10% for a load current $I_L = 4$ μA. Results are shown for MOD $= 0$ and MOD $= 0.5$ V, i.e., binary modulation states. The latter state mismatches the antenna to the rectifier and backscatters increased power to the reader. With a 2-μW load, he power-up threshold $P_{\rm th}$ is the minimum available power level (in the matched configuration, i.e., MOD $= 0$) at which the output voltage exceeds 0.5 V. From Fig. 17, $P_{\rm th} = 8.5$ μW $\pm 10\%$.[4]

[4]Practically, this condition should be true over a bandwidth of at least 25 MHz to provide enough tolerance for reliable operation in typical indoor environments, giving a more realistic $P_{\rm th} \approx 12.5$ μW.

If the load is reduced to 1 μW (2.5 μA at 0.4 V), we get $P_{\rm th} = 6$ μW $\pm$ 10%. Both measured $P_{\rm th}$ values agree well with predictions from theory (8 μW and 5.2 μW, respectively).

Fig. 18 shows measured load curves of the system for different values of P_A. The RF frequency was fixed at 970 MHz and the modulator input was MOD $= 0$. Load curves were obtained by varying the load current I_L drawn from the rectifier. Each curve corresponds to a certain value of rectifier output resistance $R_{\rm out}$. The value of $R_{\rm out}$ decreases as P_A increases because the switches in the rectifier become more strongly turned on. Decreasing P_A makes the no-load voltage smaller and $R_{\rm out}$ larger, which shifts the load curves downward and to the left. Similar frequency response and load curve data were also obtained for a tag using the 0.5-μm rectifier. System performance achieved in the two cases is summarized in Table II.

VII. CONCLUSION

We have developed a general theory for far-field RF power extraction systems. This theory has been used to design power extraction systems for UHF RFID applications. The systems use compact planar antennas, coupled resonator impedance matching networks and MOS rectifiers fabricated in standard 0.5- and 0.18-μm CMOS processes. The latter system has been found to have power-up thresholds of 6 μW (at 1 μW load) and

8.5 μW (at 2 μW load) while operating around 950 MHz. As far as we know, this is the best performance reported from a power extraction system built in *standard CMOS* to date. Major improvements in rectifier efficiency occur when advanced fabrication technologies are used. The availability of high-Q capacitors and transistors with lower gate resistance, threshold voltage and parasitic capacitances (i.e., higher f_T) reduces the power-up threshold, thereby extending the operating range of passive RFID systems.

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