Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise

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Abstract

A technique for characterizing the cyclically time varying statistical properties and spectrum of power supply noise using only two on-chip samplers is presented. The samplers utilize a voltage-controlled oscillator to perform high-resolution analog-to-digital conversion with minimal hardware. The measurement system is implemented in a 0.13μm process as part of a high-speed link transceiver. Measurement results showing the cyclostationary behavior of power supply noise are presented.

Keywords: power supply noise measurement, on-chip samplers, cyclostationary.

Introduction

As CMOS technology scales, the supply voltage drops and the chip current increases, causing the required supply grid impedance to scale as the square of the scaling factor. Achieving this low impedance across a wide range of frequencies has become increasingly challenging. CAD tools are using more and more sophisticated models of the distribution network in order to give chip designers the ability to find potential problems in simulation [1]. However, circuits to measure supply noise and validate these models have not been as fully developed.

In general, it is very difficult to measure a full time-domain supply waveform during the entire course of chip operation because either an extremely high speed analog interface or A/D converter would be required to avoid filtering or aliasing. Therefore, measurement circuits have been designed to observe specific properties of noise that can be extracted without high-speed interfaces or converters.

Muhtaroglu *et. al.* proposed a circuit that is effective in detecting overshoot and undershoot events over a window of time [2]. By performing repeated measurements at different threshold levels, this type of circuit provides information about the distribution of supply noise. Under controlled testing conditions, chips can be operated in a repetitive manner to facilitate the use of sub-sampling "on-chip oscilloscopes", such as those used by Takamiya *et. al.* to measure the supply voltage [3].

Unfortunately, sub-sampled waveforms measured in a repetitive mode may not capture supply noise behavior during normal chip operation. Samplers that do not rely on averaging for accuracy could be used to collect data about the distribution of the supply noise; however, the noise dynamics would remain uncharacterized. This is a limitation because both the distribution and frequency spectrum of the noise must be known in order to characterize the effect of supply noise on sensitive analog or mixed signal circuits.

We extend the previous measurement techniques by treating the supply noise as a random process, and use its statistical properties – in particular, its autocorrelation [4] – to measure the noise spectrum. Autocorrelation can be measured using only two samplers with precise sampling instants, but low sampling rates. We further extend this technique to measure the dynamics of a repetitively time-varying, or cyclostationary [5], noise process by recording the sampling instants in addition to the distance between the samples. This additional information allows one to find periodic structure in the noise, and better characterize its behavior.

In order to achieve the sub-mV level resolution necessary to collect supply noise statistics with relatively simple circuitry, we used a voltage-controlled oscillator (VCO) to perform A/D conversion on the noise samples. Results from a 0.13μm high-speed link transceiver chip on which the samplers were implemented characterize the measurement system's accuracy and present both deterministic and cyclostationary properties of supply noise.

Random Supply Noise and Autocorrelation

While supply noise may actually be deterministic in nature, the number of state variables that would need to be tracked to calculate it is enormous. Therefore, instead of finding the exact behavior, supply noise is usually modeled as a random process, and can be characterized by its autocorrelation or its frequency spectrum. This spectrum can be used to calculate the effects of the noise on sensitive circuits. In addition, the shape of the frequency spectrum can give insights into the source of the noise (e.g. clock buffer switching).

For a time-invariant (also known as stationary) process the autocorrelation (R) is defined as

$$R(\tau) = E[v_{noise}(t+\tau/2)\, v_{noise}(t-\tau/2)] \quad (1)$$

where τ represents the separation of the two noise samples in time and E[] returns the expected value of the random process. The Fourier transform of the autocorrelation gives the power spectral density (PSD) of the noise process. For example, the autocorrelation of an infinite bandwidth (white), zero mean process is an impulse whose magnitude is set by the variance (σ^2) of the noise process. Intuitively, if a noise process contains high frequency components, it will change within a short period of time, and therefore samples of the noise that are far apart in time will not be correlated with each other.

Thus far, the discussion of autocorrelation has been limited to stationary noise processes that do not vary with time. As the chip runs synchronously to one or more clocks and these clocks modulate the occurrence of noise events, it is unlikely that the properties of supply noise will be independent of time. Since this modulation is repetitive, at a particular point

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in time relative to the clock cycle, the properties of the noise should be the same. This is known as a cyclostationary process, and can be characterized by measuring the autocorrelation, and hence PSD, of the noise at each time point in the cycle. Restated in a different way, the autocorrelation R becomes a function of both the time separation τ, and the time t at which the samples were taken.

The most important characteristic of autocorrelation for the measurement system is that it is an average statistical property of the noise, and therefore we do not need to know its exact behavior at all times in order to extract its frequency content. The Nyquist frequency of the measurement is set by the minimum time spacing between the samplers, not by the repetition rate of the sampling, which greatly reduces the requirements on the throughput of the sampling circuits.

Measurement Circuits

A block diagram of the implemented noise measurement system is shown in Fig. 1. We used an external pulse generator to control the samplers' timing. This allows a high degree of flexibility in the range of time spacing between the samplers, the sampling rate, and the ability to lock the samplers to different noise cycles.

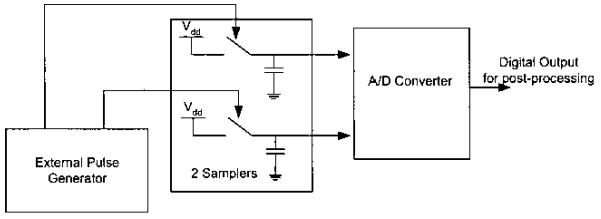

Fig. 1 Supply noise measurement system block diagram.

The sampling switch is the only circuit in the measurement system that must be on the die in order to measure supply noise relative to on-chip V_{ss}. It is also the only circuit whose bandwidth must be high enough to avoid filtering high frequency content. While previous designs such as [3] and [6] used NMOS switches, it is much easier to achieve the required bandwidth using PMOS switches when sampling V_{dd}.

In order to minimize coupling between V_{dd} and the sampled node during hold mode, the samplers operate off of their own, slightly higher than nominal supply (V_{ddQ}=1.3V instead of 1V). Since any noise on V_{ddQ} (either due to switching or uncoupled ground-bounce) will capacitively couple onto the sample node through the sampling switch parasitic capacitances, this supply is heavily bypassed to on-chip V_{ss}.

To avoid adding additional noise to the measurement system by communicating analog quantities off the chip, A/D conversion is performed internally. Since all the digital samples are post-processed using measured calibration curves, the linearity and offset requirements of this on-chip converter are not stringent. This allows us to use a simple and compact design so that it can be integrated onto many different parts of the die.

A. VCO Converter

Conversion is achieved by using the sampled voltage to set the frequency of a VCO, and then digitally estimating this frequency by counting the number of clock edges the oscillator outputs over a specified window of time, as shown in Fig 2. A simple toggle counter is used to minimize the hardware required for the converter.

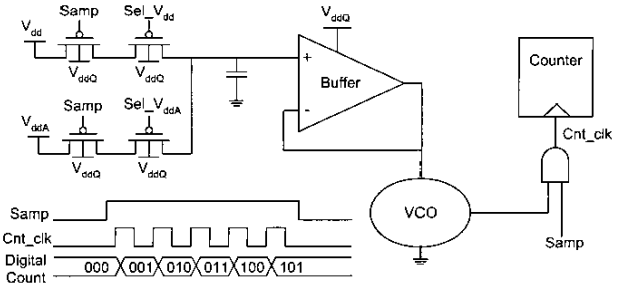

Fig. 2 VCO converter schematic and example waveforms.

Despite the fact that the oscillator is essentially free-running, the quantity that is being digitally measured is the average VCO frequency over the conversion window. Therefore, this scheme is insensitive to high frequency jitter (induced either by thermal noise or noise from V_{ddQ}) because the counting process averages out cycle-to-cycle variations in the oscillator's period.

Unlike high frequency jitter, the averaging does not attenuate noise that is on the same time scale as the counting window. Fortunately, for noise frequencies too low to be averaged by the counter, on and off-chip V_{ss} are very well correlated. Therefore, even if the on-chip bypass capacitance does not fully couple V_{ss} to V_{ddQ} at these frequencies, the external regulator and bypass capacitors will. Experimental results presented in the next section show that V_{ddQ} remains coupled to V_{ss} even at low frequencies.

The buffer and VCO were implemented with a regulator and pseudo-differential regulated supply CMOS buffers [7]. Since V_{ddQ} must be quiet for the system to perform accurate measurements, the supply rejection requirements of the regulator are not very stringent.

The resolution achieved by the VCO converter is set by the minimum change in sampled voltage necessary to get a difference of one count over the conversion window.

$$1\ \text{LSB} = 1/(T_{win}K_{vco}) \qquad (2)$$

where K_{vco} (in Hz/V) is the VCO gain, and T_{win} is the conversion window. The resolution of the converter is inversely proportional to the measurement time.

Since the phase of the oscillator is random with respect to the start of the counting window, the oscillator effectively adds a uniformly distributed noise term to the output of the converter whose magnitude is 1 LSB. This noise is helpful, because the effective resolution of the converter will increase as the measurements are externally averaged together.

In the VCO-based conversion scheme, the voltage to frequency gain of the oscillator may change with temperature. Depending upon the VCO implementation, temperature variations could cause offset or gains errors in the measurement. However, with additional circuitry such as a local thermometer (which could be implemented by another VCO converter sampling a relatively constant voltage), the temperature dependence of the oscillator could be measured during calibration and cancelled in post-processing.

Measurement Results

The proposed supply noise measurement circuits were implemented on a 0.13µm CMOS process along with 4 high-speed link cells and a central ASIC that controls and adapts the links [8,9]. The measurement circuits have the capability to measure both the digital logic supply (V_{dd}) and the supply dedicated to the analog blocks such as the PLL and phase interpolators (V_{ddA}). Along with the measurement circuits, noise generators were integrated to allow testing and validation of the measurement system.

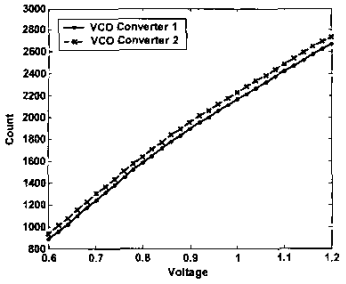

Fig. 3 VCO calibration curves with a 1µsec conversion window.

The measured VCO count versus voltage curves with a 1µsec conversion window for the two samplers are shown in Fig. 3. At a 1V supply, K_{vco} is roughly 2.6GHz/V, corresponding to a nominal LSB of 385µV.

A. Measurement System Validation and Characterization

Since noise on V_{ddQ} directly affects the sampled node, the main accuracy concern for this measurement system is the degree to which V_{ddQ} remains coupled to on-chip V_{ss}. In order to characterize this effect, we used the noise generators to inject square wave currents onto the supply grid while the rest of the chip was inactive.

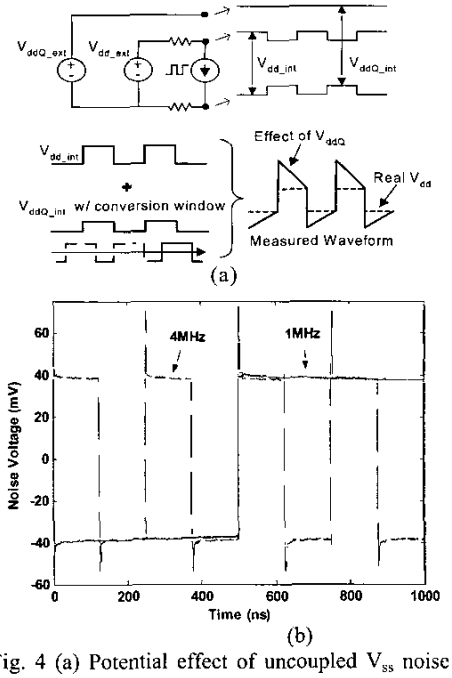

Fig. 4 (a) Potential effect of uncoupled V_{ss} noise through V_{ddQ} on measured waveform (b) Measured noise injected on V_{ddA} (mean subtracted) at 1MHz and 4MHz with a 500ns conversion window.

The injected current causes the chip's supplies to collapse. As Fig. 4(a) shows, if V_{ddQ} is not perfectly coupled to on-chip V_{ss}, it will effectively move in the same direction as V_{dd} because of the change in V_{ss}. Since the VCO integrates V_{ddQ} noise over the conversion window, if the conversion window is the same width as the injected pulse, uncoupled ground-bounce would cause the measured waveform to be somewhat triangular instead of square. The measured injected waveforms of Fig. 4(b) exhibit negligible differences in magnitude and shape between 4MHz and 1MHz with a 500ns conversion window. This shows that uncoupled ground-bounce on V_{ddQ} is minimal for this chip.

Despite the fact that these generated waveforms are deterministic, their spectrums can be characterized using autocorrelation to validate the measurement procedure. A 32MHz square wave was created on V_{dd} and the measured waveform and PSD are shown in Fig. 5. The PSD exhibits the odd harmonics associated with the square-wave waveform.

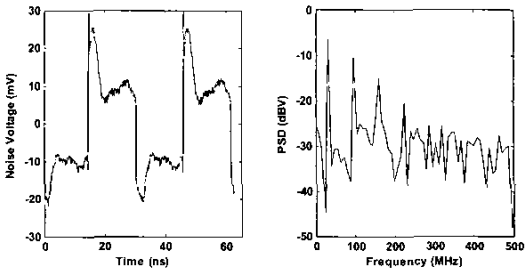

Fig. 5 Measured (a) waveform and (b) PSD of injected 32MHz square wave on V_{dd}. The PSD has been scaled by the Nyquist frequency (10GHz) to calculate the power and shown with the unit (dBV) instead of the usual (dB V^2/Hz). For PSDs in dBV, the average level in dB corresponds roughly to the noise σ.

Finally, to complete the characterization of the samplers, the noise floor of the system was measured in two different ways. First, using a single sampler with the chip powered down, 100k samples were taken and the voltage distribution around the mean was recorded – the measured σ was 800µV. Second, both samplers were used to measure the noise floor in the frequency domain. The measured noise floor of the PSD (overlaid in Fig. 7) was 300µV. The reduction from the single sampler is due to the averaging of the noise sources, which are uncorrelated between the two samplers.

B. Measured Supply Noise

With the characterization of the samplers complete, the chip was activated with the links running at 4Gb/s in serial loop-back on 2^{31} PRBS data. Before proceeding to measure autocorrelation, we used a single sampler to check if any deterministic, repetitive noise waveform could be measured on the supplies. In fact, such waveforms did exist and appeared as shown in Fig. 6.

As seen in Fig. 7, the most dominant source of noise appears at 200MHz. Since the clock frequency of the ASIC core is 200MHz, and the core has its own supply voltage but a shared V_{ss}, this noise is likely due to ground or substrate noise that is not fully decoupled to the supplies, which explains why the waveforms look very similar. An additional noise component exists at 400MHz, which is the reference clock for the PLLs in the links and drives some of the digital logic.

Finally, the noise also has some content at 4GHz, likely due to modulation of the tail currents in the differential pairs used in the transmitter, VCO, clock buffers, and phase interpolators.

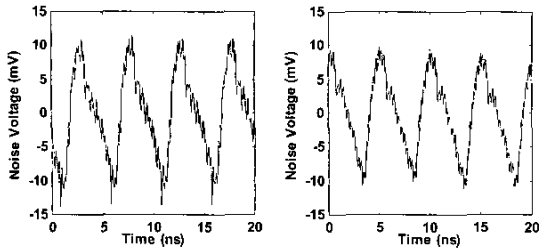

Fig. 6 Measured deterministic noise on (a) V_{dd} (b) V_{ddA}.

To characterize the dynamics of both the deterministic and random supply noise, we proceeded to measure the stationary, or average PSD with the chip operating under the same conditions (Fig. 7). The frequency components of the deterministic waveform mentioned above dominate the random noise, which in this view seems to be white in nature.

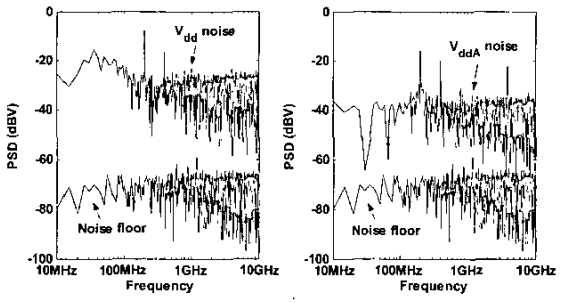

Fig. 7 Measured PSD with the noise floor for (a) V_{dd} (b) V_{ddA}

For circuits that do not operate at a particular periodicity, the stationary PSD gives a complete description of the supply noise. However, the random noise is actually cyclostationary in nature. In the stationary PSD of Fig. 7, the noise appears white because its time-varying behavior has been averaged by the measurement procedure.

For cyclostationary noise processes, both the distribution and the dynamics of the noise can vary with time. Measuring the PSD at every single time point takes an extremely large number of samples. Therefore, we measured the PSD of the random noise at two different times in order to observe examples of these types of changes. Additionally, in order to make the cyclostationary behavior more apparent, we decreased the operating frequency of the links by a factor of two. At this reduced rate, the majority of the logic should complete before the beginning of the next clock cycle, causing a period of relative calm on the supply.

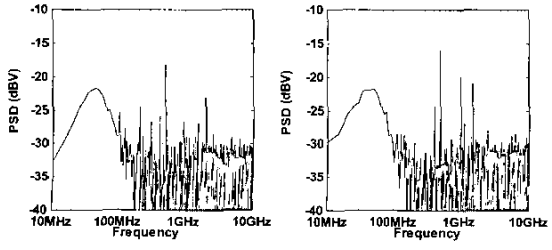

Fig. 8 Measured PSDs of V_{dd} noise at two different times in the noise period with the links operating at 2Gb/s.

Although the noise power in the PSD shown on the right of Fig. 8 is only slightly higher than that of the PSD on the left, their dynamics are clearly different - the PSD on the right has a strong component at 1GHz that is not present in the other PSD. Since a large portion of the transceiver runs off of a 1GHz clock at this data rate, these two PSDs correspond to times of relatively low and relatively high switching activity in the link circuits.

Conclusion

We have presented a measurement system for characterization of power supply noise using two low-rate samplers to measure autocorrelation. The system made use of a VCO-based A/D converter in order to achieve high-resolution measurements with relatively simple circuitry.

The system was used to measure supply noise on a high-speed link chip, and a deterministic signal of ~20mV peak-to-peak was detected on both the digital and analog supplies. In addition to this deterministic signal, the non-deterministic portion of the noise was shown to exhibit cyclostationary behavior, and example time-indexed spectrums showing the cyclically varying properties of this noise were presented.

In order to properly handle the effects of cyclostationary power supply noise, modeling techniques for synchronous analog and mixed-signal circuits will need to be extended. With the integration of these supply noise measurement systems, designers can begin to use real measured noise spectrums to characterize both the supply grid and the impact of supply noise on their circuits.

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