Analog Multi-Tone Signaling for High-Speed Backplane Electrical Links

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***Abstract*— Implementing a multi-tone (MT) architecture for high-speed backplane electrical links is difficult given the tight power and complexity constraints in this application. This paper proposes an approach that incorporates a baseband (BB) channel and a few passband (PB) channels. In this MT system inter-channel interference (ICI) and inter-symbol interference (ISI) are eliminated through fractionally spaced equalization at the transmitter and feedback equalization at the receiver. The design is modeled as a MIMO system, and optimal equalizer coefficients to minimize the transmit peak voltage are found by casting the optimization as a Second Order Conic (SOC) problem. In addition, for systems that need adaptation, we show how equalizer and power allocation coefficients can be obtained (sub optimally) using Zero Forcing (ZF) optimization. The effect of transmitter and receiver clock jitter are modeled in a way that can be included in both SOC and ZF optimizations, and the performance of this system is compared to more conventional baseband examples. It is shown that this AMT system can be built with complexity/power similar to a comparable performance baseband system, but has the ability to scale to higher bit rates.**

I. Introduction

While Discrete Multi-Tone (DMT) signaling is widely used today, implementation constraints prevent its application to high-speed backplane links. In these links data transfer rates can reach 6Gbps in commercial systems today, and power efficiency of <30mW/Gbps are required. As rates scale to >10Gbps, a 50cm Printed Circuit Board (PCB) trace becomes a challenging communication channel. Two sample channel responses are shown in Fig. 1.

There are two main issues with direct application of DMT to link systems. The first is the lack of a high-speed, high-resolution Analog to Digital Converters (ADC) with power consumptions within the link power budget. For instance, a 20Gsps 8-bit ADC consumes about 9W of power [1] while the total link budget is generally less than 1W. The second is that the hardware needed to perform FFT and IFFT over large block sizes is too large to implement in a link that might be repeated multiple times on a die. As a consequence uncoded 2PAM Baseband (BB) signaling with linear transmit equalization and receive Decision Feedback Equalization (DFE) is widely used in the industry [2][3] and 4PAM modulation has also been adopted [4][5] in some systems.

In this paper, we propose an alternative architecture for high-speed links which adds a few passband (PB) sub-channels to the BB channel and is therefore more efficient in channel bandwidth utilization. Since the number of sub-channels is very small, the cyclic prefix length should be kept to a minimum while the interference has to be cancelled. To achieve these contradictory goals, a more generalized channel shortening architecture using fractionally spaced linear equalizers at the transmitter and MIMO feedback equalization at the received is proposed.

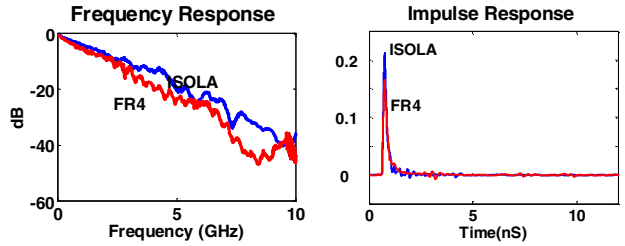

Fig. 1: Left: Frequency responses of sample channels. Right: Their impulse responses. The FR4 channel is the mid-plane 20" FR4 channel considered for IEEE 802.3 and the ISOLA channel is an improved channel with orthogonal line card connections.

In order to obtain the equalizer taps, the MT system can be modeled as a Multi-Input Multi-Output (MIMO) system where equalizers perform both equalization and power allocation at the same time. In Section III we will describe system modeling and show that the BER and peak voltage constraints can be cast as Second Order Conic (SOC) constraints [6], and therefore, optimal equalizer taps can be obtained through convex optimization. For systems that require an adaptive solution, we show that with appropriate definition of the cost function and some approximations, the equalizer tap design in zero-forcing sense can be decoupled from power allocation. As a consequence, equalizer taps (up to a scale factor) are obtained through conventional ZF techniques, and then joint power allocation is performed through simple matrix inversion.

Due to the high-speed nature of the circuits in link systems, performance can be significantly limited by noise sources other than thermal noise and interference. These other noise sources are created by system non-idealities like the uncertainty in the phase of the clocks. Therefore it is necessary that these noise sources are accurately modeled and included in system optimization. As part of our system formulation, in Section III we will include two of these noise sources, transmit

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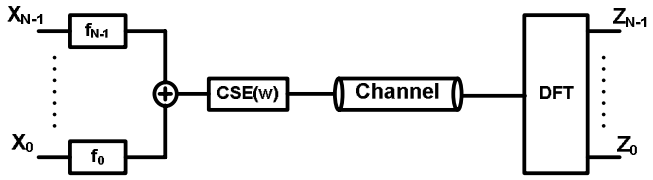

Fig. 2: General DMT architecture with channel shortening filter at the Tx.

and receive sampling jitter, and provide compact formulations that can be included in SOC or ZF optimization.

Section IV uses the models from Section III to compare 2-PAM and 4-PAM to our MT solution for the two channels shown in Fig. 1.

II. AMT System Architecture

Multi-tone (MT) systems exploit the orthogonality of a set of equally spaced sinusoids to achieve optimal power allocation in an efficient way. In its simplest form, one block of signals is constructed as follows:

$$Y(t) = x_0 + \sum_{n=1}^{N/2} \left[x_{2n-1} \cos(2\pi n f_0 t) + x_{2n} \sin(2\pi n f_0 t) \right] \quad (1)$$

where T (=1/f_0) is the symbol period, and x_n (n = 0, 1, …, N and x_N = 0) are the digital data sequence that belong to one transmission block. Since different tones may be delayed by different amounts when passed through the channel, symbol period T is generally extended to T(1+α) (α >0) so that all received tones that belong to the same block overlap for at least one symbol period. Such extension is called cyclic prefix in discrete implementations of MT. When the time span of the dispersion in the channel is large compared to symbol period, the penalty due to the cyclic prefix becomes significant, and therefore, channel shortening techniques are used as part of the MT architecture [7] [8] [9]. Fig. 2 shows a standard DMT system with a time-domain channel-shortening equalizer (CSE) at the transmitter. The CSE operates at the rate of Nf_0. In this figure, filters $\mathbf{f}_k$ represent transmit pulse shapes, which correspond to the columns of the cyclically extended Inverse Discrete Fourier Transform (IDFT) matrix:

$$F_{ext} = \begin{bmatrix} F_{N-v:N} \\ F \end{bmatrix}$$

where F is the IDFT matrix. As we explained earlier, a DMT system in this form is not feasible within a high-speed link power budget; however, a variation is possible.

To avoid the need for high-speed ADCs in the receiver, the DFT operation in the receiver may be performed using mixers and integrators as shown in Fig 3. However, in order to keep the overhead of RF front-end low, the number of sub-channels should be very small, which means sub-channel bandwidth would be in the order of a few GHz. Another consequence of very small number of sub-channels is that the CSE should nearly flatten the channel to keep the cyclic overhead low, which is contrary to the purpose of MT signaling. To get around this problem, the CSE is moved to the individual sub-channels and combined with the filters f_k in the transmitter, Fig. 3, such that each sub-channel has its own dedicated

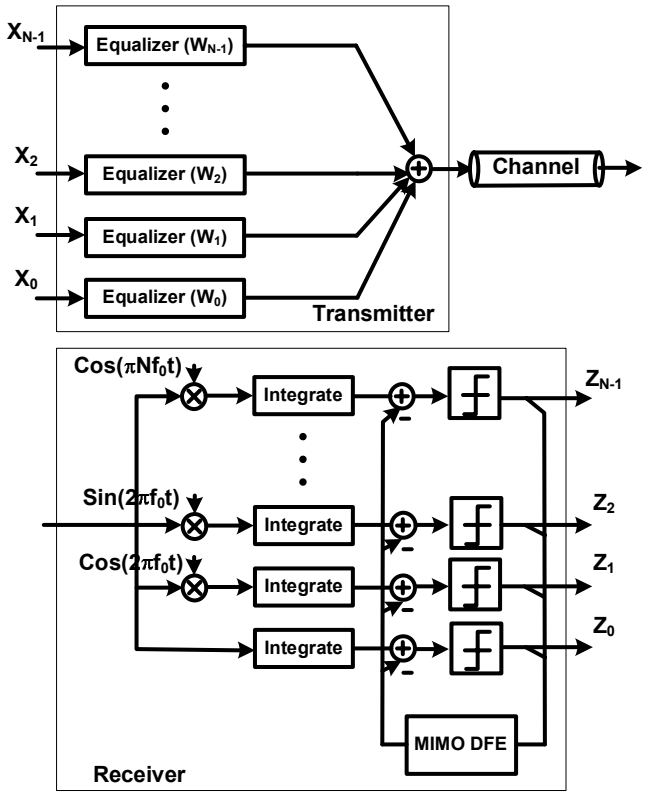

Fig. 3: Analog MT architecture with linear transmit equalization and MIMO DFE.

equalizer. This way the sub-channel equalizers, $\mathbf{w}_k$, are responsible for shaping the spectrum of their corresponding input signals such that they all arrive orthogonal at the receiver input. In addition a MIMO DFE (only the feedback part) is added at the receiver, Fig. 3, to facilitate the task of the FF equalizers. This way the FF equalizers would only need to maintain the orthogonality in the precursor part of the received signal. For small number of sub-channels (N = 4 or 6), this is an architecture that can be implemented with reasonable complexity.

Alternatively, the system in Fig. 3 may be regarded as a Filtered MT [13] system with dedicated full rate filters for the individual sub-channels and MIMO DFE to cancel any remaining interference. In this context, each equalizer, $\mathbf{w}_k$, has to shape its corresponding sub-channel's spectrum around its corresponding center frequency to cancel pre cursor ISI, and beyond that over the entire channel to cancel precursor ICI.

With this interpretation, since the highest frequency sub-channel is spread over the range of $Nf_0/2 \pm f_0/2$, it would not be equalized appropriately and may not be suitable for signal transmission at full rate. However, it can be used for other purposes like reducing the transmit peak voltage, transmitting clock, or other low rate side information.

If this sub-channel is not used in the system for data transmission, for fixed sub-channel symbol rate of f_0, a guard band (or equivalently cyclic prefix) of up to α=100/(N-2)% maybe inserted between the sub-channels if the frequency spacing between the carriers in the receiver is increased to

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$(1+\alpha)f_0$ and active integration period is reduced proportionally. The mixers would need to remain in synch with the integrators to retain the time-invariance nature of the system.

III. AMT System Formulation

Simplified block diagram of the system is shown in Fig. 4. In this figure $\mathbf{w}_0$, $\mathbf{w}_1$, …, $\mathbf{w}_{(N-1)}$ represent the linear equalizer taps in the transmitter, $\mathbf{p}$ is the channel pulse response, and $\mathbf{c}_0$, $\mathbf{c}_1$, …, $\mathbf{c}_{N-1}$ are filters matched to the sinusoids in Fig. 3. Let**:**

$$\mathbf{p}_k = \mathbf{p} * \mathbf{c}_k = \left[p_{k0} \;\; p_{k1} \cdots p_{kNv}\right]^T_{(Nv+1\times 1)}$$
$$\mathbf{w}_m = \left[w_{m_0} \;\; w_{m_1} \cdots w_{m(Nn_f-1)}\right]^T_{(Nnf\times 1)}$$
$$\mathbf{x}_m(n) = \left[x_m(n-n_f-v+1) \cdots x_m(n-1) \;\; x_m(n)\right]^T_{(nf+v\times 1)}$$
$$\mathbf{w}_{b_{km}} = \left[0 \; 0 \cdots 0 \;\; w_{b_{km0}} \;\; w_{b_{km1}} \;\; \cdots w_{b_{km(n_b-1)}} \;\; 0 \cdots 0\right]^T_{(N(nf+v)\times 1)}$$
$$k, m = 0,1,\ldots,N-1 \quad (2)$$

Where * is the convolution operator. In the above expressions $\mathbf{w}_{bkm}$ represents the feedback taps from the m[th] slicer output to the k[th] slicer input and the zeros in $\mathbf{w}_{b\_km}$ correspond to indices 0 to Δ+1 and $\Delta+n_b$+2 to $n_f+\nu$ assuming a delay of Δ for the system. Received signal at the k[th] slicer input may be described as:

$$\begin{aligned} z_k(n) &= \sum_{m=0}^{N-1} \mathbf{x}_m^T(n)\mathbf{P}_k \; \mathbf{w}_m - \sum_{m=0}^{N-1} \mathbf{x}_m^T(n)\mathbf{w}_{b_{km}} \\ &= \sum_{m=0}^{N-1} \mathbf{x}_m^T(n)\left[\mathbf{P}_k \quad -\mathbf{I}_{(n_f+v)\times(n_f+v)}\right]\begin{bmatrix}\mathbf{w}_m \\ \mathbf{w}_{b_{km}}\end{bmatrix} \end{aligned} \quad (3)$$

where $\mathbf{P}_k$ is the convolution matrix corresponding to $\mathbf{p}_k$. The above formulation is equivalent to removing the rows $\Delta+n_b$+2 to $n_f+\nu$ of the matrix $\mathbf{P}_k$ and eliminating feedback taps w_{b_km} from the formulation. We will define $\mathbf{Q}_k$ to be the resulting matrix after the elimination of the rows from $\mathbf{P}_k$ and use the following simple formulation in the remaining sections:

$$z_k(n) = \sum_{m=0}^{N-1} \mathbf{x}_m^T(n)\mathbf{Q}_k \mathbf{w}_m \quad (4)$$

A. Convex Formulation

For convex optimization we will assume that all gain factors in the transmitter are absorbed in the equalizer taps and input symbols $x_m(n)$ have unit average energy. With this assumption, the minimum distance between the constellation points at the receiver for the k[th] sub-channel is given by:

$$d_{\min_k} = \sqrt{\frac{12}{2^{2b_k}-1}}\, 1_\Delta^T \mathbf{Q}_k \mathbf{w}_k \quad (5)$$

Where b_k is the number of bits transmitted on the k[th] sub-channel. Interference power is also given by:

$$\sigma_{I_k}^2 = \sum_{m=0}^{N-1} \mathbf{w}_m^T \mathbf{Q}_k^T \mathbf{Q}_k \mathbf{w}_m - \left\| 1_\Delta^T \mathbf{Q}_k \mathbf{w}_k \right\|^2 \quad (6)$$

where $\mathbf{1}_\Delta$ is a column vector that is 1 at the Δ+1[th] position and is zero otherwise. Let $offset_k$ represent the minimum

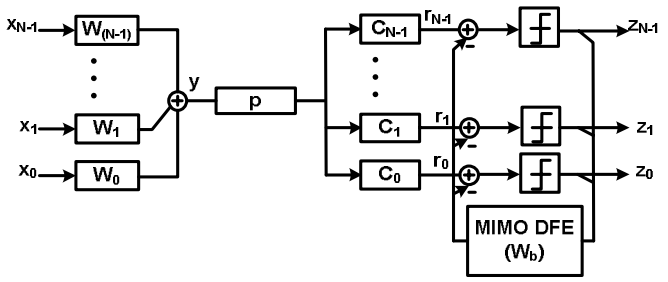

Fig. 4: Simplified system diagram

resolvable voltage swing by the k[th] slicer in the receiver and P_e represent the target BER at the receiver. Following the formulation in [10] the BER constraint can be expressed as:

$$2\left(1-2^{-b_k}\right)Q\left(\frac{0.5d_{\min_k} - offset_k}{\sigma_{noise}}\right) \le P_e \quad (7)$$

or equivalently:

$$\begin{aligned} &Q^{-1}\left(\frac{P_e}{2\left(1-2^{-b_k}\right)}\right)\sqrt{\sigma_{I_k}^2 + \sigma_{Thermal}^2} \\ &\qquad - \sqrt{\frac{3}{2^{2b_k}-1}}\, 1_\Delta^T \mathbf{Q}_k \mathbf{w}_k + offset_k < 0 \end{aligned} \quad (8)$$

For more accuracy the effect of residual ISI may be broken to a peak distortion part and a Gaussian part [10]; however, we skip that stage here for brevity. The peak voltage constraint at the transmitter at time $nT+(i/N)T$ can also be described as:

$$\begin{aligned} \sum_{m=0}^{N-1} x_m^T(n)\mathbf{w}_m^i &< \sum_{m=0}^{N-1} Max\left(x_m^T(n)\right)\left|\mathbf{w}_m^i\right| \\ &< \sum_{m=0}^{N-1} \sqrt{\frac{3\left(2^{b_m}-1\right)}{2^{b_m}+1}}\left|\mathbf{w}_m^i\right| = V_{Tx\_Max}^i \end{aligned} \quad (9)$$

where w^i_m is the i[th] poly-phase of w_m. Finally equalizer coefficients can be obtained through the following Second Order Conic optimization problem:

$$\begin{aligned} &Minimize \;\; V_{Peak} \\ &Subject\ to: \\ &BER_k < P_e \qquad for\ k = 1,2,\ldots,N \\ &V_{Tx\_Max}^i < V_{Peak} \qquad for\ i = 1,2,\ldots,N \end{aligned} \quad (10)$$

B. ZFE-DFE Solution

Even though the convex formulation of (10) provides the optimal equalizer taps, it cannot be easily employed in systems which require adaptation. Since most adaptive solutions are based on MMSE or ZF optimization, in this section we derive the ZFE-DFE solution for the system.

The important point to note is that in a system with transmit equalization, optimum received signal level is a variable and cannot be treated as a constant. Let's assume that the equalizer

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taps are set so that the gain of the main tap for the k^{th} sub-channel is given by g_k. The error in the k^{th} sub-channel is:

$$e_k(n) = z_k(n) - g_k x_k(n-\Delta) = \left(\sum_{m=0}^{N-1} \mathbf{x}_m^T(n)\mathbf{Q}_k\,\mathbf{w}_m\right) - g_k \mathbf{x}_k^T(n)1_\Delta \tag{11}$$

Defining the cost as the sum of the Mean Square Error (MSE) at all slicer inputs:

$$\sigma^2 = \sum_{k=0}^{N-1}\sigma_k^2 = \sum_{m=0}^{N-1}\left[\mathbf{w}_m^T\left(\sum_{k=0}^{N-1}\mathbf{Q}_k^T\mathbf{Q}_k\right)\mathbf{w}_m - 2g_m 1_\Delta^T\mathbf{Q}_m\mathbf{w}_m + g_m^2\right] \tag{12}$$

The term in the brackets in the above equation is basically the total interference caused by the m^{th} transmitter at all the receivers. Minimizing the above cost function, would therefore, lead to minimizing the total interference caused by the individual transmitters independent of the others:

$$\mathbf{w}_m = g_m\left(\sum_{k=0}^{N-1}\mathbf{Q}_k^T\mathbf{Q}_k\right)^{-1}\mathbf{Q}_m^T 1_\Delta \tag{13}$$

Using the sum of MSE as the cost function is an approximation, and therefore inferior to convex modeling, because it ignores the fact that different channels have different constellations and can tolerate different levels of interference. However, this approximation leads to a result that has an interesting practical implication: the equalizer taps for a given sub-channel can, up to a scale factor, be obtained independent of other sub-channels. Therefore, in a real system they can be adapted when all other sub-channels are turned off and the corresponding g_m is set to an arbitrary number (which leads to an open eye).

Now we would like to find the power allocation coefficients g_m in a joint manner for all the sub-channels. It is again possible to follow the procedure in the previous section and form an SOC problem in terms of g_m coefficients; however, a simpler solution is possible if we approximate the effect of residual interference as peak distortion. In other words, we make the assumption that since target BER is very small, the residual interference taps are very likely to add constructively and in the worst case reduce the eye-opening at the receiver by the sum of the absolute of all the taps. Peak distortion caused by interference at the k^{th} slicer input can be expressed as:

$$V_{ISI_k} = \sum_{m=0}^{N-1} g_m \beta_{km} \tag{14}$$

Where:

$$\beta_{km} = \sqrt{\frac{3\left(2^{b_m}-1\right)}{2^{b_m}+1}}\left\|\mathbf{Q}_k\left(\sum_{k=0}^{N-1}\mathbf{Q}_k^T\mathbf{Q}_k\right)^{-1}\mathbf{Q}_m^T 1_\Delta\right\|_1 \tag{15}$$

and is constant. The BER constraint of (7) therefore reduces to:

$$Q^{-1}\left(\frac{P_e}{2\left(1-2^{-b_k}\right)}\right)\sigma_{Thermal} + offset_k < \sqrt{\frac{3}{2^{2b_k}-1}}\,g_k 1_\Delta^T\mathbf{Q}_k\left(\sum_{m=0}^{N-1}\mathbf{Q}_m^T\mathbf{Q}_m\right)^{-1}\mathbf{Q}_k^T 1_\Delta - \sum_{m=0}^{N-1} g_m\beta_{km} \tag{16}$$

The peak voltage at time $nT+(i/N)T$ at the transmitter output can also be described as:

$$V_{Tx}^i = \sum_{m=0}^{N-1} g_m \alpha_m^i \tag{17}$$

Where α^i_m are also constant and can be obtained by inserting poly-phases of the taps in (13) into (9) (for g_m=1). Using these constraints, the SOC problem of (10) turns to a linear programming problem:

$$\begin{aligned} &Minimize\ V_{Peak} \\ &Subject\ to: \\ &\mathbf{Bg} > \mathbf{b} \\ &\mathbf{Ag} < V_{Peak}\mathbf{1} \end{aligned} \tag{18}$$

In the above problem **B** is an NxN matrix with entries $B_{mk} = -\beta_{km}$ if $k \neq m$ and $B_{mk} = \sqrt{\frac{3}{2^{2b_k}-1}} - \beta_{km}$ if k=m, A is an NxN matrix with entries $A_{km} = \alpha_{km}$, and b is a column vector whose entries b_k are equal to the left hand side of (16). By writing the Lagrangian for problem (18), it is easy to verify that the minimum V_{peak} (if it exists) is achieved when $\mathbf{Bg} = \mathbf{b}$ or equivalently $\mathbf{g} = \mathbf{B}^{-1}\mathbf{b}$. This means that with peak distortion approximation for interference, optimum power allocation is achieved when all the receivers meet the BER constraint with equality. Therefore, in a real system once the equalizer taps for all the sub-channels are adapted, the power allocation coefficients g_m can be obtained by measuring "eye closures" at the slicer inputs to form the B matrix followed by inverting the matrix.

C. Jitter

The uncertainty in the phase of the clock is one of the major performance limiting factors in high-speed links. The jitter in the transmitter clock can extend or shorten the transmit pulse duration at the output of the Digital to Analog Converter (DAC). Such edge modulation, when passed through the channel, would manifest itself as correlated noise at the sampling instant. On the other hand, the uncertainty in the receiver sampling clock would lead to sampling at sub-optimal points and therefore degrades the SNR. A through analysis of jitter for BB links was originally presented in [11]. In this section we extend that formulation to the case of MIMO systems and provide a more compact formulation.

1) TX jitter

As shown in [11] the effect of transmitter jitter can be modeled as Fig. 5(a). In this figure r_0, r_1 … r_{N-1} represent the noise samples at the slicer inputs and h is the impulse response

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of the channel. Intuitively, when a pulse at the output of the DAC (y) is extended, the extended portion of the pulse occupies the place of the following pulse. For small jitter variance, the net effect may be modeled as an impulse noise at the transition point with magnitude of $\phi(n)(y(n) - y(n-1))$. From noise modeling perspective, this is equivalent to a filter s = [1 -1] placed at the DAC output followed by a multiplicative noise $\phi(n)$. This time-varying multiplicative noise creates a linear time-varying (LTV) channel between the transmitters and the receivers. Following our notation in the earlier parts of this section, noise at the k^{th} slicer input can be described as:

$$r_k(n) = \sum_{m=0}^{N-1} \mathbf{h}_k * \left[\phi(n) \times (\mathbf{s} * \mathbf{w}_m * \mathbf{x}_m(n))\right] = \sum_{m=0}^{N-1} \mathbf{x}_m^T (\mathbf{H}_k \bullet \boldsymbol{\psi}) \mathbf{S} \mathbf{w}_m \quad (19)$$

where $\bullet$ is element by element matrix multiplication, $\mathbf{S}$ is the convolution matrix corresponding to s, h_k and H_k are similar to p_k and P_k in (2) and (3) but correspond to impulse response instead of the pulse response of the channel, and $\boldsymbol{\psi}$ is the jitter matrix whose elements can be described by $\boldsymbol{\psi}_{ij} = \phi(n - i + j)$. It can be shown that the jitter noise variance is:

$$\sigma^2_{TX\_jitter_k} = \sum_{m=0}^{N-1} \mathbf{w}_m^T \mathbf{S}^T (\mathbf{H}_k^T \mathbf{H}_k \bullet \mathbf{R}_\Phi) \mathbf{S} \mathbf{w}_m \quad (20)$$

where $\mathbf{R}_\Phi$ is the autocorrelation matrix of the jitter.

2) RX jitter

The difference between the signal at the optimum sampling point and the signal the actual sampled point may be considered as receiver jitter noise. The deviation from the optimum point is equal to the slope of the received waveform times the deviation to the first order. Approximating the slope with finite difference (d/dt) at a fine sampling resolution, the model of Fig. 5(b) can be obtained. Alternatively, the differentiator operator can be moved into the channel to convert the pulse response, **p**, to impulse response, **h**, convolved with **s** = [1 -1], Fig. 5(c) [11]. Again:

$$r_k(n) = \phi_k(n) \times \sum_{m=0}^{N-1} \mathbf{h}_k * \mathbf{s} * \mathbf{w}_m * \mathbf{x}_m(n) = \phi_k(n) \times \sum_{m=0}^{N-1} \mathbf{x}_m^T \mathbf{H}_k \mathbf{S} \mathbf{w}_m \quad (21)$$

and the jitter variance is:

$$\sigma^2_{RX\_jitter_k} = \sigma^2_{\phi_k} \left(\sum_{m=0}^{N-1} \mathbf{w}_m^T \mathbf{S}^T \mathbf{H}_k^T \mathbf{H}_k \mathbf{S} \mathbf{w}_m \right) \quad (22)$$

Clearly both (20) and (22) are convex in equalizer taps and can therefore be incorporated in the BER constraint (8) of the SOC formulation, or in the cost function (12) of the ZF optimization.

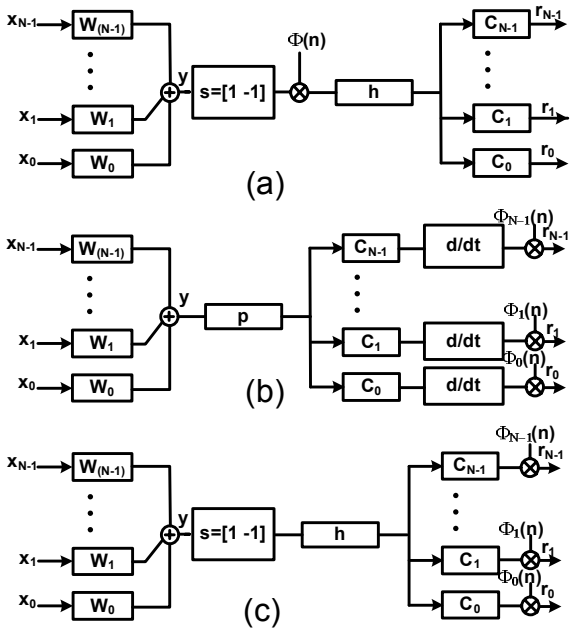

Fig. 5: (a) Transmitter jitter model. (b) Receiver jitter model (c) Alternative receiver jitter model.

IV. Simulation Results

Since we are interested in the performance of a limited power/complexity MT solution, in this section we create a number of different link architectures that all use comparable resources. One difficulty in doing this kind of comparison is that at a given target data rate different architectures operate at different symbol rates and consequently their circuits operates at different speeds. For example, at a target data rate of 10Gbps, the equalizers and the slicers in an AMT with a 4PAM BB sub-channel and a 4QAM PB sub-channel operate at 2.5GHz while same components operate at 10GHz and 5GHz in the corresponding 2PAM and 4PAM BB systems. In order to evaluate power/complexity of each system, we make the following assumptions:

1) Equalizer: We assume equalizer power consumption is proportional to symbol rate times number of equalizer taps. In addition we count multiplication by a two bit number as two summations, which means equalizer power is also proportional to the number of bits in the constellation. As a result we fix the number of FF and FB equalizer taps in all systems so that they have same complexity at any given target data rate. The absolute numbers were set as estimated complexity of future 2-PAM designs – for the FR4 channel the 2PAM BB system has 8 FF and 10 FB taps; for the ISOLA channel has 8FF and 16FB.

2) Slicer sensitivity: It is easy to show that in an interference dominated system, the required transmit peak voltage is linearly proportional to the slicer sensitivity. This is simply because both d_{min} and residual interference in (7) are linearly proportional to transmit peak voltage. Therefore, the choice of this parameter has a strong effect on the overall system performance. In reality as symbol rate goes down, better slicers can be designed, and therefore, slicer sensitivity is

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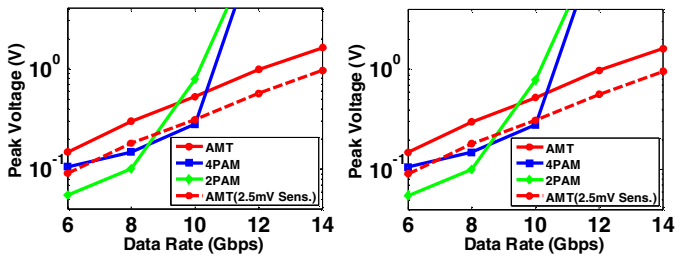

Fig. 6: Minimum required peak voltage over FR4 (a) and ISOLA (b) channels.

reduced; nonetheless, it is difficult to establish an accurate relationship. Therefore, in our analysis we will consider the case when same sensitivity of 5mV exists for all systems as well as the case when sensitivity is reduces to 2.5mV for AMT sub-channels.

3) First post cursor DFE taps: A major challenge in implementing DFE in links is the loop delay for canceling the first post cursor interference taps. Generally, the delay for resolving the received symbol and subtracting its effect from the following symbol exceeds the symbol-time, and therefore, speculative or partial DFE is used in most 2PAM systems [12]; however, since the complexity increases exponentially with the number of constellation points, this approach is generally not used for 4PAM systems. In order to maintain same equalizer complexity between 4PAM and AMT (which operates at half the symbol rate), we will assume that the first post cursor tap is left to be cancelled by the FF equalizer in 4PAM.

4) Since including jitter effect requires assumptions about its correlation properties which are very design dependent, we will ignore jitter in these simulations.

Using these assumptions yields the results shown in Fig. 6 for the minimum required transmitter peak voltage (in logarithmic scale) obtained through convex optimization for the two channels shown in Fig. 1. The AMT system has only one 4PAM BB sub-channel and one 4QAM PB sub-channel and 25% guard-band is assumed. The results indicate that it is possible to build an AMT system with comparable power/complexity as a normal baseband system. As expected, the optimal architecture depends on how close to the performance limit of the channel one needs to operate. For low data rates, the required output swing of the AMT signal is larger than the BB approach, and in fact the 2-PAM solution is optimal in this range. As the data rate increases, our simple AMT solution becomes more attractive, and ultimately can provide the highest data rate.

V. Conclusion

As the data rates of high-speed backplane links continue to increase, finding power efficient ways for signal transmission over dispersive channels become more important. While DMT has proved to be an optimal solution to this problem in many other applications, the power/complexity overhead needed to create the input A/D converter and the gigaops needed to perform FFT/IFFT to support 10-20Gbps rates are too large. We show that a simple AMT system using fractional linear transmit equalization and MIMO DFE can be built with roughly comparable complexity to a baseband solution. The equalization parameters for this system can be found by solving a Second Order Conic optimization problem. At equal power/complexity, the AMT solution provides a higher maximum bit rate than a baseband link, but has overheads when operating at lower bit rates. We are continuing to work on this design, both to create a more detailed implementation model to check our assumptions, and to further optimize the base architecture.

Acknowledgment

The authors would like to thank Ravi Kollipara of Rambus Inc. for providing the channel models.

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1-4244-0357-X/06/$20.00 ©2006 IEEE

This full text paper was peer reviewed at the direction of IEEE Communications Society subject matter experts for publication in the IEEE GLOBECOM 2006 proceedings.