Analog Multi-Tone Signaling for High-Speed Backplane Electrical Links

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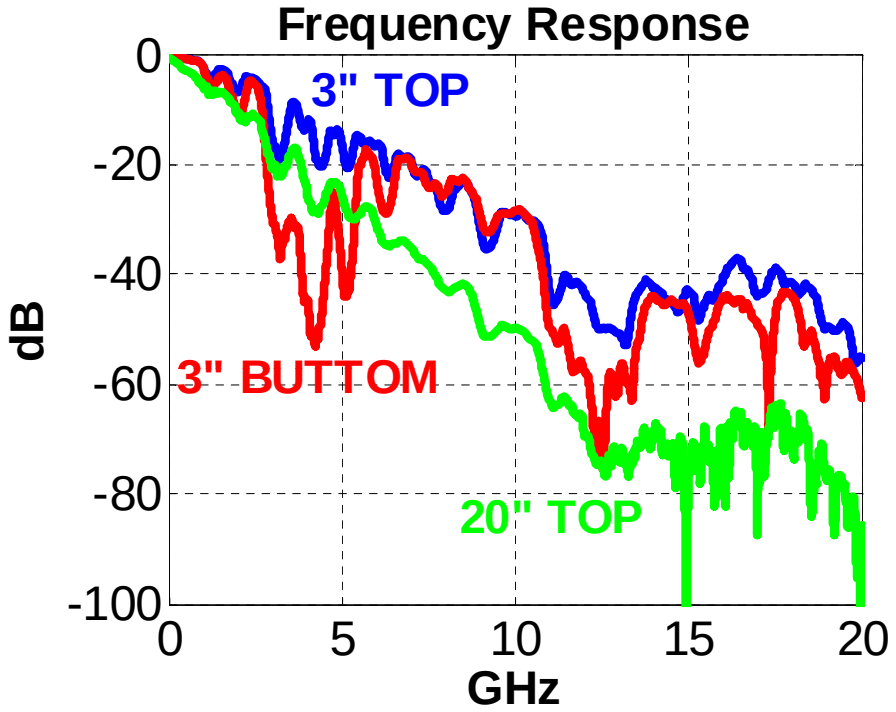
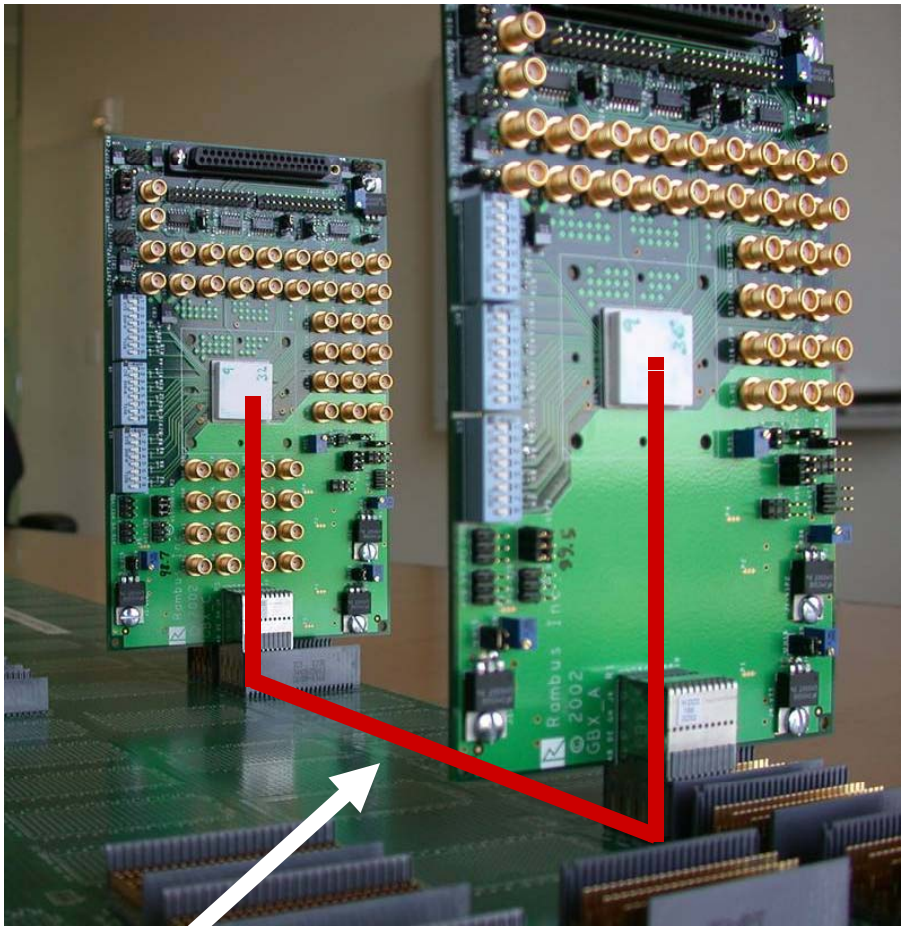
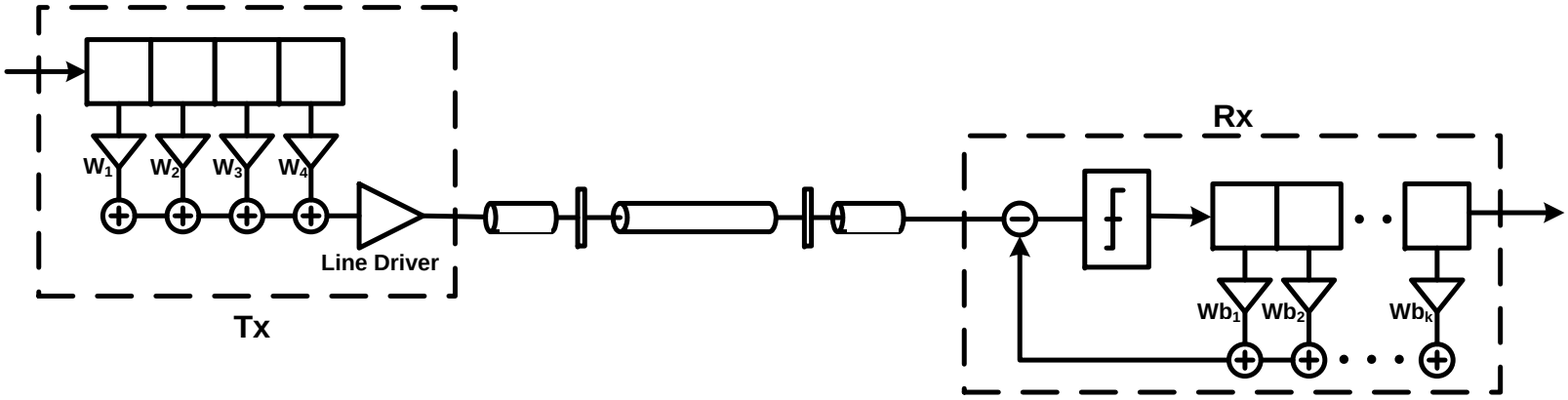
High-Speed Link





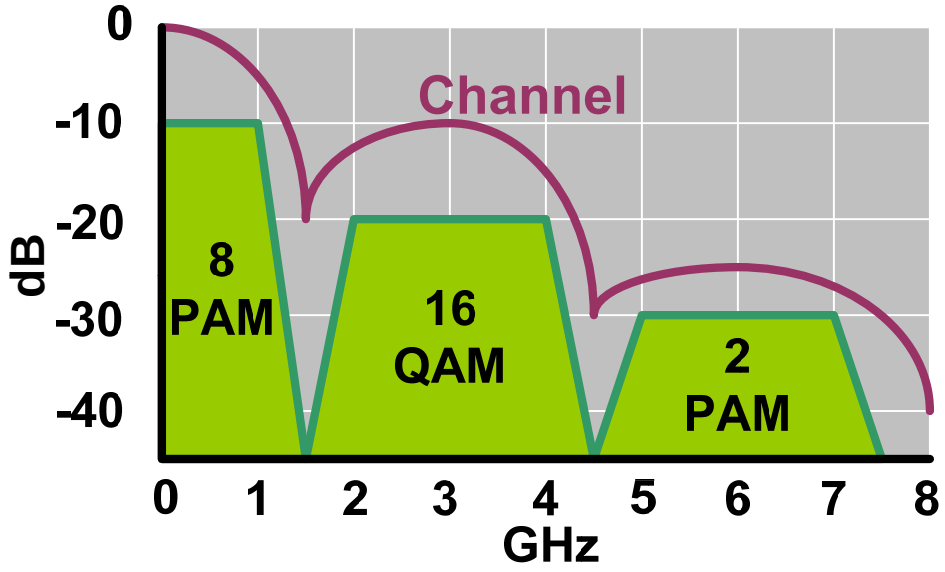
- **Multi Gb/sec chip-to-chip communication over PCB traces.**
  - **Routers, XAUI, PCI express**

State of the Art Links



- **Baseband 2PAM or 4PAM**
- **4-5 tap discrete linear transmit equalizer**
- **5-20 tap (predictive or partial response) DFE**
- **Designed for BER of 10^{-15}**
- **No error detection/correction coding**

Potential of Multi-Tone

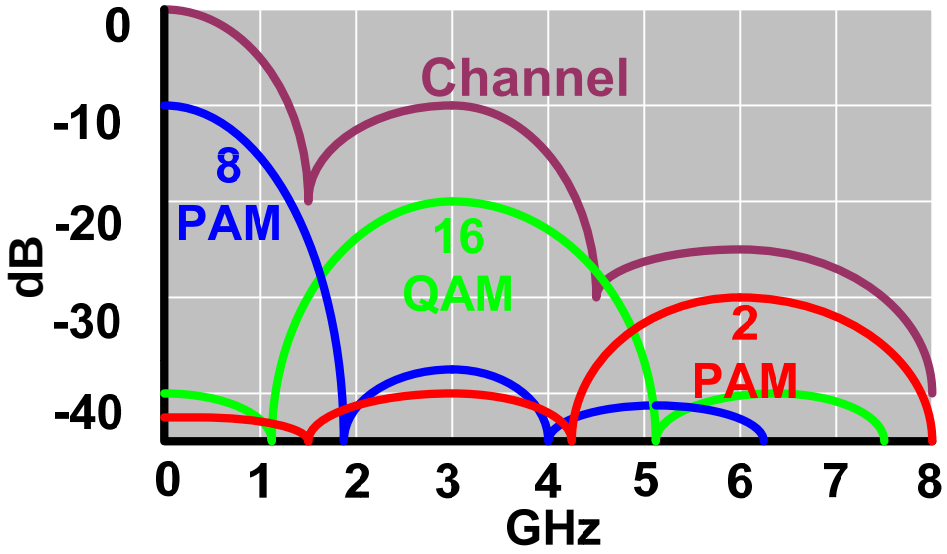


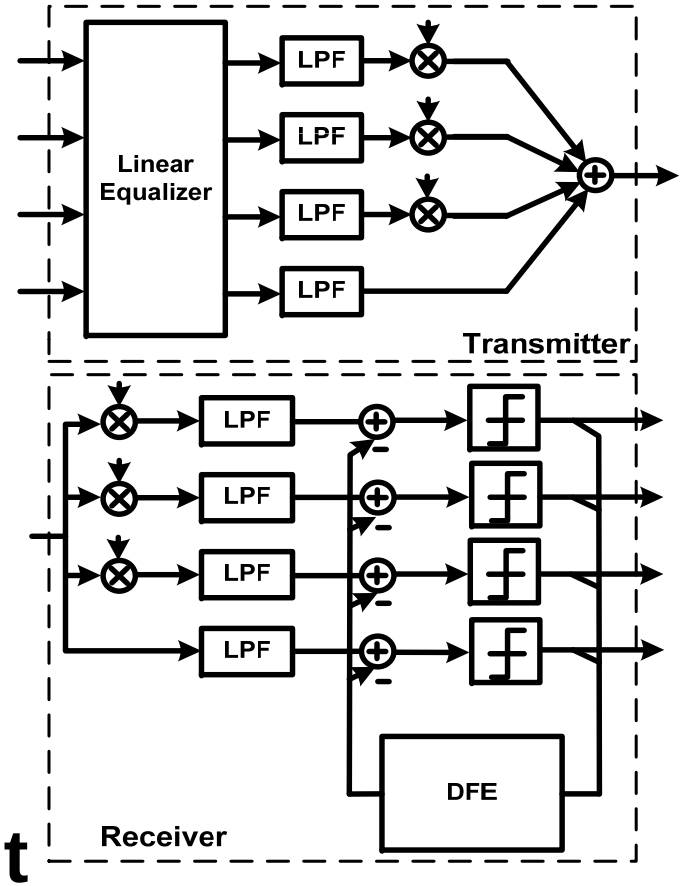
- **Better power allocation over channels with a notch**
- **Parallelized data stream in frequency leading to implementation advantages**

Design Considerations

- **Power efficiency is the main constraint**
  - **Cannot afford high-resolution ADC**
  - **Limits signal processing**
- **Rules out DMT techniques**
- **A customized MT architecture is required**
  - **Few sub-channels can create close to optimum transmit spectrum**

Analog Multi-Tone (AMT)

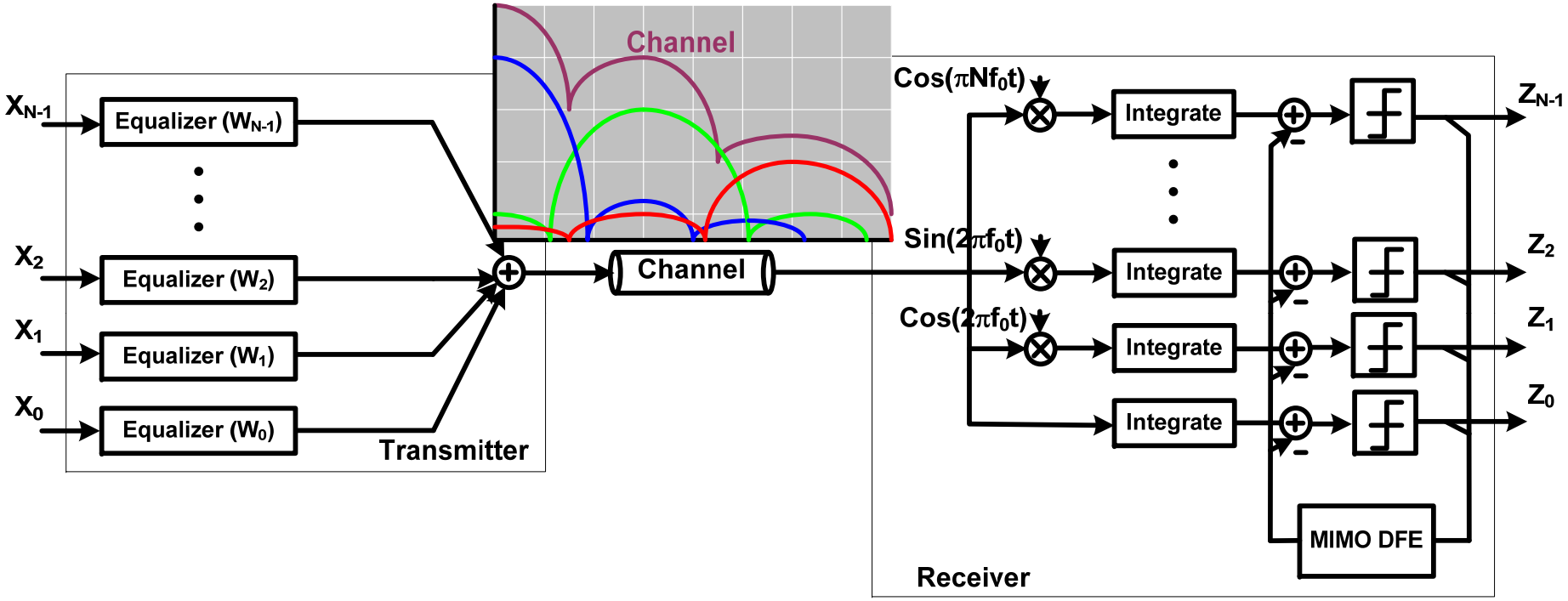




- A bank of parallel links on different carrier frequencies
- Sub-channels not independent
  - Inter-channel interference (ICI) exists

Conceptual

Practical Architecture



- N-times over-sampled equalizers per sub-channel
  - Tx power equal to a BB covering same BW
- Receive filters are integrators
- MIMO DFE in the receiver
  - DFE power equal to a BB covering same BW

Analysis Framework (Convex - SOCP)

- **Find Tx equalizer and Rx DFE taps that**
  - **Minimize transmit voltage (power)**
  - **Meet BER constraint per sub-channel**

$$2\left(1-2^{-b_k}\right)Q\left(\frac{0.5d_{\min_k}-offset_k}{\sigma_{noise}}\right)\le P_e$$

  - ***offset*$_k$: Receiver sampler dead-band (fixed)**
  - **d_{min}: Minimum distance at Rx (linear)**
  - **σ_{noise}: Sigma residual interf. and thermal (norm-2)**

SOCP: Minimize V_{Peak} $(Tx\,Peak\,Voltage)$

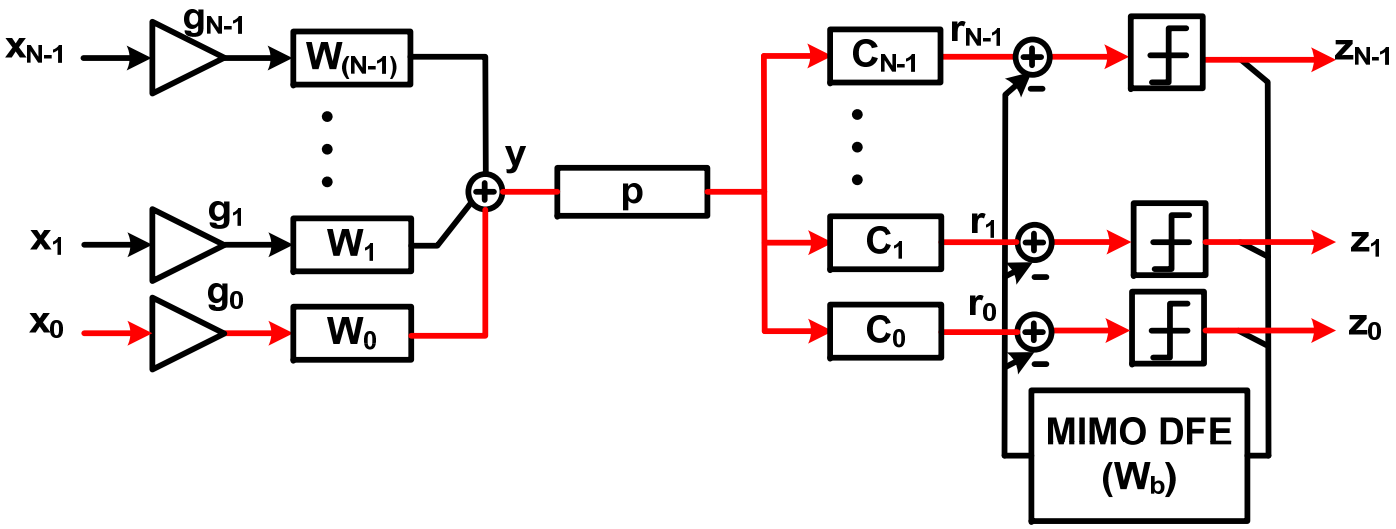
Subject to :

$BER_k < P_e \qquad for\, k = 1,2,...,N$

$V^i_{Tx\_Max} < V_{Peak} \qquad for\ i = 1,2,...,N$

ZFE with BER Constrained Power Allocation

- ***Step 1:*** **Independent sub-channel tap optimization (ZFE)**
  - **Minimize interference power from one transmitter to all receivers (find $W_{Tx,k}$ and $W_{FB,km}$)**
  - **Independent of sub-channel transmitter power**



ZFE with BER Constrained Power Allocation

- ***Step 2:*** **Joint power allocation (BER constrained)**
  - **Assume Tx voltage of g_k for each sub-channel**
  - **Model interference as peak distortion**
    - **BER constraint per sub-channel is linear in g_k**
- **SOCP reduces to an LP in vector** g

$$\text{Minimize } V_{Peak} \text{ (Tx Peak Voltage)}$$

$$\text{Subject to :}$$

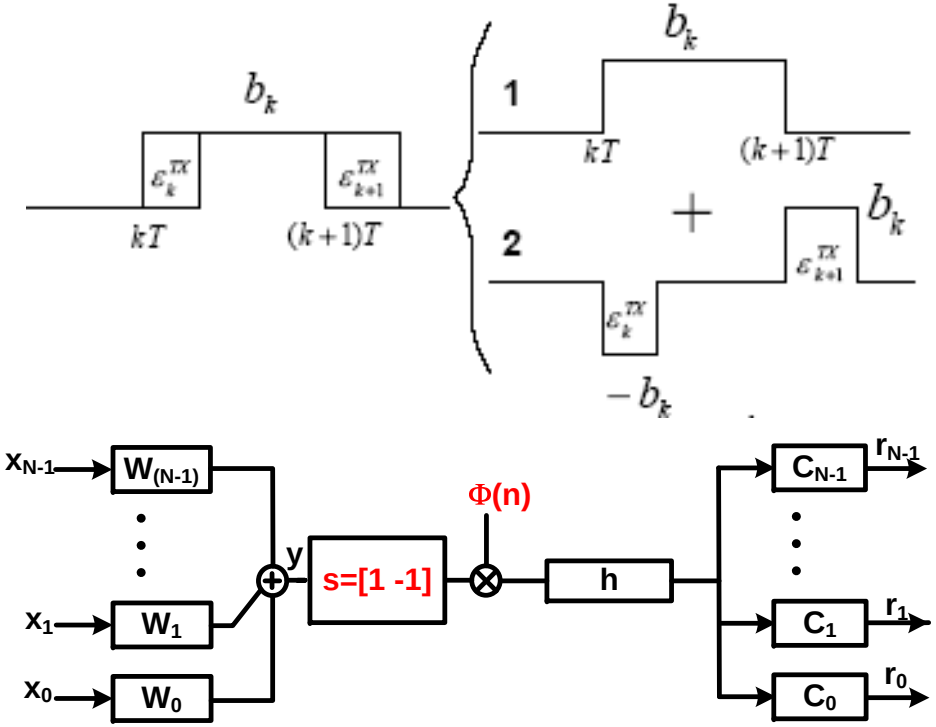
$$\mathbf{Bg} > \mathbf{b} \text{ (BER Const)}$$

$$\mathbf{Ag} < V_{Peak}\mathbf{1} \text{ (Peak Voltage Const)}$$

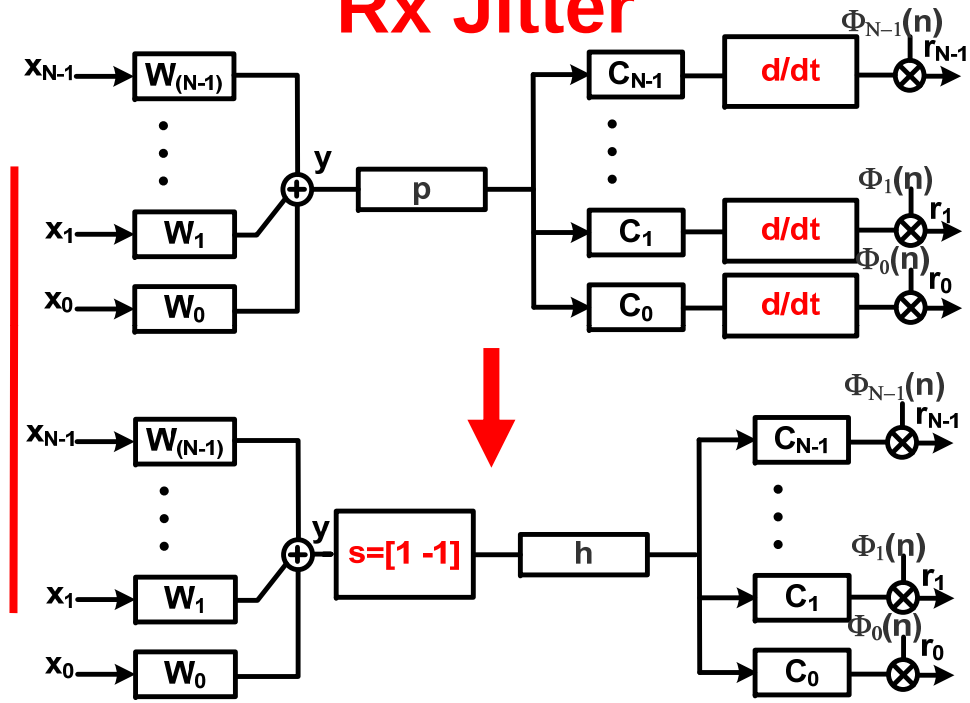
- **A,B fixed since taps are fixed**
- **Solution is $g = B^{-1}b$**

Closed From Jitter Modeling

Tx Jitter



Rx Jitter

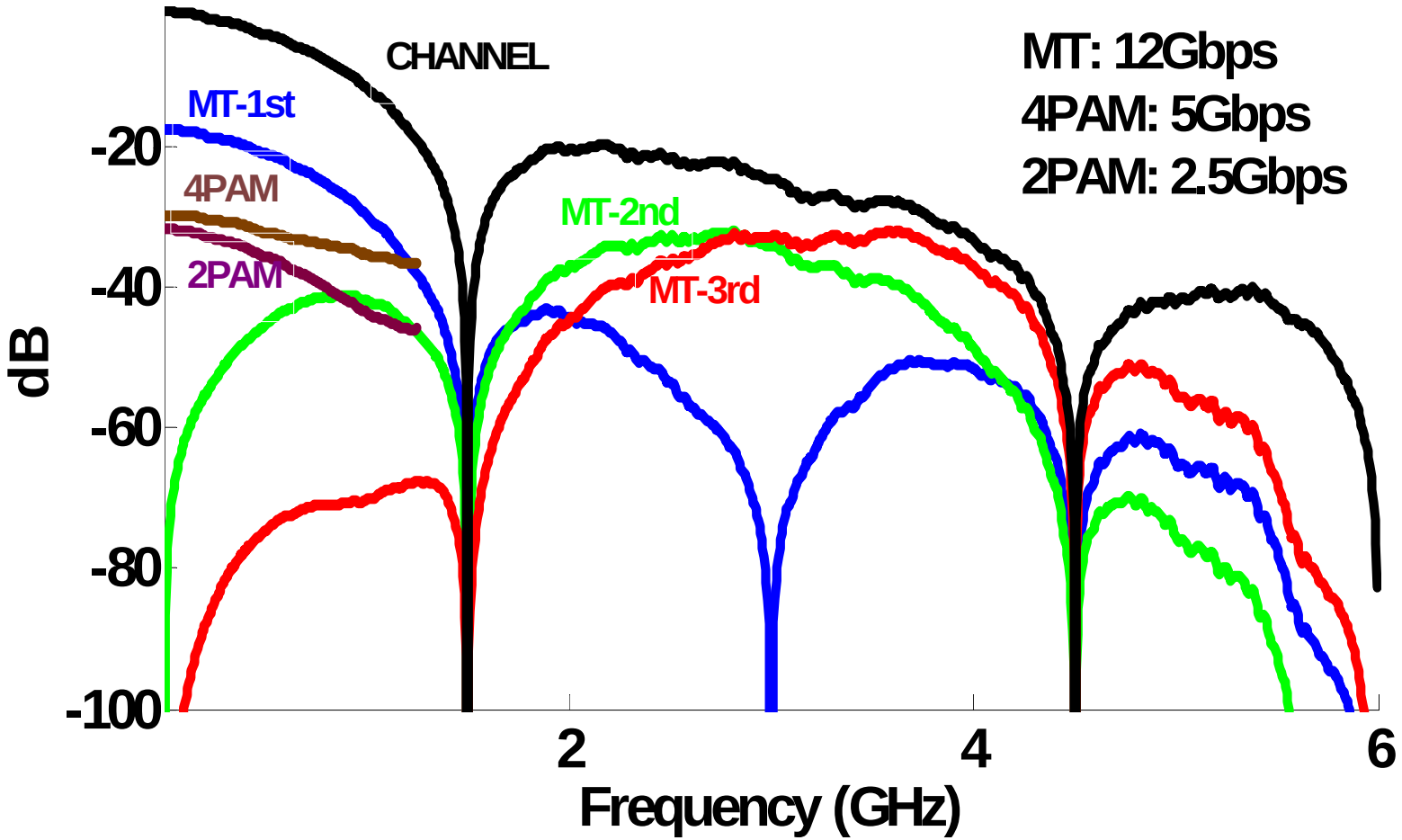


Variance at k^{th} Rx output

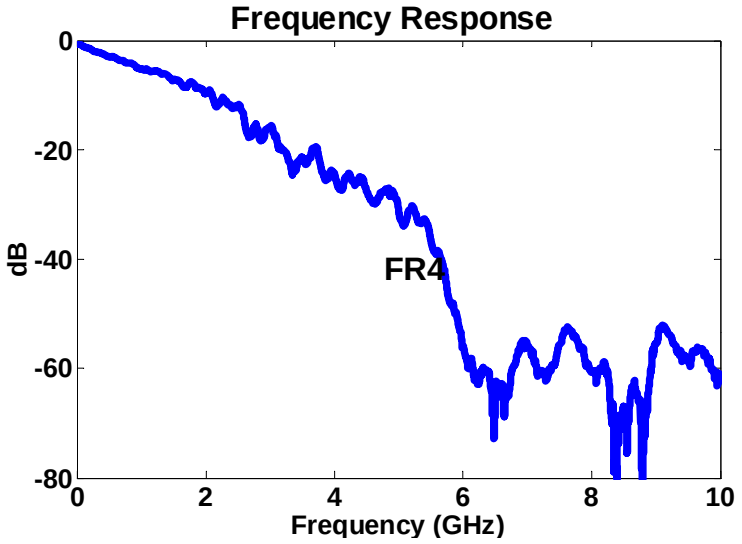
$$\sigma^2_{TX\_jitter_k} = \sum_{m=0}^{N-1} \mathbf{w}_m^T \mathbf{S}^T (\mathbf{H}_k^T \mathbf{H}_k \bullet \mathbf{R}_\Phi) \mathbf{S} \mathbf{w}_m \qquad \sigma^2_{RX\_jitter_k} = \sigma^2_{\phi_k} \left(\sum_{m=0}^{N-1} \mathbf{w}_m^T \mathbf{S}^T \mathbf{H}_k^T \mathbf{H}_k \mathbf{S} \mathbf{w}_m \right)$$

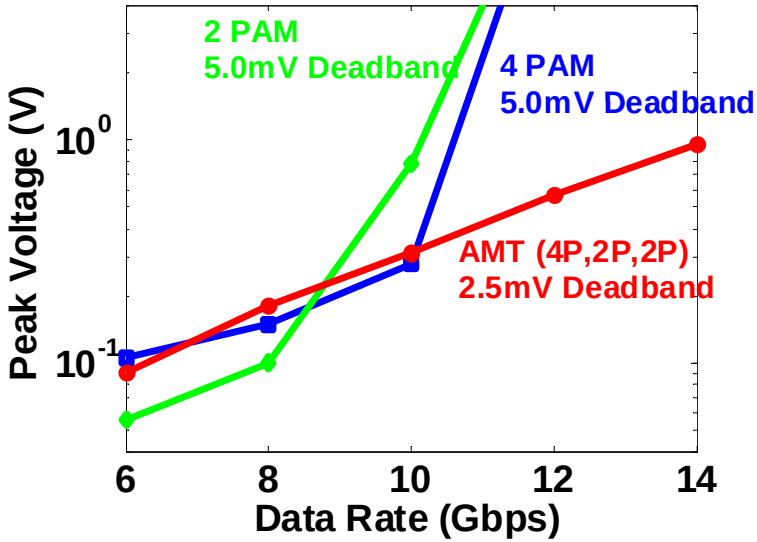
Performance on a Channel with Notch

Sub-channel Response at Rx Output



Performance on a Smooth Channel





- **Comparable hardware complexity**
- **For same V_{Peak} (transmit voltage)**
  - **AMT can achieve higher rates**
  - **Needs better Rx precision at lower rates**
    - **Possible since AMT samplers operate at half BB (4PAM) rate**

Conclusion

- **Power efficiency in links requires customized MT architectures**
- **The AMT architecture has comparable complexity with BB**
- **AMT has clear advantage over channels with a notch**
  - **Comparable performance over smooth channels**