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Practical Limits of Multi-Tone Signaling Over High-Speed Backplane Electrical Links

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***Abstract*— Application of Discrete Multi-tone (DMT) signaling to high-speed backplane interconnects requires major modifications to the well-known analysis methods applied to wireline communication systems. Tight power budgets in backplane links impose severe constraints on DMT block size and use of channel shortening filters in the system. Consequently, maximum throughput is achieved in a DMT system that is (residual) interference limited and water-filling is not applicable in its original form.**

In this paper, the DMT system is cast as a Second Order Conic (SOC) problem with peak transmit power as the constraint and optimum integer bit-loading and power allocation are achieved through a novel incremental integer bit-loading algorithm. The convex framework is subsequently used to find "practical" upper bounds on the performance of multi-tone signaling over high-speed links. The results indicate that DMT has the potential to achieve 15-23Gbps over typical backplane channels and system requirements in terms of FFT block size and prefix length are obtained.

I. Introduction

Backplane link refers to a communication system that connects two integrated circuits (IC) over a copper trace on a printed circuit board. Current systems use links running at 6.25 Gbps and at power-efficiencies of less than 30-40 mW/Gbps [2][3]. Due to these high signal transmission rates and tight power budgets, commercial links have mostly relied on simple 2PAM or 4PAM baseband (BB) signaling with modest linear equalization at the transmitter and Decision Feedback Equalization (DFE) at the receiver [4][5]. However, as demand for higher signaling rates continues, the super-linear growth of BB equalization complexity with signaling rate has initiated two trends in the link industry: improving the channels through costly manufacturing processes and improving system performance through more power-efficient signal processing.

A study in [2] showed about an order of magnitude difference between the capacity of current typical link channels and state of the art product links and proposed the gap may be closed by appropriately shaping the transmit spectrum through Multi-tone (MT) signaling. Even though MT signaling has been extensively studied for wired communication such as Digital Subscriber Line (DSL) systems, conclusions from those studies are not necessarily applicable to link environments due to the implementation constraints and the differences between link channels and the DSL channels. Fig. 1 shows two typical link channel responses that roughly sketch the best and worst scenarios.

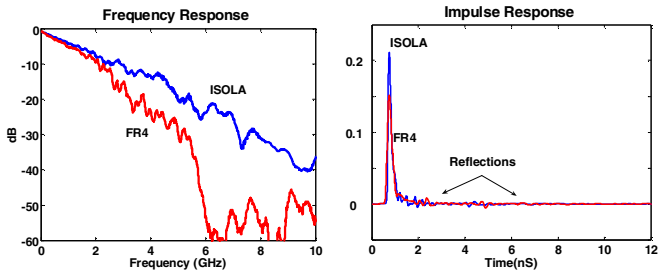


Fig. 1: Left: Frequency responses of sample channels. Right: Their impulse responses. Capacitive loading of 400 fF at the transmitter and at the receiver as well as package characteristics are modeled into the responses.

Due to the very high signaling rates and tight power budgets backplane links have a peculiar set of system constraints. For example, due to complexity issues, error correction coding is not yet employed in links and systems are designed for un-coded error rates of 10^{-15}. Consequently, clipping the transmit voltage as is done in DSL systems to reduce peak to average power ratio is not an option in any MT implementation. As another example, discrete linear signal processing is generally avoided in the receiver due to the difficulty (power and area cost) in designing multi GS/s high-resolution Analog to Digital Converters (ADC). In the transmitter, however, linear signal processing can be efficient as long as multipliers can be avoided. This is the case for example when linear transmit equalizers are used in BB links since the input to the filter is only 1 or 2 bits depending on the constellation size (2PAM or 4PAM). However, if the resolution of the input sequence increases, as would be the case if a channel shortening filter operates on the outputs of an IDFT block, the complexity would significantly increase. For example a back of envelope calculation shows that a simple 4-tap channel shortening filter consumes about two times the power of a 64-point IFFT[1]. Therefore, we will not consider a channel shortening filter for the system in our analysis. To make things even worse, IDFT block size itself cannot be made very large due to same complexity issues. We will consider block sizes of up to 64 in

[1] A 64-point IFFT implemented as 2 stages of radix-8 IFFT requires roughly 6x64 additions and 64 multiplications over 64 sample period. A 4-tap channel shortening filter requires 4 multiplications and 3 additions over 1 sample period.

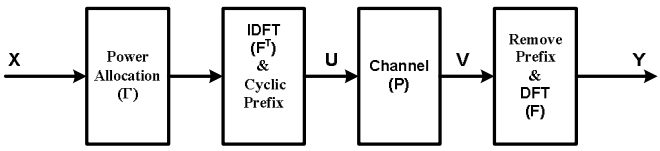


Fig. 2: Block Diagram of the DMT system

this paper. Finally, link systems are generally constrained by peak transmit voltage rather than average energy.

A consequence of having a small DMT block size and the absence of channel shortening filters is that the optimum throughput in the system is not necessarily achieved by completely orthogonalizing the channel. In other words, in the optimum configuration of DMT that maximizes throughput, the system would most likely be (residual) interference limited and water-filling is not applicable in its original form. Therefore, in order to get around this problem and to be able to model the peak voltage constraint correctly in the system, in this paper we pursue a different approach.

In Section II we describe the system in terms of linear equations and derive expressions for the total interference power, taking into account all residual inter-channel interference (ICI) and inter-block interference. These expressions will be used in the same section to cast the power allocation problem into a Second Order Conic (SOC) problem [6]. The SOC problem is convex in power allocation coefficients for given bit-loading. Then in Section III, we propose a novel incremental integer bit-loading algorithm that wraps around the SOC problem and quickly converges to an optimal sub-channel bit assignment.

Using the optimization framework, we plot the achievable data rates over channels of Fig. 1 with different DFT block sizes and cyclic prefix lengths in Section IV. Despite the fact that implementing a DFT of size 64 in the receiver of a backplane link may not be practical, the data from this section will provide a "practical" upper bound on the rates achievable over a backplane link using multi-tone signaling. In addition, the insight provided by the results of the analysis can help identify the key characteristics of a variant of a DMT system suitable for high-speed links. Such concluding remarks are presented in Section V.

II. Discrete Multi-tone System Formulation

In DMT systems, a cyclic prefix is added to the beginning of the transmitted signal to avoid interference between consecutive blocks of the transmitted signal and also to allow exploiting of the simple computational properties of the Fast Fourier Transform (FFT) and its inverse (IFFT). Fig. 2 shows a simplified block diagram of a DMT system. In mathematical terms, addition of the cyclic prefix makes channel's convolution matrix (P) circulant and consequently makes the columns of the DFT matrix (F) its eigenvectors. However, addition of the redundant prefix to the transmitted block incurs a penalty in the overall system throughput as well as the transmitted signal energy. Let:

$$P = \begin{bmatrix} p_0 & p_1 & \cdots & p_\nu & 0 & \cdots & 0 \\ 0 & p_0 & p_1 & & & & 0 \\ & & \cdots & & & & \\ 0 & \cdots & 0 & p_0 & p_1 & \cdots & p_\nu \end{bmatrix}_{N\times(N+\nu)} \quad (1)$$

represent the channel convolution matrix where N is DMT block size (DFT matrix F is NxN) and ν+1 is the length of channel dispersion (channel has ν+1 taps)[2]. Then, the received signal vector V at the receiver input can be expressed as a linear function of the transmitted vector U at the transmitter output:

$$V_{N\times 1} = PU_{(N+\nu)\times 1} \quad (2)$$

Since in this paper we focus on DMT block sizes of up to 64 and small prefix lengths (r), it is very likely that channel dispersion exceeds the DMT frame size (ν +1>N+l) , causing inter-block interference. DMT frame here is defined as a DMT block of size N plus the cyclic prefix. In order to correctly model all interference in the system, we rewrite equation (2) as follows:

$$V_{N\times 1} = P_{Post}U_{Post} + P_{Main}U_{Main} + P_{\mathrm{Pr}e}U_{\mathrm{Pr}e} \quad (3)$$

where

$$P = \begin{bmatrix} P_{Post_{Nxl}} & P_{Main_{Nx(N+r)}} & P_{\mathrm{Pr}e_{Nxs}} \end{bmatrix}$$
$$U^T = \begin{bmatrix} U^T_{Post_{Nxl}} & U^T_{Main_{Nx(N+r)}} & U^T_{\mathrm{Pr}e_{Nxs}} \end{bmatrix}$$

l and s are equal to the number of taps that cause interference from the following and preceding blocks respectively (ν = s+r+l). Without loss of generality and in order to simplify the notation we can assume that the channel is padded with enough zeros such that both s and l are equal to (r+N). If inter-block interference extends to multiple DMT frames, equation (3) can be easily generalized to have multiple $P_{Post}U_{post}$ and $P_{Pre}U_{pre}$ terms; however, we will skip this generality to keep equations simple. We further assume that the receiver locks to the portion of the channel response with the highest energy. The received vector V can be expressed as[3]:

$$V = P_{Post}F^T_{ext}\Gamma X_{Post} + P_{Main}F^T_{ext}\Gamma X_{Main} + P_{\mathrm{Pr}e}F^T_{ext}\Gamma X_{\mathrm{Pr}e} \quad (4)$$

[2] We are following the notation used in [7] in this paper, which assumes the format of $[x_n\ x_{n-1}\ \ldots\ x_1]$ for a vector X as opposed to the more customary format of $[x_1\ x_2\ \ldots\ x_n]$.

[3] Conjugate symmetry should be assumed for the input vector X so that transmitter output U is real. A conjugate symmetric vector still has N independent real variables and the vector of N real variable can be mapped to the conjugate symmetric vector X through a linear transformation. Therefore, for simplicity, in all the equations we assume that X represents the vector of the N real variables and the linear transform that maps X to a conjugate symmetric vector is absorbed into the IDFT matrix F^T.

where $F_{ext}^T = \begin{bmatrix} F^T \\ F_{,}^T(1:r) \end{bmatrix}$ is the IDFT matrix augmented with its first *r* rows to create the cyclic prefix, Γ is the diagonal N by N power allocation matrix, and X_{Post} and X_{Pre} are the following and preceding interfering blocks of symbols respectively.

Finally the received signal Y is given by:

$$\begin{aligned} Y_{N\times 1} &= FV \\ &= FP_{Post}F_{ext}^T\Gamma X_{Post} + FP_{Main}F_{ext}^T\Gamma X_{Main} + FP_{\Pr e}F_{ext}^T\Gamma X_{\Pr e} \end{aligned} \quad (5)$$

The first and third terms on the right hand side of the equation basically model interference from other transmitted signal blocks at the receiver.

The DMT system described above is bound by two types of constraints: per sub-channel BER constraint and transmit peak voltage constraint. Using equation (4), for a given bit-loading $b = [b_1 \quad b_2 \quad \cdots \quad b_N]$, we can express both constraints as convex inequalities as functions of the power allocation variables Γ_j.

The BER constraint for the k^{th} sub-channel is [7]:

$$2\left(1-2^{-b_k}\right)Q\left(\frac{d_{\min\_k}}{2\sigma_k}\right) < BER \quad (6)$$

Here d_{min_k} is the minimum distance between the constellation points at the signal y_k received at the k^{th} sub-channel, and σ_k is the standard deviation of noise at the receiver. Guassian distribution is assumed for the noise, which consists of thermal noise and (residual) interference. This approximation is justified since for reasonable performance (residual) ISI is caused by a large tail of reflection taps with small magnitudes. Equation (6) can equivalently be written as:

$$Q^{-1}\left(\frac{BER}{2\left(1-2^{-b_k}\right)}\right)\sigma_k - d_{\min\_k} < 0 \quad (7)$$

Using equation (5) we know that symbol x_k transmitted from the k^{th} sub-channel would appear at the receiver as:

$$Y_k = F_k P_{Main} F_{ext}^T \Gamma(x_k 1_k) \quad (8)$$

Where $\mathbf{1}_k$ is vector that is one at the k^{th} position and zero otherwise. $\mathbf{F_k}$ is the k^{th} row of the DFT matrix. Also assuming that energy (per dimension) (E_x) for all transmitted symbols is unity, the minimum distance between the constellation points of x_k is:

$$d_{\min\_k\_TX} = \sqrt{\frac{12}{2^{2b_k}-1}} \quad (9)$$

Consequently, the minimum distance between the constellation points at the receiver is:

$$\begin{aligned} d_{\min\_k} &= F_k P_{Main} F_{ext}^T \Gamma\left(\sqrt{\frac{12}{2^{2b_k}-1}} 1_k\right) \\ &= \left(\sqrt{\frac{12}{2^{2b_k}-1}}\Gamma_k\right) F_k P_{Main} F_{ext}^T 1_k \end{aligned} \quad (10)$$

which is a linear function of Γ_k. Furthermore using Equation (5) again:

$$\begin{aligned} \sigma_k^2 &= FP_{Post}F_{ext}^T\Gamma E_X \Gamma^T F_{ext} P_{Post}^T F^T \\ &\quad + FP_{\Pr e}F_{ext}^T\Gamma E_X \Gamma^T F_{ext} P_{\Pr e}^T F^T \\ &\quad + \sigma_{Thermal}^2 \end{aligned} \quad (11)$$

which is a quadratic function of power allocation coefficients Γ_j (j = 1,2,…,N). Therefore the BER constraint is a convex, or more precisely a Second Order Conic (SOC) inequality in Γ_j. The middle term in (5) does not contribute to (11) due to the cyclic prefix.

The transmitter peak voltage constraint exists because transmitter output has a maximum swing V_p, and consequently, all output samples should be less than or equal to V_p to keep the line driver circuit in intended operation region. Starting from the expression for transmitter output vector U, the peak voltage constraint can be derived as:

$$\begin{aligned} U &= F_{ext}^T \Gamma X_{Main} \le \left|F_{ext}^T\right| \Gamma Max(X_{Main}) \\ &= \left|F_{ext}^T\right| \Gamma Diag\left(\sqrt{\frac{3\left(2^{b_k}-1\right)}{2^{b_k}+1}}\right) 1 < V_p \end{aligned} \quad (12)$$

which is equivalent to a set of N independent linear inequalities in Γ_j and the single-ended swing V_p. $\left|F_{ext}^T\right|$ is the element-wise absolute of F_{ext}^T and **1** is a vector of all ones. The first inequality in (12) is based on the fact that maximum swing at the output is created when the signs of the (real) input symbols match the signs of the IDFT matrix coefficients, and the input symbols assume their maximum values. With the assumption of unit energy (per dimension) for transmit signals, $\max(x_k)$ is equal to:

$$Max(x_k) = \left(2^{b_k}-1\right)\frac{d_{\min\_k\_TX}}{2} = \sqrt{\frac{3\left(2^{b_k}-1\right)}{2^{b_k}+1}} \quad (13)$$

For large FFT sizes, the above formulation would be a little pessimistic, because the probability of getting a peak would go even below the target BER of 10^{-15}. A better approximation in such cases would be through clipping probability. The signal variance vector at the Transmitter output is given by:

$$\sigma_U^2 = \left|F_{ext}^T\right|^2 \Gamma^2 1 \tag{14}$$

where $\left|F_{ext}^T\right|^2$ is the element-wise norm-2 square of F_{ext}^T. In order to achieve certain clipping probability P_{clip}, we should have:

$$Q^{-1}\left(P_{Clip}\right)\sigma_U < V_P \tag{15}$$

Equation (15) is also an SOC constraint.

Finally, for a given sub-channel bit allocation, the optimal power allocation can be obtained through solving the following convex optimization problem [2][8]:

$$\begin{aligned} &Minimize\ V_P \\ &Subject\ to: \\ &Q^{-1}\left(\frac{BER}{2\left(1-2^{-b_k}\right)}\right)\sigma_k - d_{\min\_k} + eye_k < 0 \quad k = 1,2,...,N \\ &\left|F_{ext}^T\right|\Gamma Diag\left(\sqrt{\frac{3\left(2^{b_k}-1\right)}{2^{b_k}+1}}\right)1 < V_p \end{aligned} \tag{16}$$

where eye_k is the minimum resolvable signal level (or eye opening) or receiver sensitivity at the k^{th} sub-channel output. It is therefore a positive number by definition[4]. If V_P is set by implementation constraints, then the following feasibility problem can be solved instead.

$$\begin{aligned} &Is\ Feasible: \\ &Q^{-1}\left(\frac{BER}{2\left(1-2^{-b_k}\right)}\right)\sigma_k - d_{\min\_k} + eye_k < 0 \quad k = 1,2,...,N \\ &\left|F_{ext}^T\right|\Gamma Diag\left(\sqrt{\frac{3\left(2^{b_k}-1\right)}{2^{b_k}+1}}\right)1 < V_p \end{aligned} \tag{17}$$

The above SOC problems can be efficiently solved using conic solvers like Mosek[5]. The sub-channel bit loading, however, is in integer space, and therefore, obtaining the optimal bit-loading requires a little bit more work.

III. Incremental Bit-loading and Power Allocation

A well known integer bit-loading method for DMT systems is the Levin-Campello algorithm, which is based on greedy optimization [9]. Starting from an "efficient" bit-loading $b = \begin{bmatrix} b_1 & b_2 & \cdots & b_N \end{bmatrix}$, the bit-loading that leads to the least transmit power (peak voltage[6]) among all bit distributions with same total number of bits, the algorithm assigns the next incremental bit to the sub-channel that leads to the least increase in the overall transmit energy (peak voltage). This algorithm is therefore efficient when the increase in total transmit energy due to an incremental change in the bit distribution can be tabulated or obtained easily. In systems that are constrained by average transmit power, this is achieved through the well known gap approximation [7]. However, in a system driven by optimization (17), obtaining such data requires solving the convex optimization of (16) N times for all possible incremental bit-assignments to the sub-channels. This process can be very slow. Fortunately, the structure of the problem offers a faster alternative.

Looking at the feasibility problem (17) we can verify that the first term on the left side of the BER constraint and the peak voltage constraint are both relatively insensitive to weak functions of the bit-loading while the second term (d_{min}) is a strong function. Therefore, assuming the problem is feasible for a given eye-opening and certain bit-loading, power allocation and V_P, it is possible to trade a larger constellation size (smaller d_{min}) with eye-opening (higher slicer sensitivity) as long as the eye remains positive[7]. More exactly, in order to increase b_k to b_k+1 while satisfying the BER constraint, eye_k should be decreased by

$$\begin{aligned} &-\Delta d_{\min\_k}\left(b_k\right) \\ &\quad = \sqrt{3}\Gamma_k F_k P_{Main} F_{ext}^T 1_k \left(\frac{1}{\sqrt{2^{2b_k}-1}} - \frac{1}{\sqrt{2^{2b_k+2}-1}}\right) \end{aligned} \tag{18}$$

Therefore, we can conclude that at a given problem setting (given eye opening, power allocation and bit-loading), every $\frac{eye_k}{-\Delta d_{\min\_k}\left(b_k\right)}$ of the eye opening is worth a bit for the k^{th} sub-channel. Based on this heuristic, the incremental bit-loading algorithm can be expressed as follows:

- Step 1: Find a feasible bit-loading
- Step 2: Starting from a feasible point, maximize total incremental bit assignment for the system by solving the convex problem (19) and obtain the optimum set of eye-openings.

$$\begin{aligned} &Maximize\ \Delta b = \sum_k \Delta b_k = \sum_k \frac{eye_k}{-\Delta d_{\min\_k}\left(b_k\right)} \\ &Subject\ to: \\ &Q^{-1}\left(\frac{BER}{2\left(1-2^{-b_k}\right)}\right)\sigma_k - d_{\min\_k} + eye_k < 0 \quad k = 1,2,...,N \\ &\left|F_{ext}^T\right|\Gamma Diag\left(\sqrt{\frac{3\left(2^{b_k}-1\right)}{2^{b_k}+1}}\right)1 < V_p \end{aligned} \tag{19}$$

- Step 3: Sort the sub-channels based on their eye-opening. Start with the sub-channel with maximum eye-opening.
- Step 4: Assign one bit to the sub-channel.

[4] eye_k can be set to zero if infinite resolution is assumed for the decision devices at the receiver. The reason for the introduction of this new parameter will become clearer shortly as we discuss the bit-loading algorithm.

[5] www.mosek.com

[6] Any function that increases with adding a bit can be substituted here.

[7] We are treating eye_k as a variable here.

- Step 5: Run feasibility problem (17). If feasible, go to step 2. If not feasible, revert previous bit assignment, choose the next sub-channel with the largest eye-opening and go to step 4[8].

When the algorithm terminates no bits can be added to any of the sub-channels, and since throughout the algorithm, power allocation is performed to maximize incremental bit-assignment, the final bit-assignment would be very close to the optimal. Step 1 of the algorithm can be performed as follows:

Initialization Phase: Finding a starting feasible point:

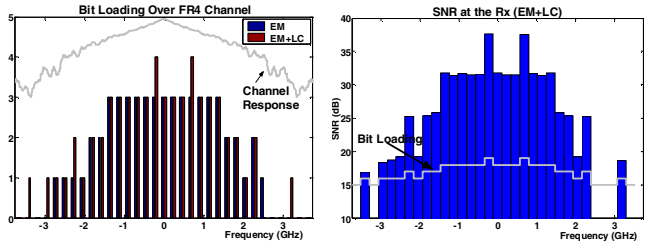
1. Assign one bit to all sub-channels.
2. Check for feasibility (17).
3. If feasible, done; otherwise, assign zero bits to the channel with the highest attenuation among active channels. Repeat step 2.

We will refer to this algorithm as Eye Maximization (EM) algorithm in the remaining of the paper. The algorithm may also be combined with the "efficentizing"[9] [9] phase of the LC algorithm to correct any deviations from the optimum bit-assignment. For example after one run of EM, the final bit-loading can be efficentized and then a new run of EM starting from the new feasible point leads to the global optimum. Our simulations show that about 5-10% improvement in overall data rate may be possible using the combined scheme at the expense of 5-10 times longer simulation time. The gains diminish with larger FFT block size.

To demonstrate the result of the bit-loading algorithm, Fig. 3 shows the bit-loading results obtained over the FR4 channel of Fig. 1 in one example setting where FFT size is set to 32, cyclic prefix is 8, and Nyquist frequency is 3.5GHz. The results are shown for the EM bit-loading as well as for the EM+LC. Bits from the left to the middle of the graph represent the Q rail and from middle to the right represent the I rail of the QAM constellations. The channel response is also imposed on the figure with an arbitrary scale. Signal to Noise Ratio (SNR) at the receiver output is also shown in Fig. 3. It can be seen that every extra bit is equivalent to about 6dB of SNR.

IV. Simulation Results

Fig. 4 shows the simulation results over the two sample channels of Fig. 1. For these simulations it was assumed that the transmitter voltage is constrained to 1.6V[10] peak-to-peak and a Noise Figure (NF) of 10 dB was assumed for the receiver. No other non-idealities were considered. For every



(a) (b)

Fig. 3: Bit-loading over FR4 channel for EM and EM+LC (a) and SNR at the receiver for EM+LC (b) for a DMT system with block size of 32, cyclic prefix length of 8, and sample rate of 7GHz. Peak to peak transmit voltage is 1.6V and Noise Figure is set to 10dB.

channel, the sample period (two times the Nyquist frequency of the system) was varied from 5.0 GHz to 17.5 GHz in steps of 2.5 GHz and for each setting the length of the cyclic prefix was varied from 8 to 20 in steps of 4. System was simulated for FFT sizes of 16, 32 and 64 and optimum sub-channel bit assignment and power allocation was obtained in each scenario using the EM algorithm. Fig. 4(a) shows the maximum achievable data rate that could be achieved over the channels as a function of (half) the DMT sample rate. For every point, the cyclic prefix length that maximized throughput was selected. Fig. 4(a) demonstrates a trade off between sampling rate and the length of the prefix. As sampling rate increases, system can exploit a larger portion of the channel; however, since there will be more interference taps, cyclic length increases as well. There is a point where the cyclic penalty cancels out the effect of the increased data rate and throughput starts to fall. Finally, it can be seen in the figure that, at least from theoretical stand point, data throughput of around 15 Gbps and 23 Gbps are achievable over FR4 and ISOLA respectively[11]. However, in order to achieve these data rates, FFT size should be 64 and prefix lengths of 12 and 16 over FR4 and ISOLA respectively are required. If we exclude the prefix penalty from rate calculations, we can observe that DMT with very large FFT sizes has the potential to achieve data rates in excess of 20 Gbps and 30 Gbps over FR4 and ISOLA respectively.

Fig. 4(b) shows the optimum bit-loadings used to achieve the maximum data rates. An interesting observation in both cases is that due to the gradual roll-off of the channel, number of bits assigned to the sub-channels varies very slowly as the sub-channels move away from DC. In fact it is possible to group every few of adjacent sub-channels to larger macro sub-channels which have same number of bits per symbol. This is done in Fig. 4(b) with solid red lines connecting the bars together. The new bit-loadings are still feasible and total throughput is about 6% less than the original configuration in both cases. What this observation suggests is that in order to achieve the water-filling gain of MT over link channels, only a few number of sub-channels is required. In other words, if it wasn't for the prefix penalty, the size of the DMT block could have been as small as 8.

[8] It would be more logical if in the 3rd step, channels are sorted based on the (real) valued incremental bits (Δb_k) that can be assigned to them by solving the following equation; however, simulation results don't show any difference in the final results.

$$\sqrt{3}\Gamma_k F_k P_{Main} F_{ext}^T 1_k \left(\frac{1}{\sqrt{2^{2b_k}-1}} - \frac{1}{\sqrt{2^{2b_k+2\Delta b_k}-1}} \right) = eye_k$$

[9] Efficentizing is a stage in the LC algorithm where starting from a given bit distribution, the bit distribution is obtained that with same total number of bits leads to the minimum total transmit energy (or voltage in our case).

[10] 1.6V is close to maximum achievable differential swing in a cascode driver in a 1V CMOS technology (90nm CMOS and bellow).

[11] These numbers include the cyclic prefix penalty.

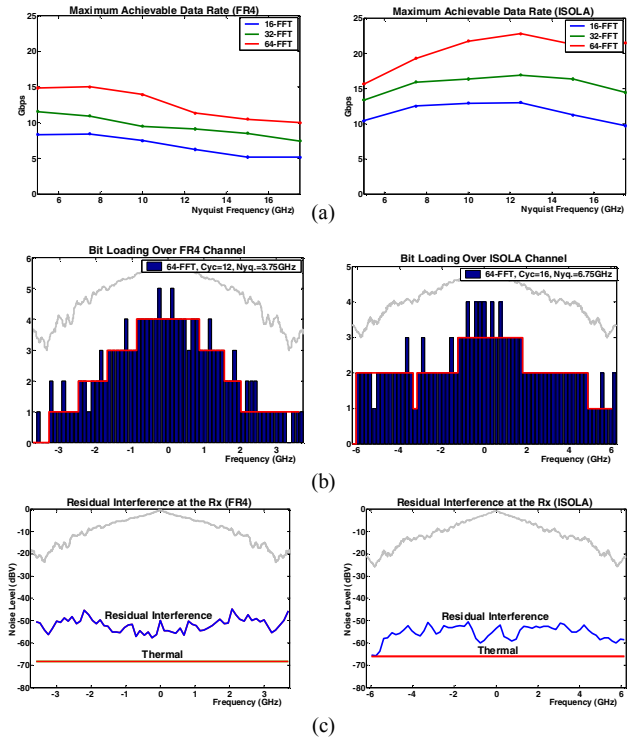


Fig. 4: Simulation results over FR4 (left) and ISOLA (right). Top: Maximum achievable bit rate (with optimum prefix length). Middle: Optimum bit-loading for the configuration which leads to highest data rate. Bottom: Residual interference at the Receiver. Peak to peak transmit voltage is 1.6V and Noise Figure is set to 10dB.

Fig. 4(c) shows the power of the residual interference at the receiver output for both channels. As it can be seen, even for FFT block size of 64 the system is completely (residual) interference dominated with interference power being about 15 dB above thermal noise in the case of FR4. This means that the system would clearly benefit from shortening of the reflection tail of the channel.

V. CONCLUSION

Accurate analysis of DMT over typical link channels indicates that theoretically MT has the potential for achieving data rates as high as 20-30 Gbps. DMT with medium block size and cyclic prefix in particular can achieve 15-23Gbps over the channels of Fig. 1.

It was shown that the characteristics of the link channels are such that close to optimum bit-loading can be achieved with very small number of sub-channels. However, in order to reduce the penalty due to the prefix overhead, DMT block size should be around 64, or significant channel shortening is required.

We note that the essence of MT is its efficiency in shaping the transmit spectrum, and cyclic prefix is just a clever way to simplify the implementation. Therefore, if we were to think outside the framework of Discrete Multi-tone and draw insight from our analysis in this paper, we would conclude that a MT architecture is most efficient for backplane links in which dispersion is dealt with independent of the number of tones. One such architecture is described in [10].

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