A 24Gb/s Software Programmable Multi-Channel Transmitter

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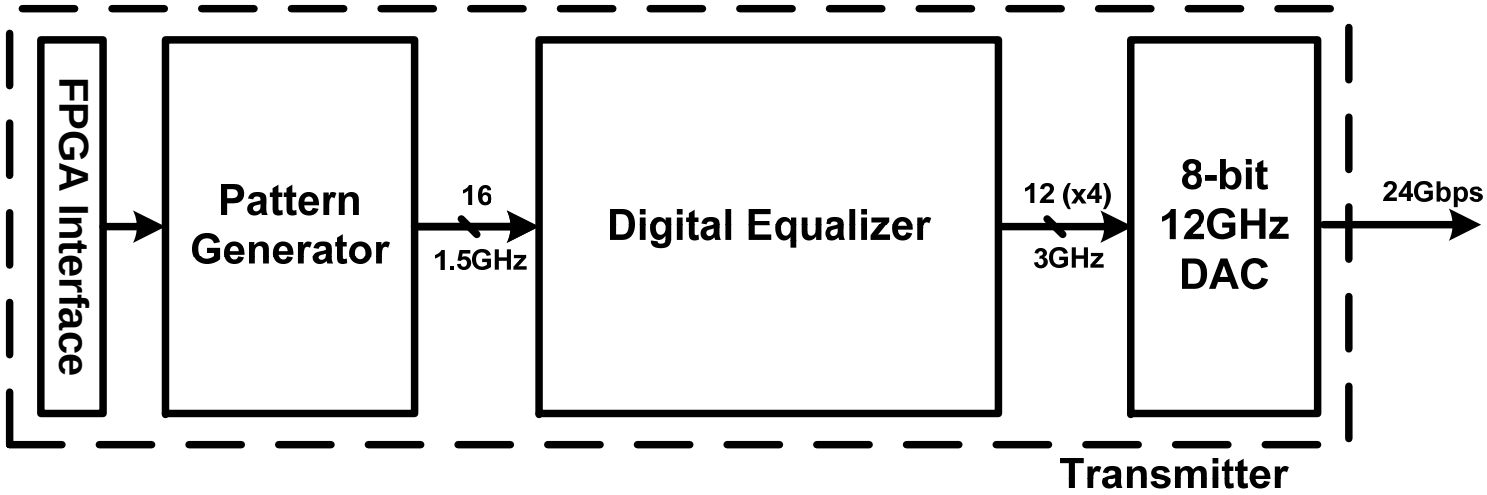
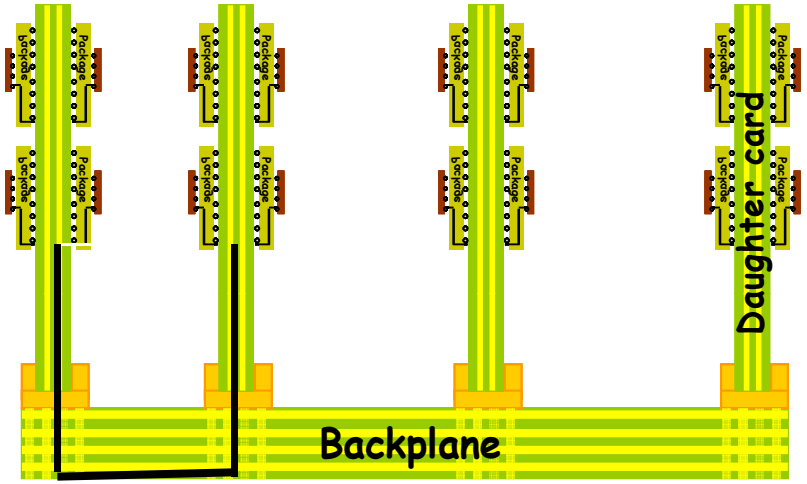
24Gb/s Transmitter

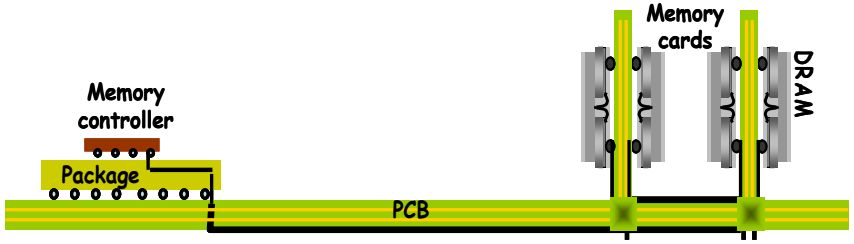


- A test instrument for verifying different transmission algorithms
- Multiple operation modes
  - 2-channel or 4-chanennel Analog Multi-Tone (AMT)
  - 2PAM, 4PAM, 8PAM, … baseband
  - Software programmable

High-Speed Electrical Links



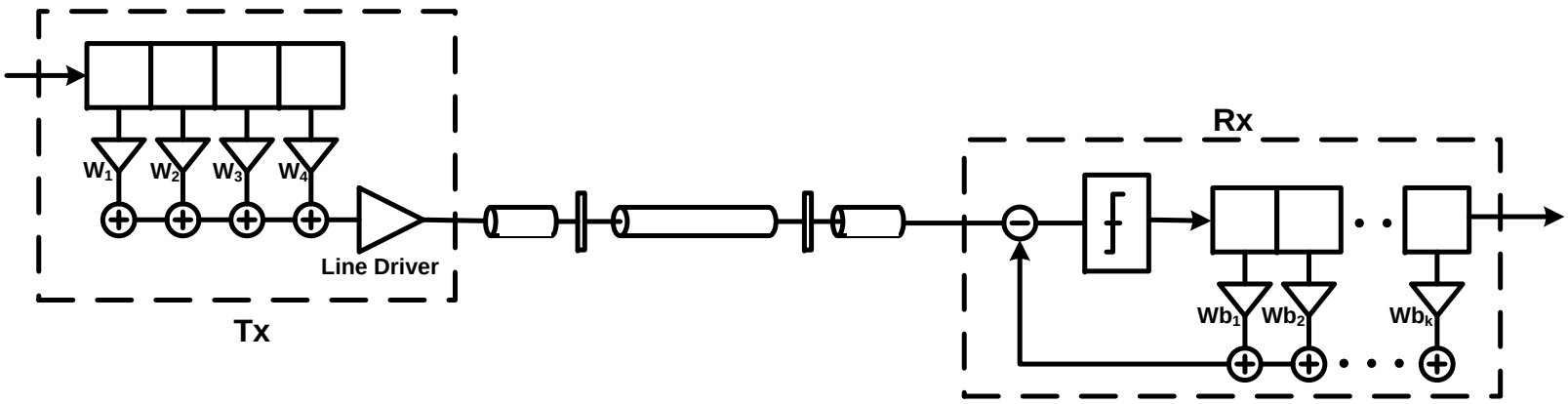
Network Routers



CPU/Controller to DRAM

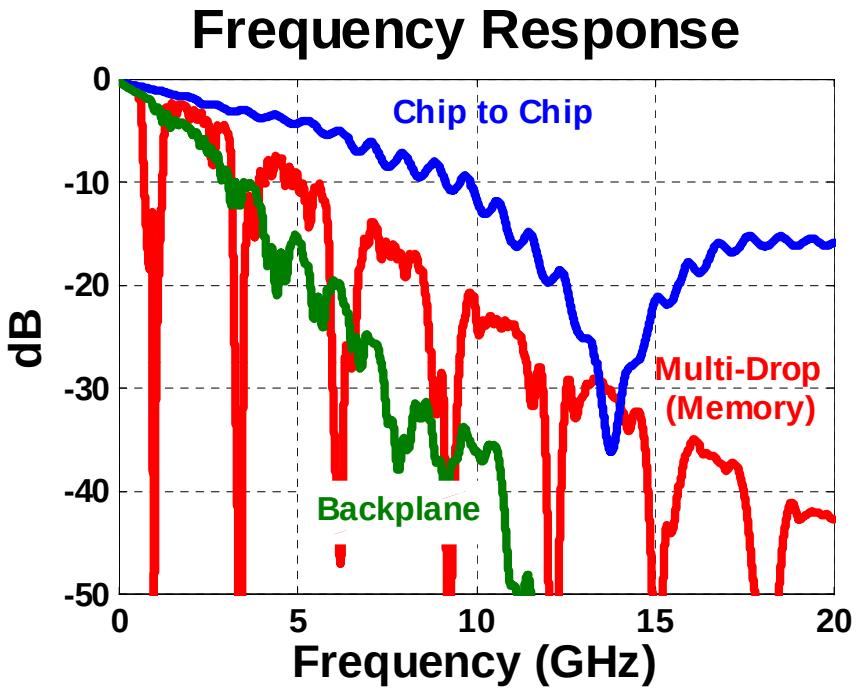
CPU to GPU

State of the Art Links



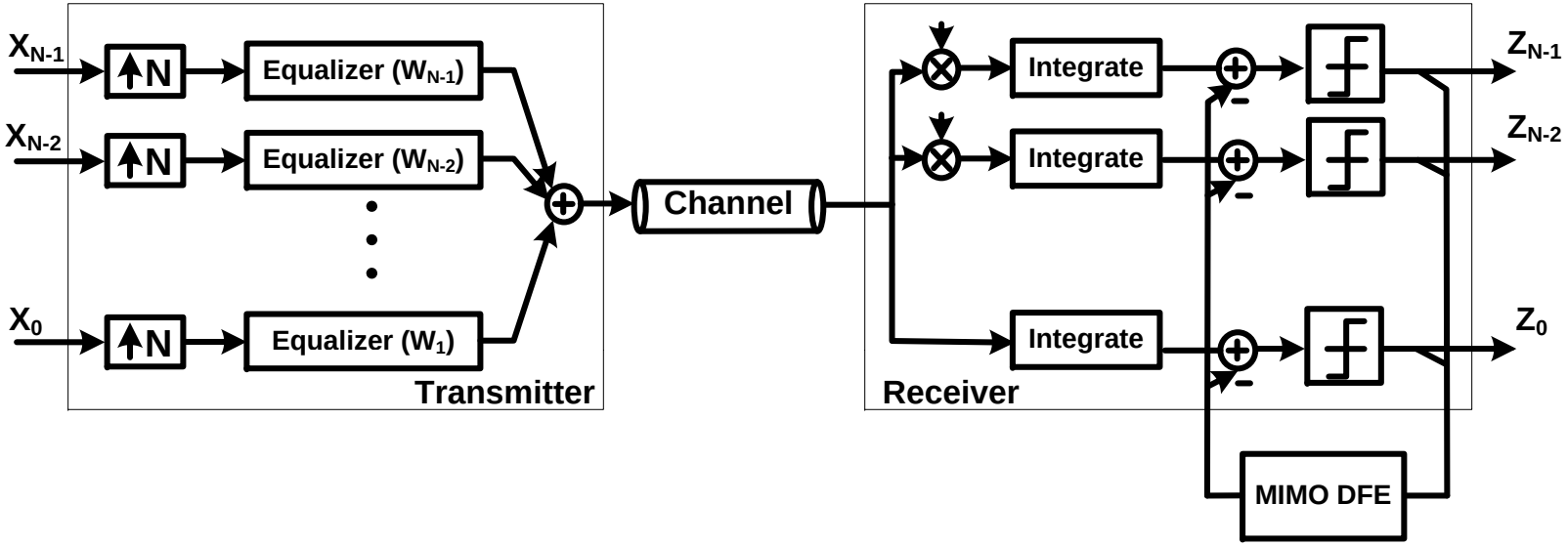
- Baseband 2PAM or 4PAM
- 4-5 tap discrete linear transmit equalizer
- 5-20 tap decision feedback equalizer (DFE)

Channel Characteristics in Links



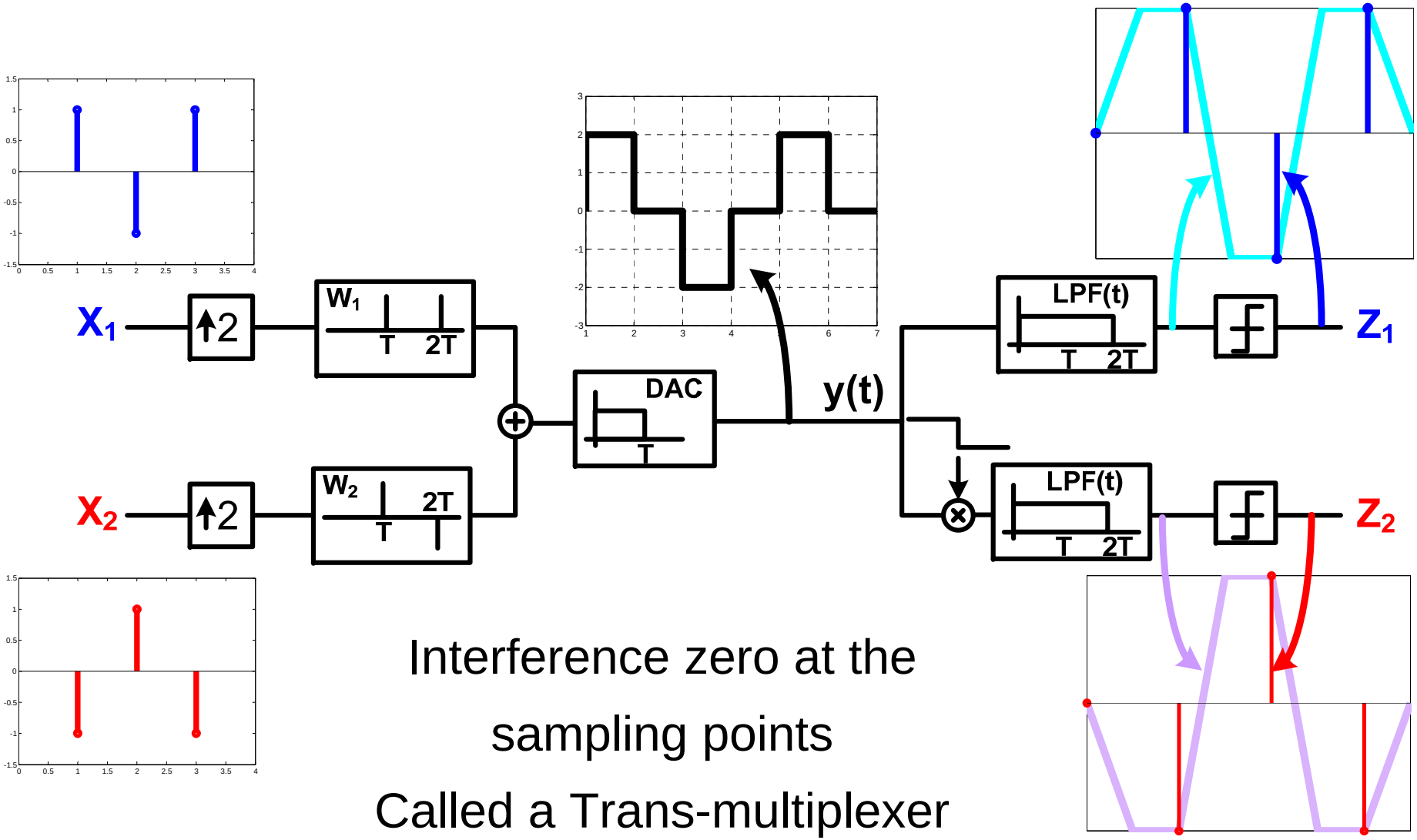
- Notches caused by reflections
  - From impedance discontinuities
  - E.g. vias, stubs, package, parasitic capacitance, etc
- Multi-Tone signaling can improve performance

A Practical AMT Architecture



- Small number of sub-channels (N)
  - 2, 3, or 4 in most cases
- N-times over-sampled equalizer per sub-channel at the transmitter
- Multi-Input Multi-Output (MIMO) DFE at the receiver
- AMT is a generalization of a baseband system

Two-Channel Example



Interference zero at the sampling points

Called a Trans-multiplexer

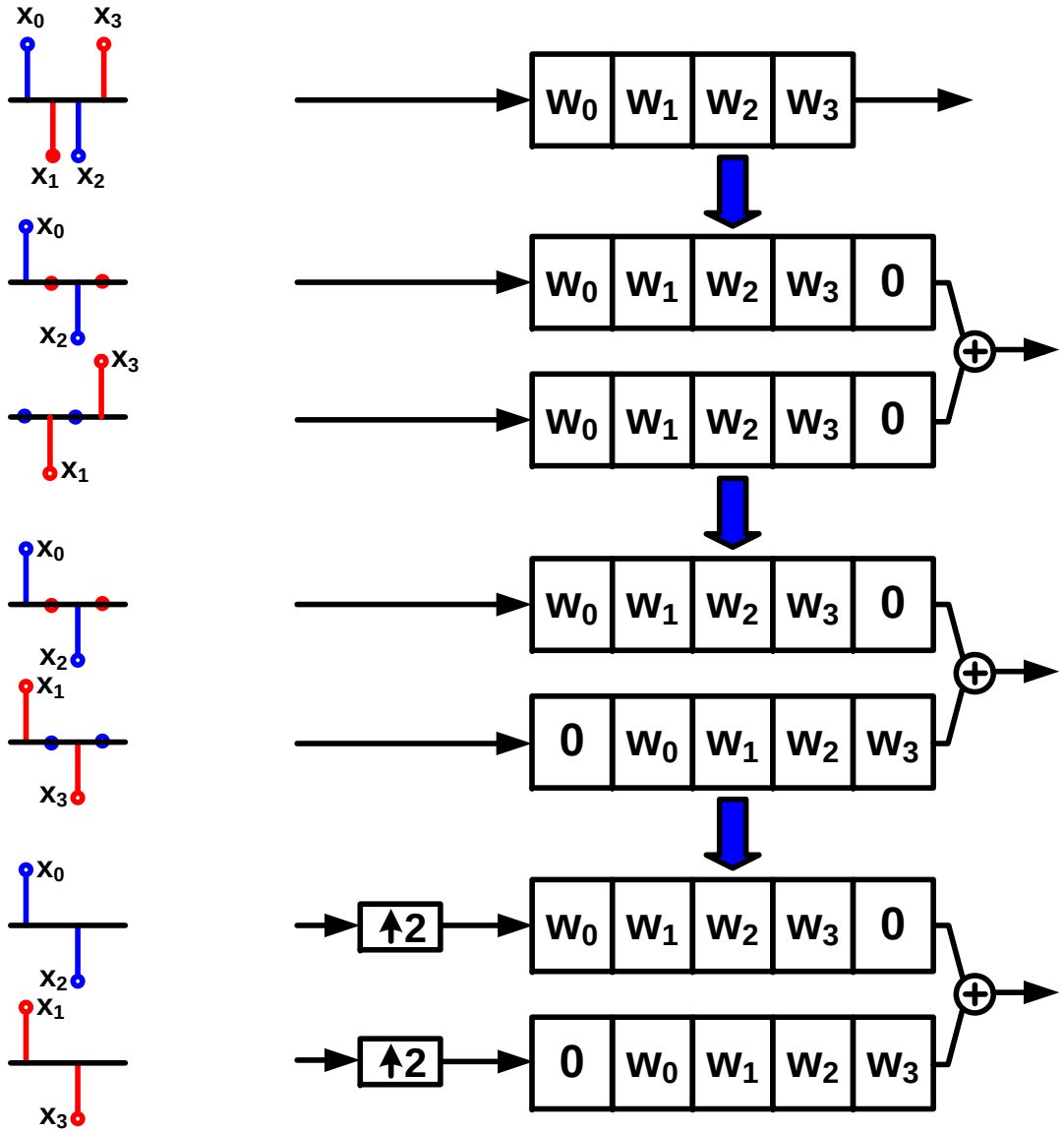
Evolution of a Baseband Tx Equalizer

4-tap BB transmitter

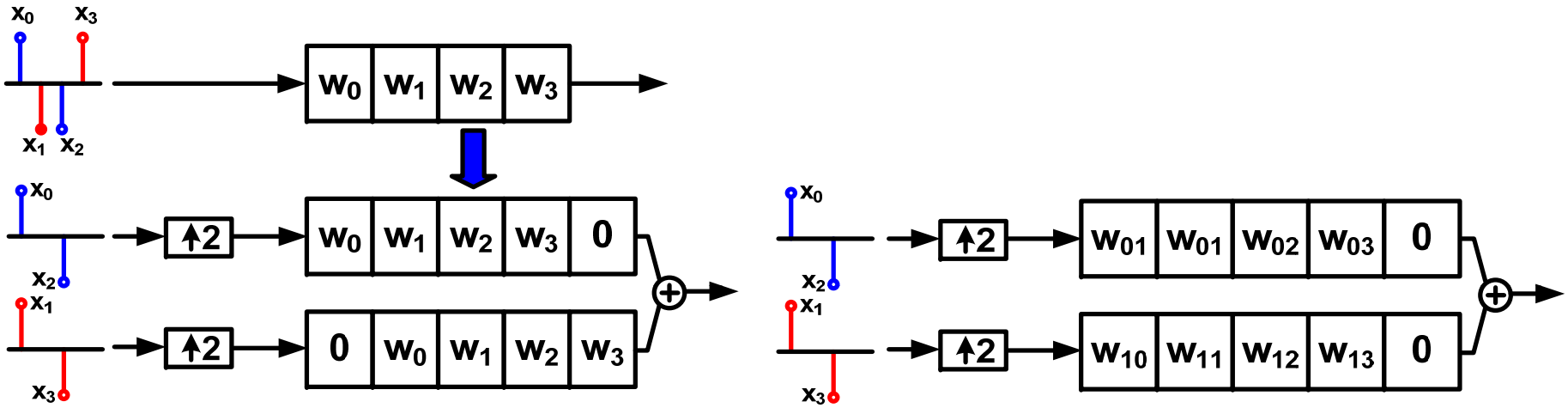
2-way parallelize

Shift “x” to the left
Shift “W” to the right

Represent as
over-sampled equalizer



AMT is a Generalization of Baseband

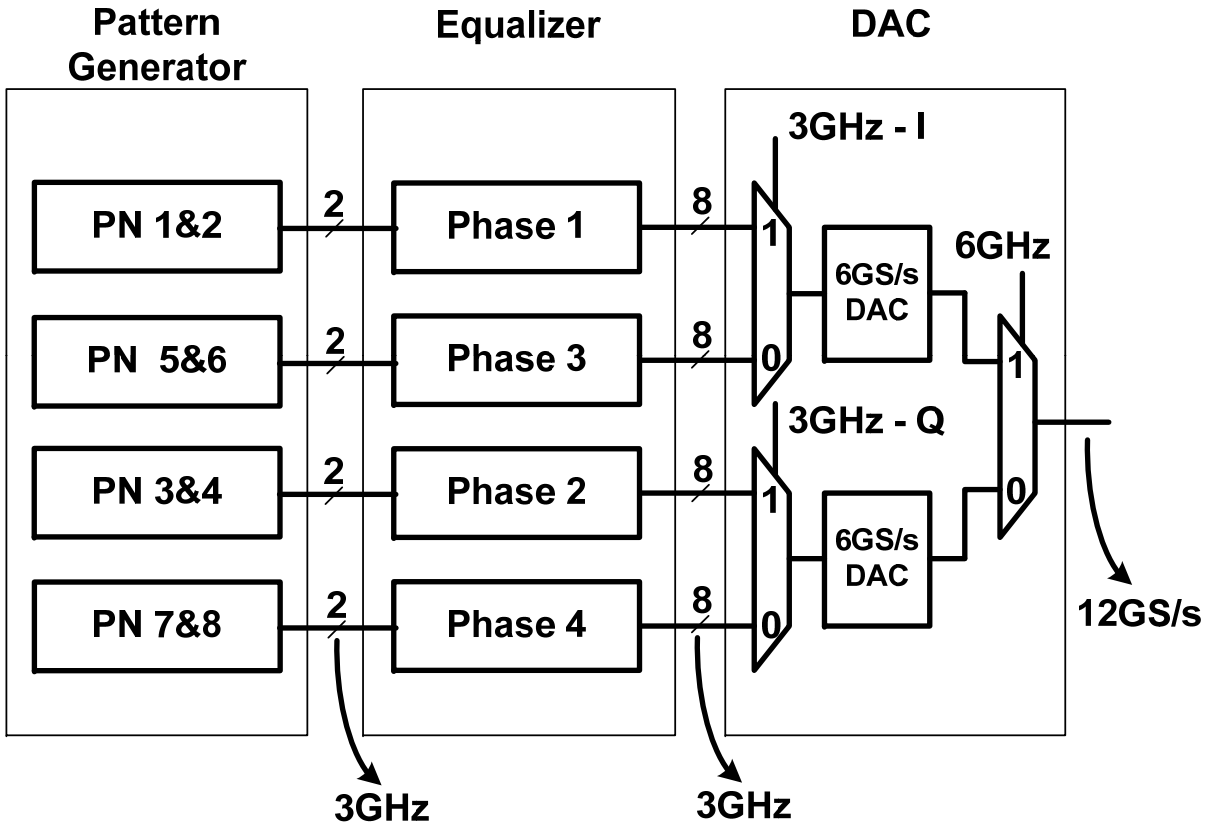


4-tap Baseband (2-way parallelized)

2-Channel AMT 4 taps per channel

- AMT has more degrees of freedom
  - Better capable of shaping the transmit spectrum
- MIMO DFE is also a generalization of a BB DFE

Software Programmable Transmitter

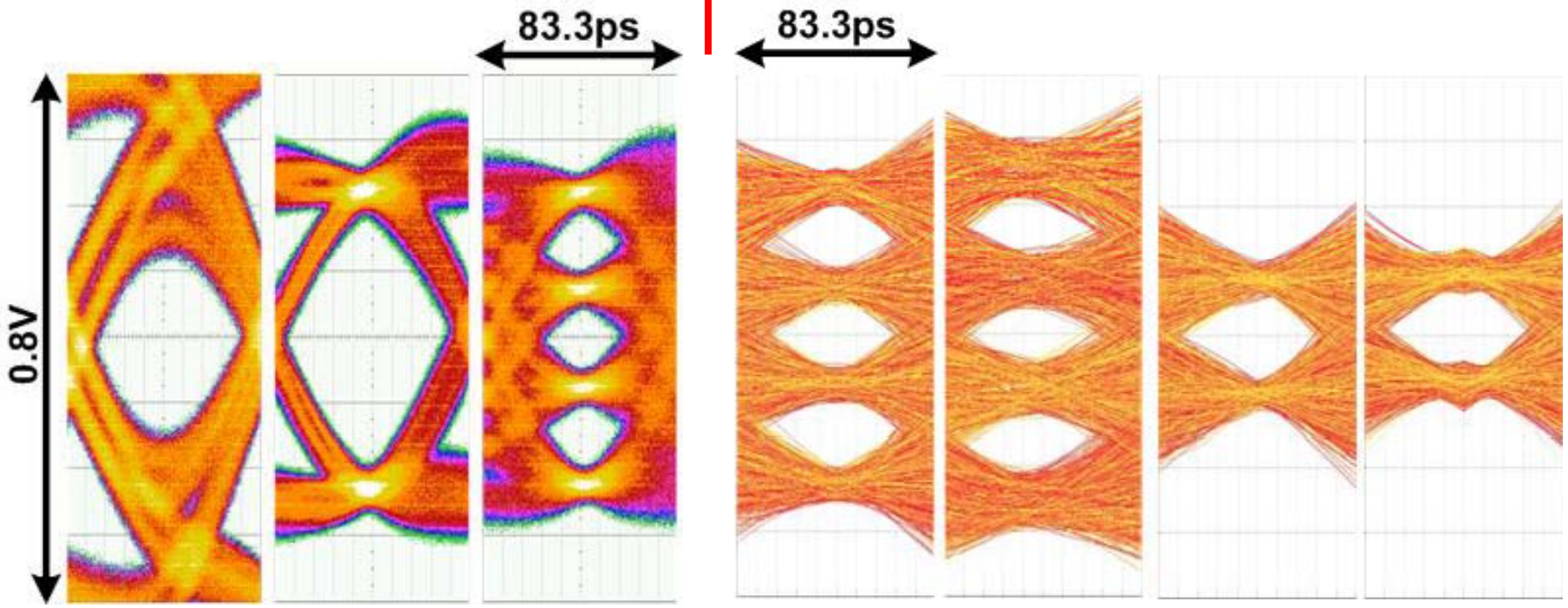


- Equivalent functionality
  - 16-tap FIR filter at 12GHz
  - 2-bit inputs (4PAM) and 10-bit taps

Measured Eye Diagrams

Baseband Mode

AMT Mode



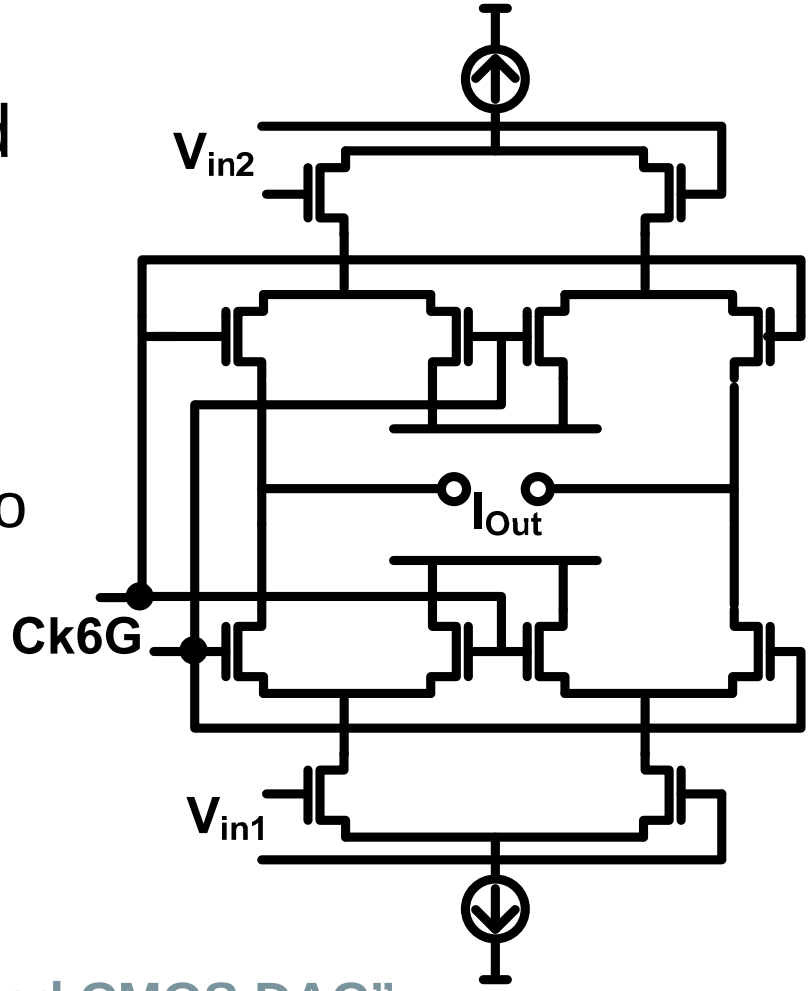
2PAM	2PAM	4PAM	Ch1	Ch2	Ch3	Ch4
Un-Equalized	Equalized	Equalized	4-channel AMT (Equalized – Post Processed)			
12Gb/s	12Gb/s	24Gb/s	18Gb/s			

On an oscilloscope

Rx implemented in Matlab

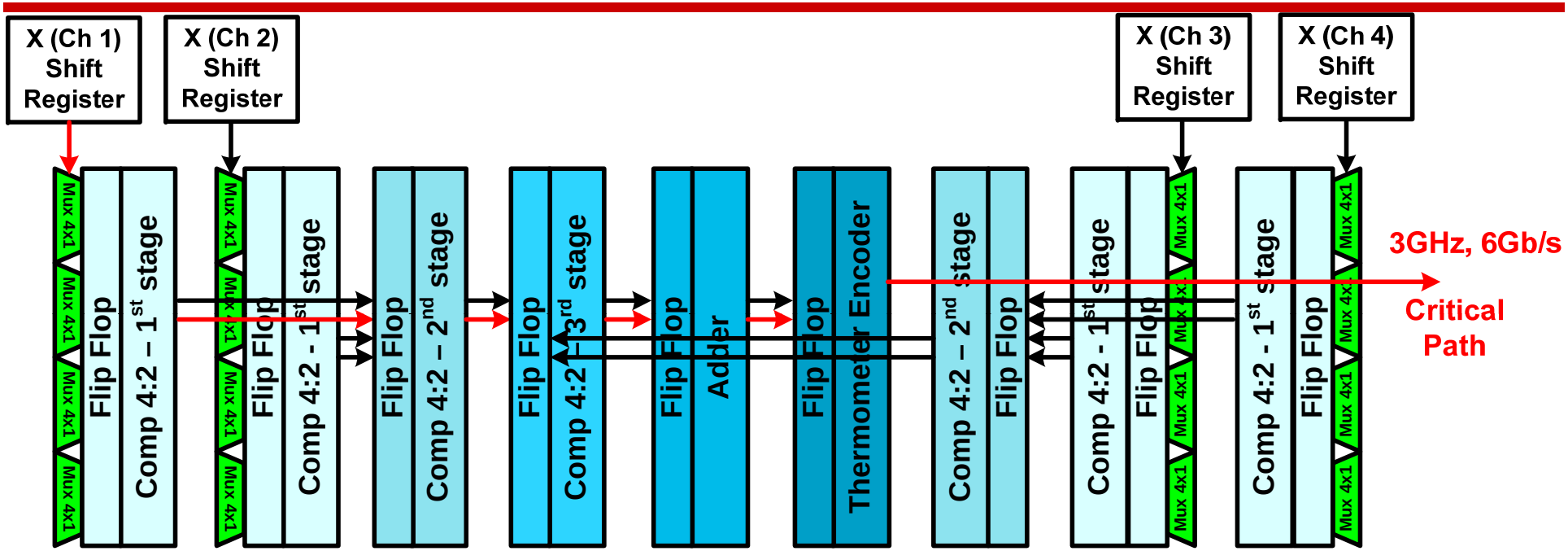
12GS/s Digital to Analog Converter

- 2-way output multiplexed current-mode DAC
- Termination supply 1.8V
  - Unused current dumped to 1.0V to save power
- $1.8V_{pp}$ output swing



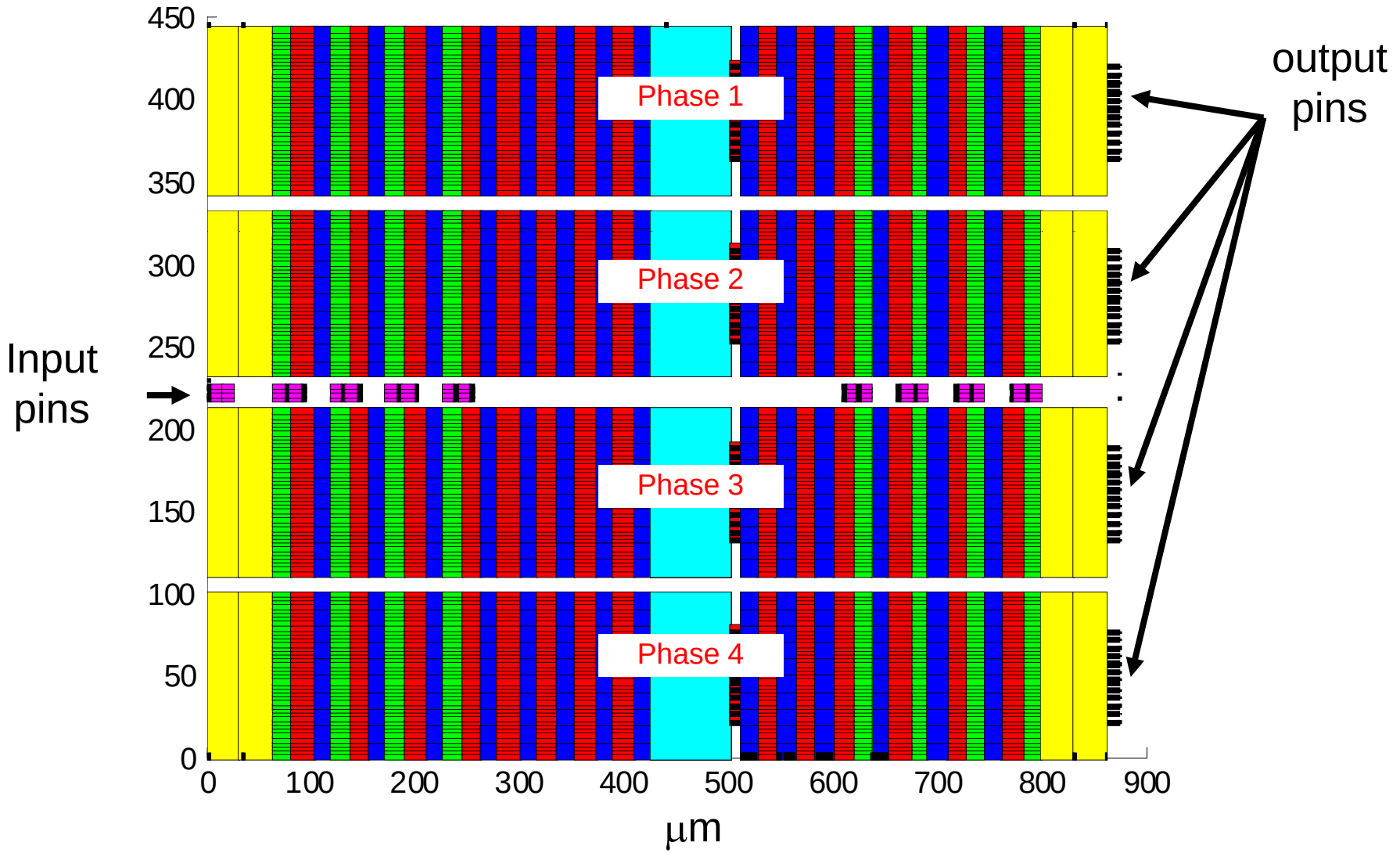
Savoj, et al, "12GS/s Phase Calibrated CMOS DAC", Companion paper, Session 7

Digital Equalizer Datapath (One Phase)

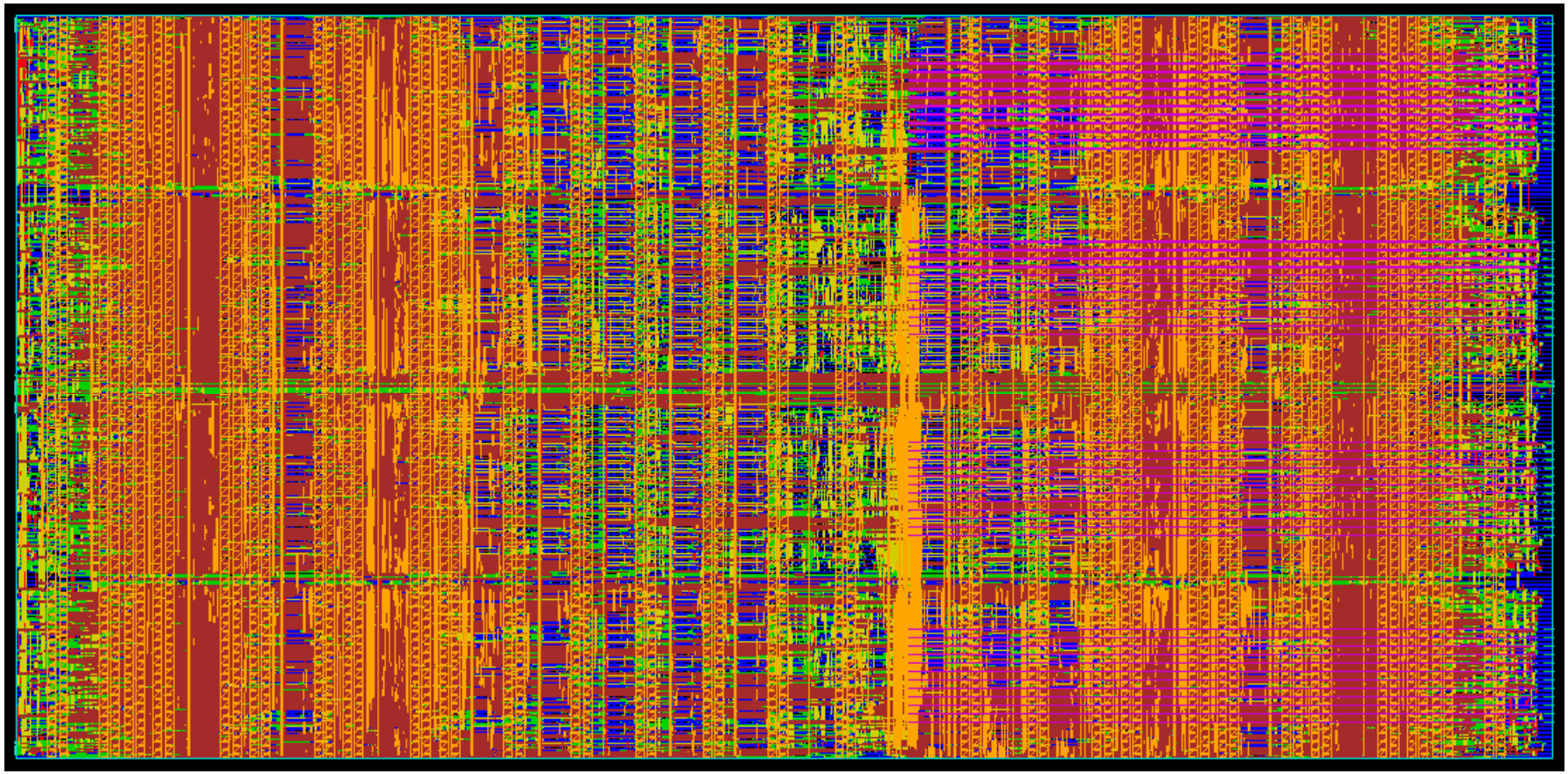


- Multiply 16 2-bit numbers by 16 10-bit numbers
  - Multiplication using 4:1 multiplexers
  - W and 3W stored in flops
- Add results using 4:2 compressor units
- 2-way parallelized to operate with a 1.5GHz clock

Equalizer Floorplan

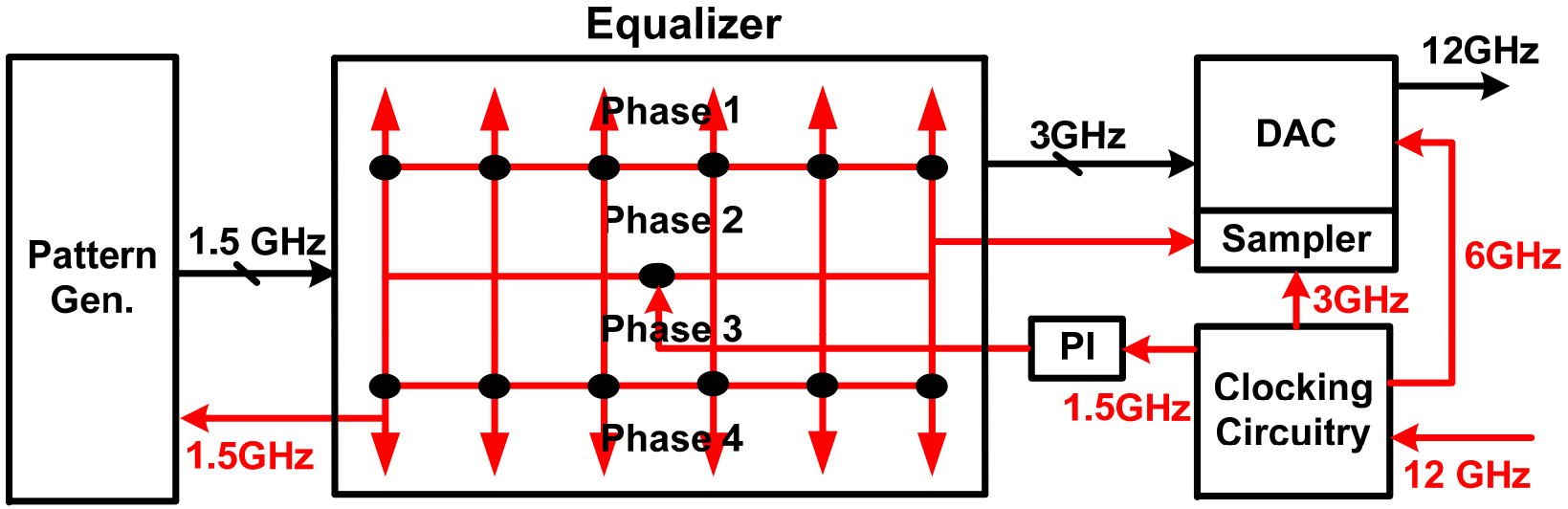


Complete Equalizer with Routing



Post Route layout in SOC Encounter

Transmitter Clocking



- Phase interpolator (PI) between DAC and equalizer
  - Programmed offline
- Mesh 1.5GHz clock distribution in the equalizer
- Pattern generator clock branches off from equalizer grid
  - Part of the clock distribution latency in the critical path

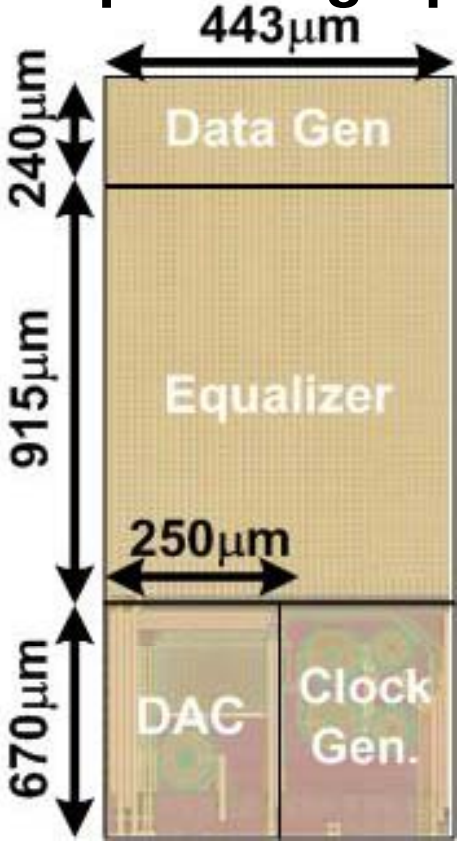
Performance Summary

Measured Transmitter Performance

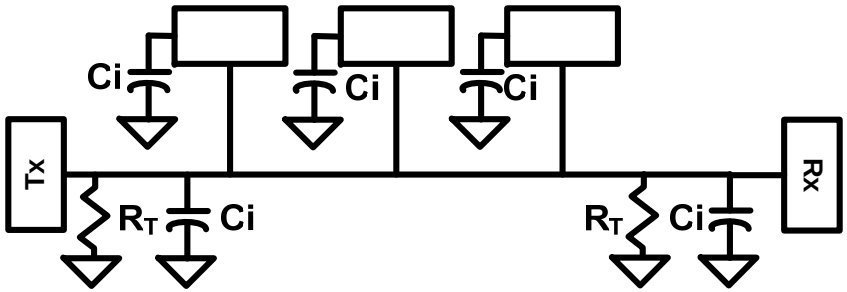
Process	90nm CMOS
Maximum Rate	29Gb/s
Digital Power	350mW
Analog Power	160mW
Area	0.8mm^2
Output Swing	1.6V$_{pp}$

21mW/Gbps

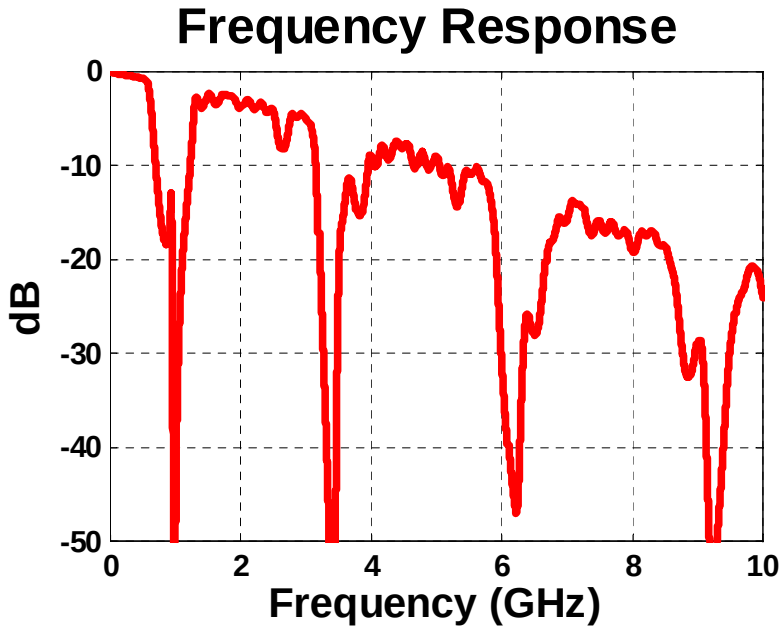
Chip Micrograph



Multi-Tone Operation

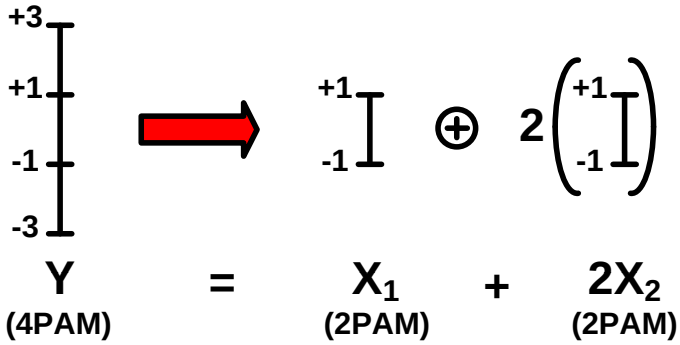


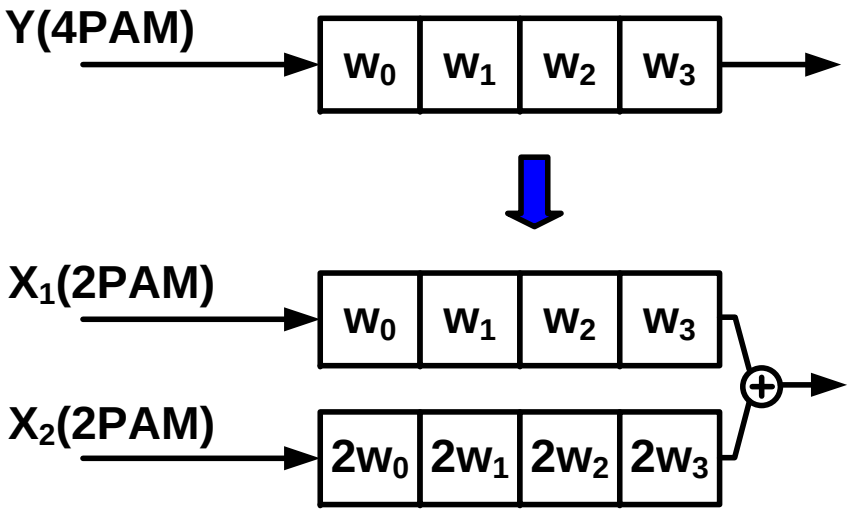
Multi-Drop Configuration
C_i = 1pF

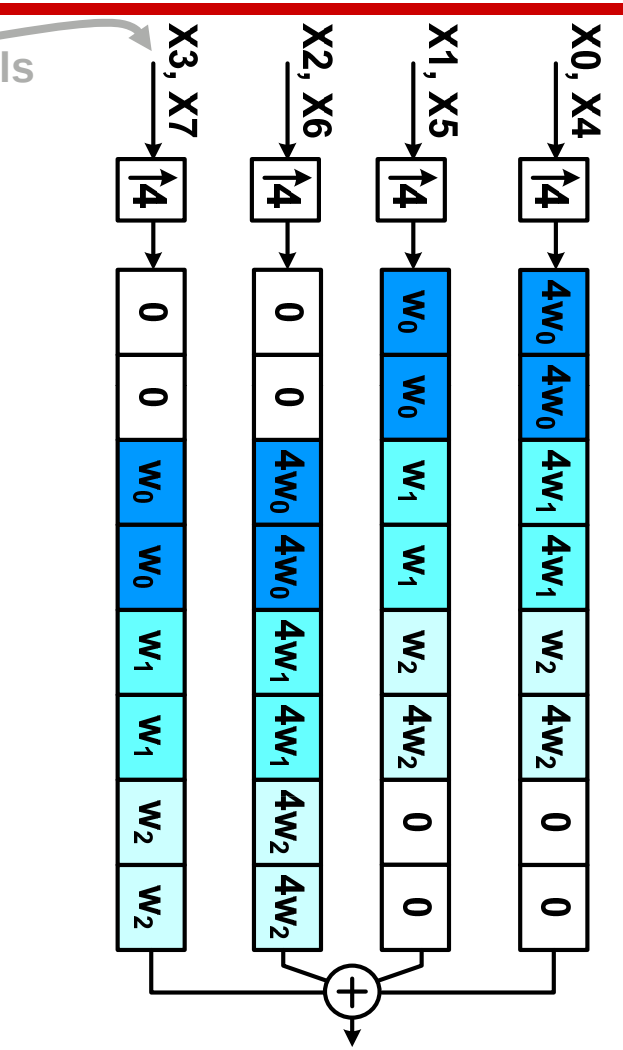


Measured
3-Channel AMT, 9Gb/s

Multi-PAM Operation

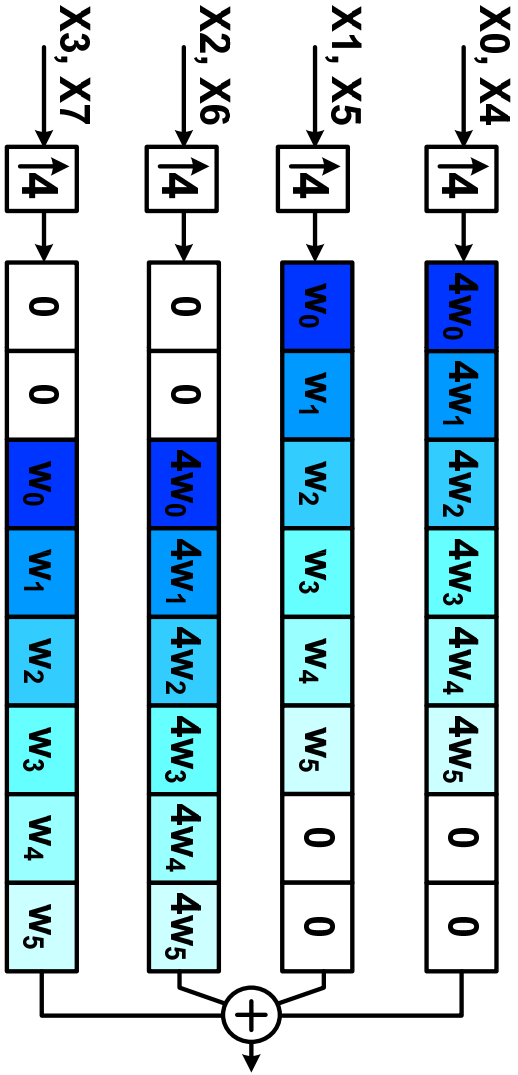






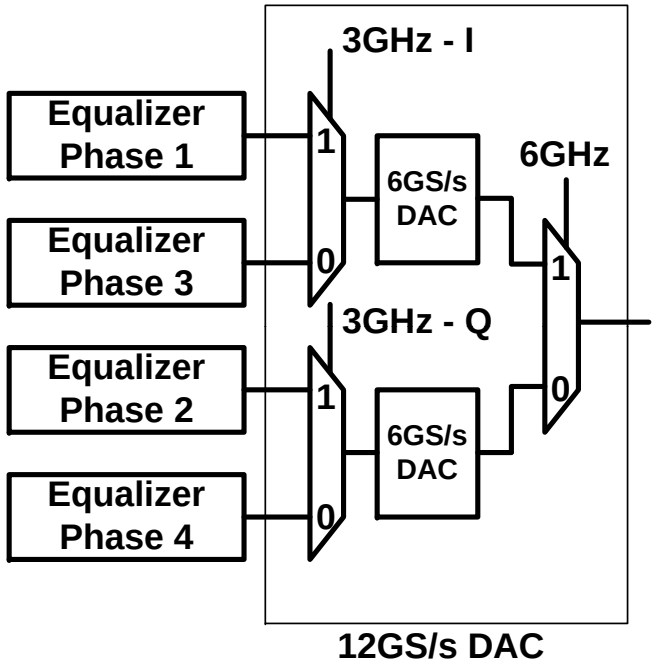
Tx configuration in 8PAM/16PAM mode

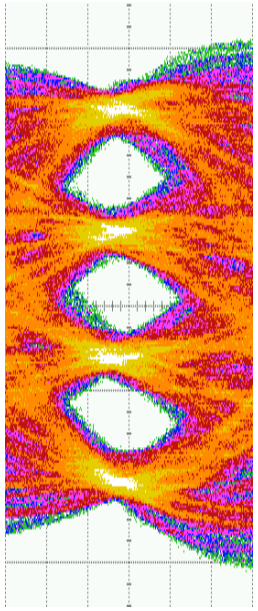
Fractional Equalization

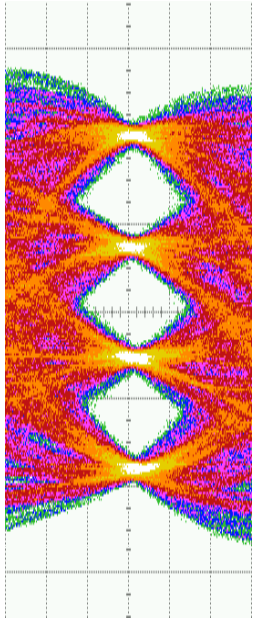


Measured
8PAM Baseband, 18Gb/s

Cyclically Time-Variant Equalization







4 different paths to output → **4 different responses**

Time-Invariant Equalization SIDR = 26dB 28Gb/s

Time-Variant Equalization SIDR = 31dB 28Gb/s

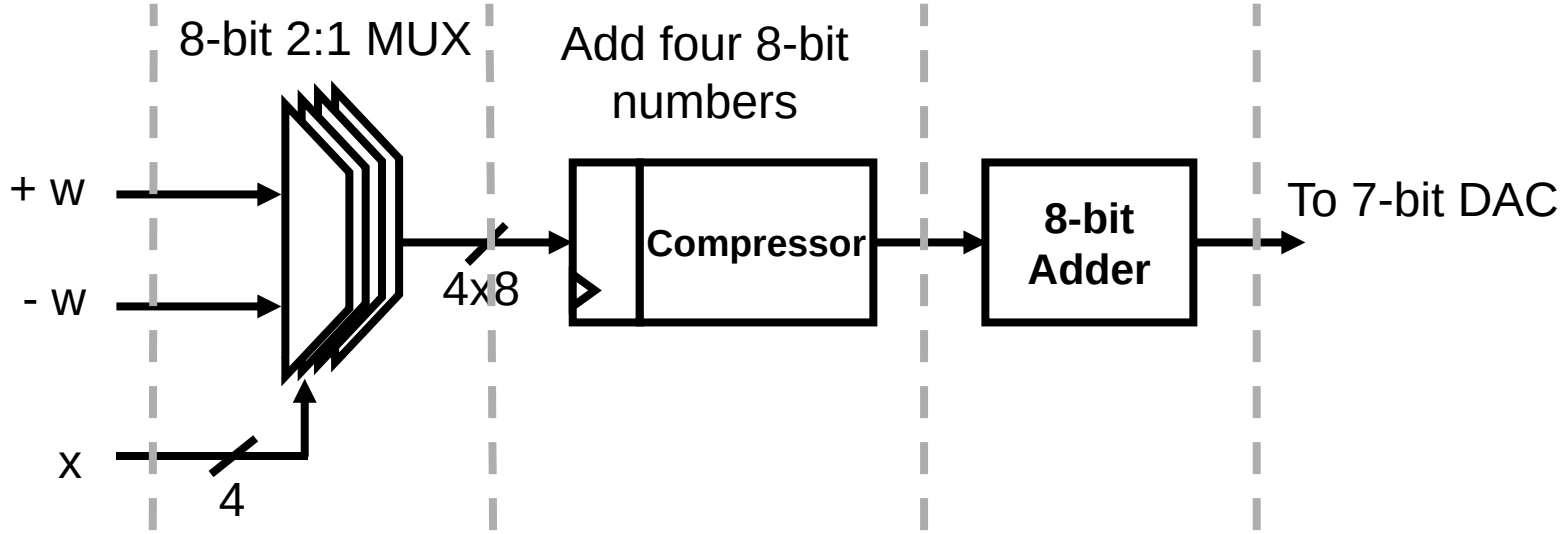
A. Amirkhany, et al, "*Time-Variant Characterization and Compensation of Wideband Circuits*," CICC 2007

Conclusions

- A 4-way parallelized equalizer with each parallel branch programmed independently supports
  - Analog Multi-Tone
  - Multi-level baseband
  - Fractional (over-sampled equalization)
  - Cyclically time-variant equalization
- Power overhead due to digital implementation
  - Instead of pseudo-DAC
- Area overhead for storing more tap coefficients

Digital Implementation Overhead

A 4-tap 2PAM 6Gbps Tx



Power	0.5mW	10.3 mW Includes clock power inside flops	5.0 mW
Area	960 um^2	16,000 um^2	8,000 um^2

Total Power Overhead = 16.0 mW (2.6mW/Gbps)

Total Area Overhead = 25,000um^2

Compared to a Pseudo-DAC implementation