Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications

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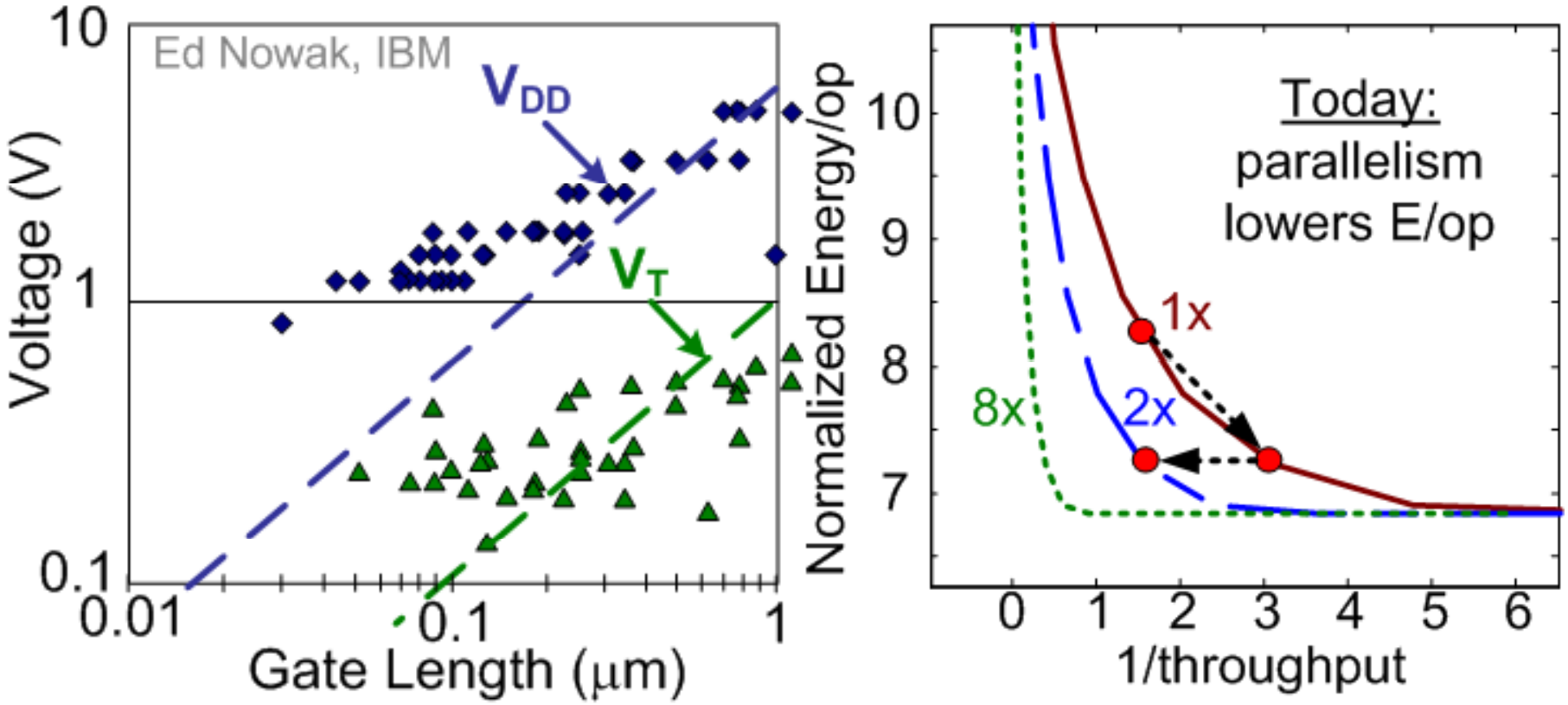
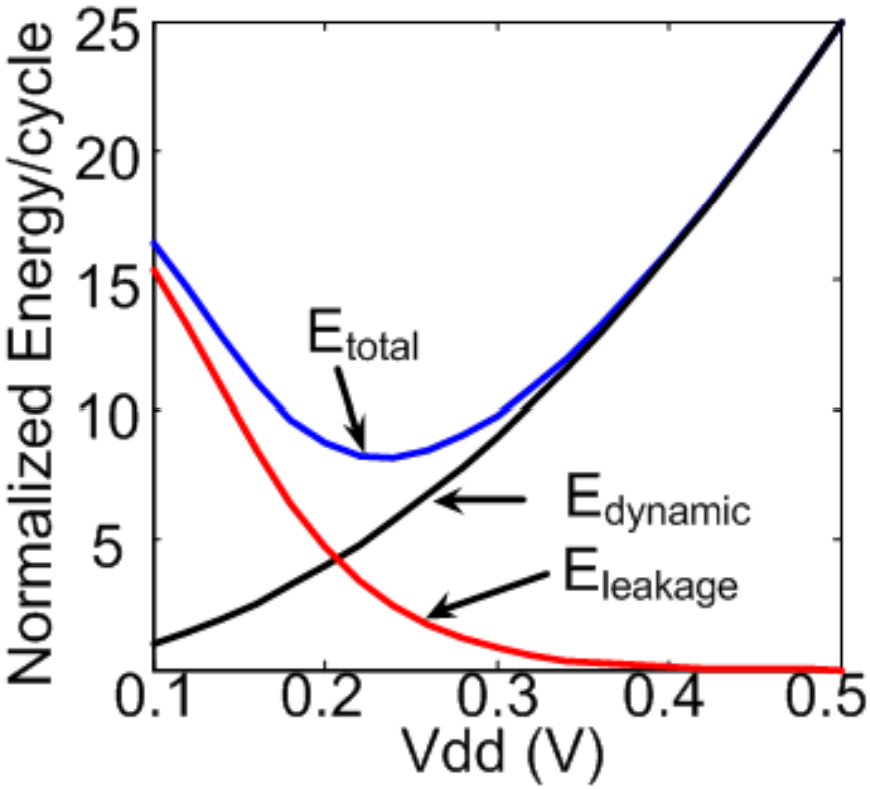
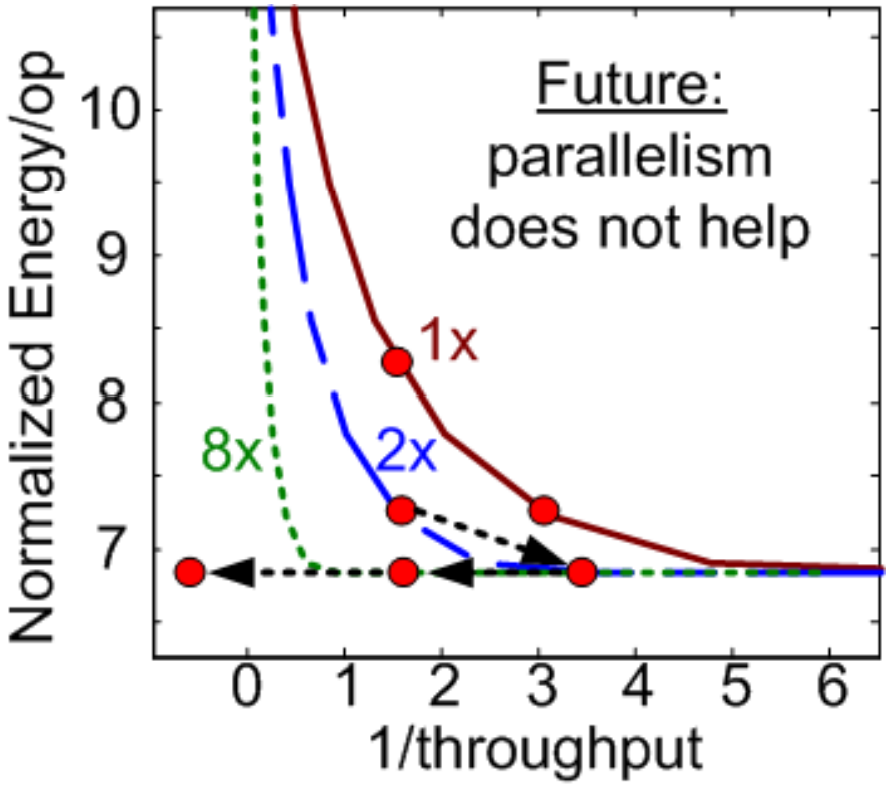
CMOS Scaling and Power



- V_{DD} and V_T no longer scaling well
  - Power/Area increases at each technology node
- Parallelism enables lower power for the same throughput

CMOS Scaling and Power

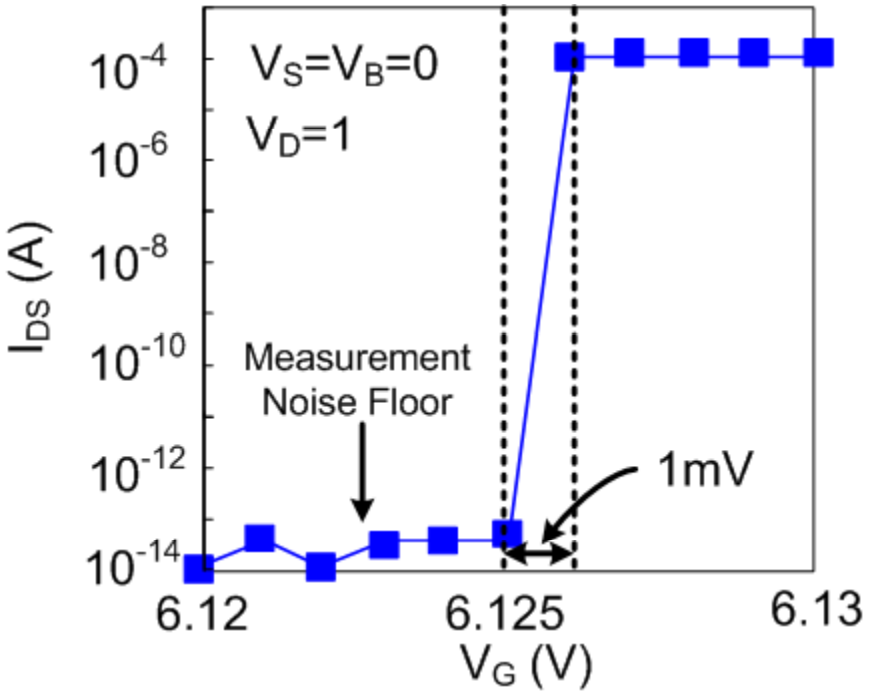




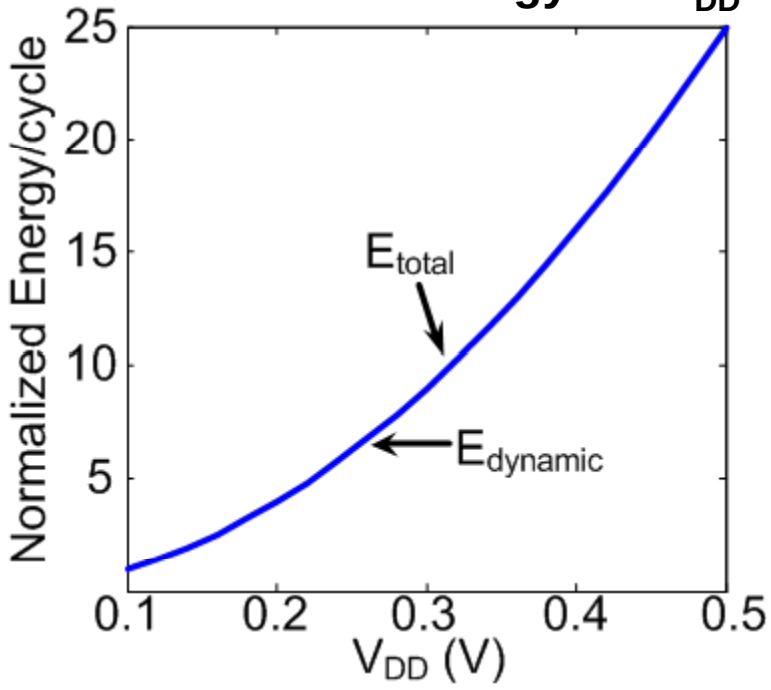
- Leakage and sub-threshold slope define minimum energy/op for CMOS
- Parallelism can't reduce power if already operating at minimum energy

MEM Switches Offer Zero Leakage

Measured MEM Switch I-V Curve



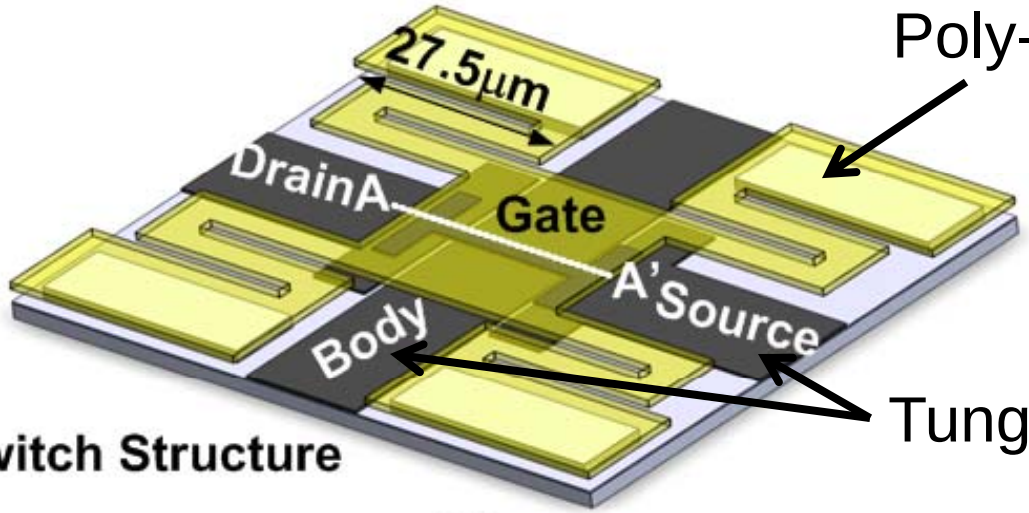
MEM Switch Energy vs. V_{DD}



- MEM switches show zero leakage and sharp sub-threshold slope [1]
- Could potentially enable reduced E/op with scaling

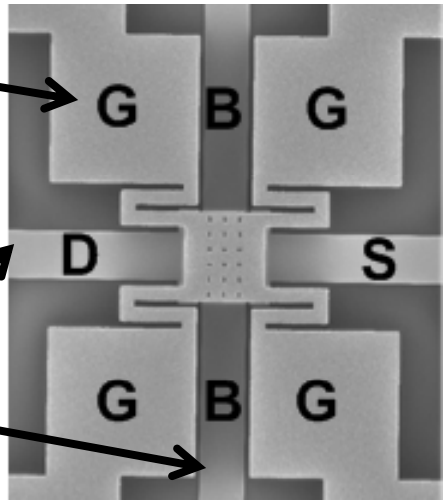
[1] Nathanael, et al. *IEDM '09*

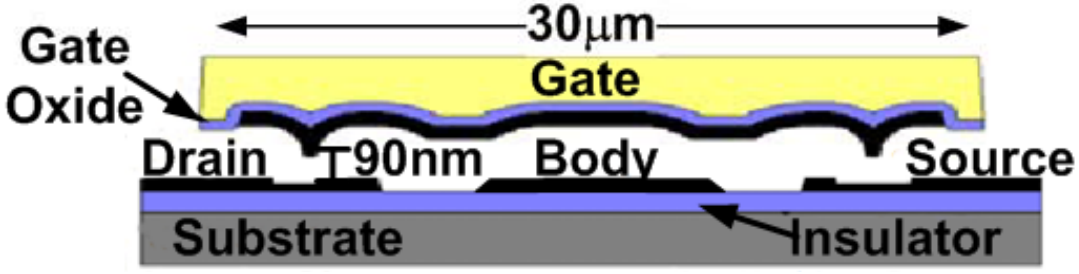
Structure and Operation of MEM Switch



Poly-SiGe

Tungsten





A-A' cross-section: *off*-state

A-A' cross-section: *on*-state

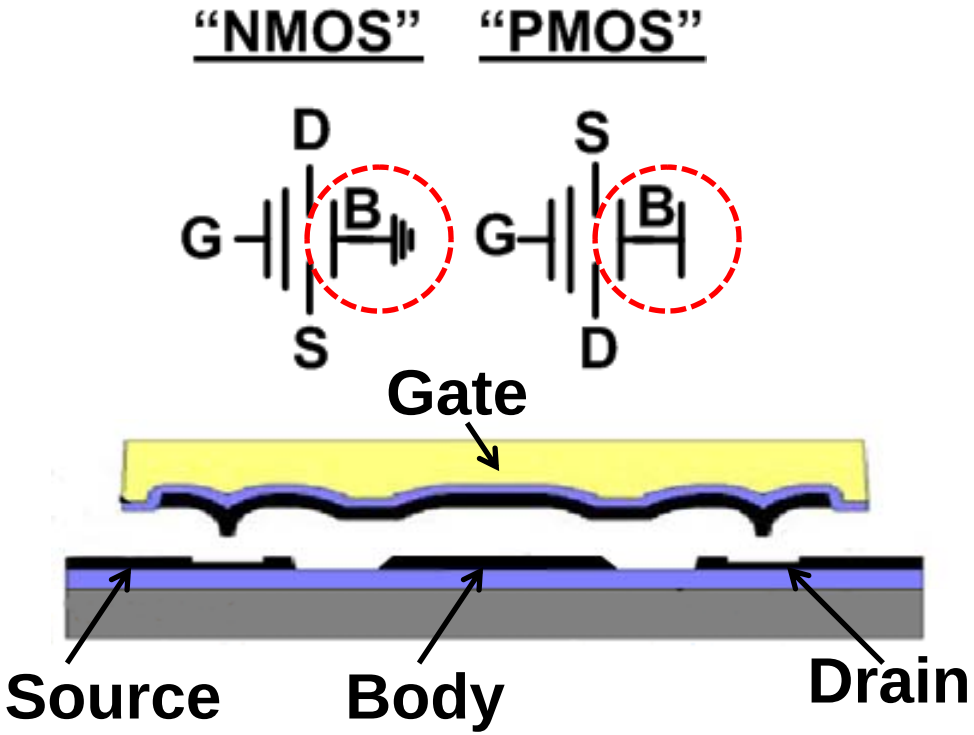
OFF Switch:

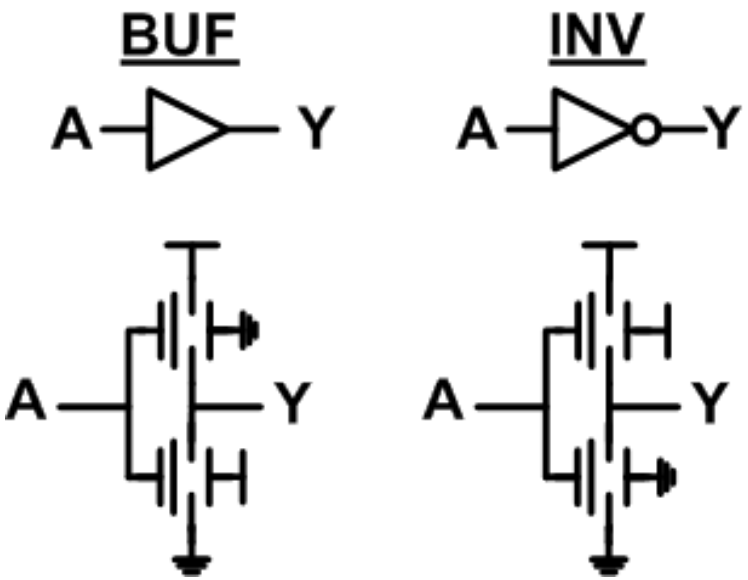
$|V_{gb}| < V_{po}$ (pull-out voltage)

ON Switch:

$|V_{gb}| > V_{pi}$ (pull-in voltage)

MEM Switches as Logic Elements

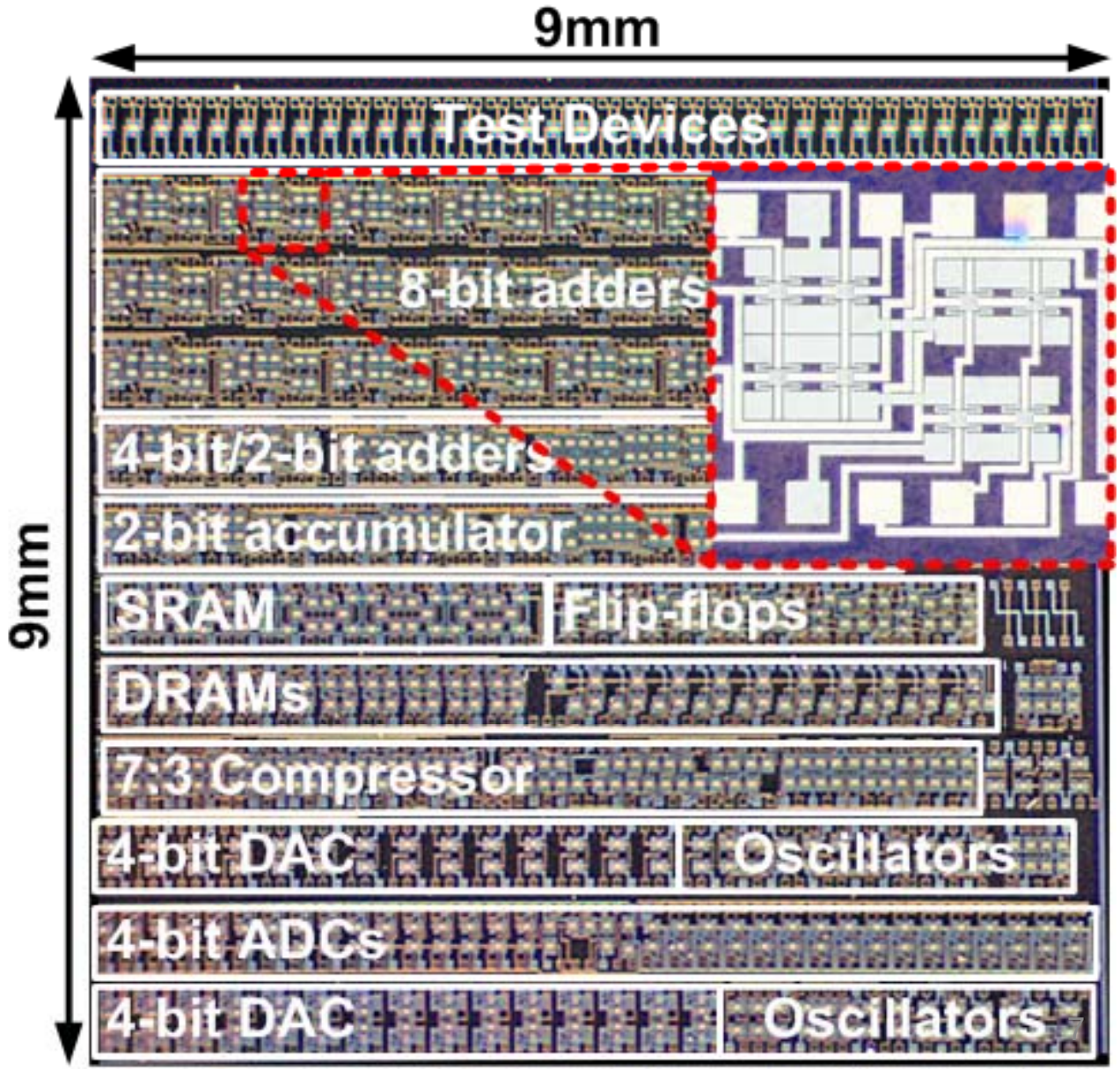




- Switches are ambipolar: absolute gate to body voltage determines actuation
- Conductance independent of drain/source voltage: non-inverting logic possible

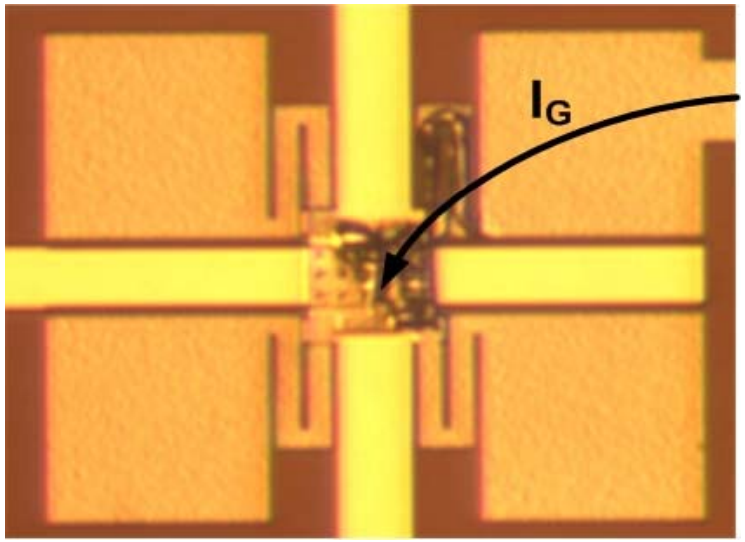
MEM Switch Testchip

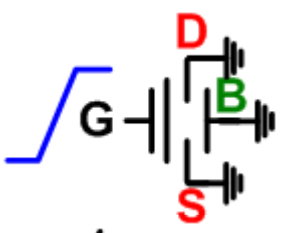
- Test Devices
- Logic
- Timing Elements
- Memory
- I/O



Things We Learned…

- Layout Matters
  - Unbalanced current flow: flexures burn up!
  - Parasitic capacitors: can affect V_{pi} (DIBL-like effect)





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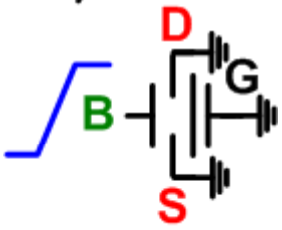
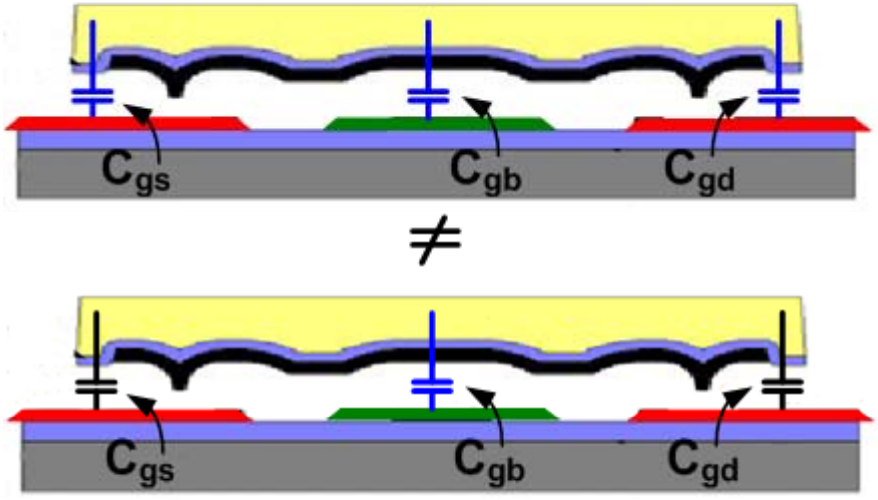
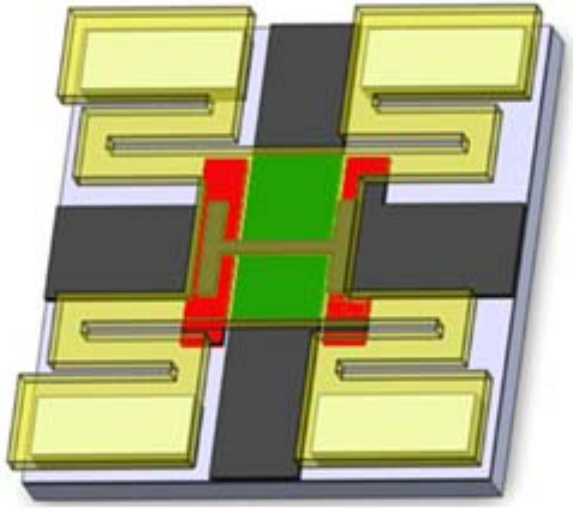
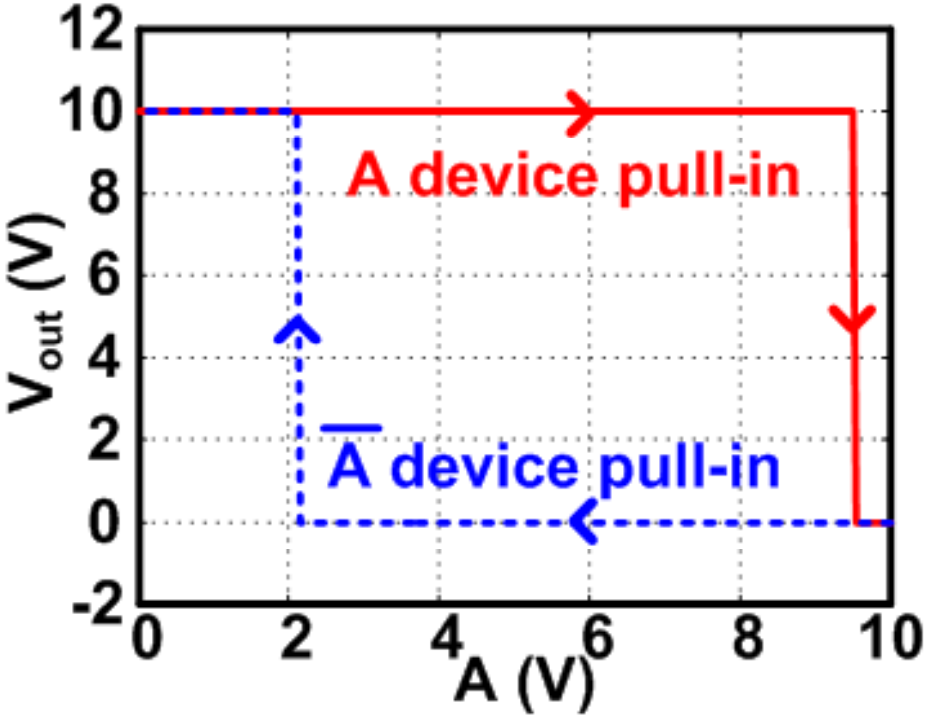
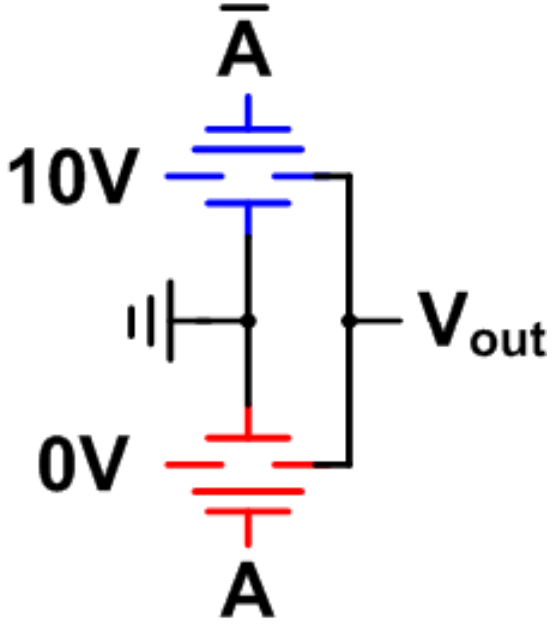






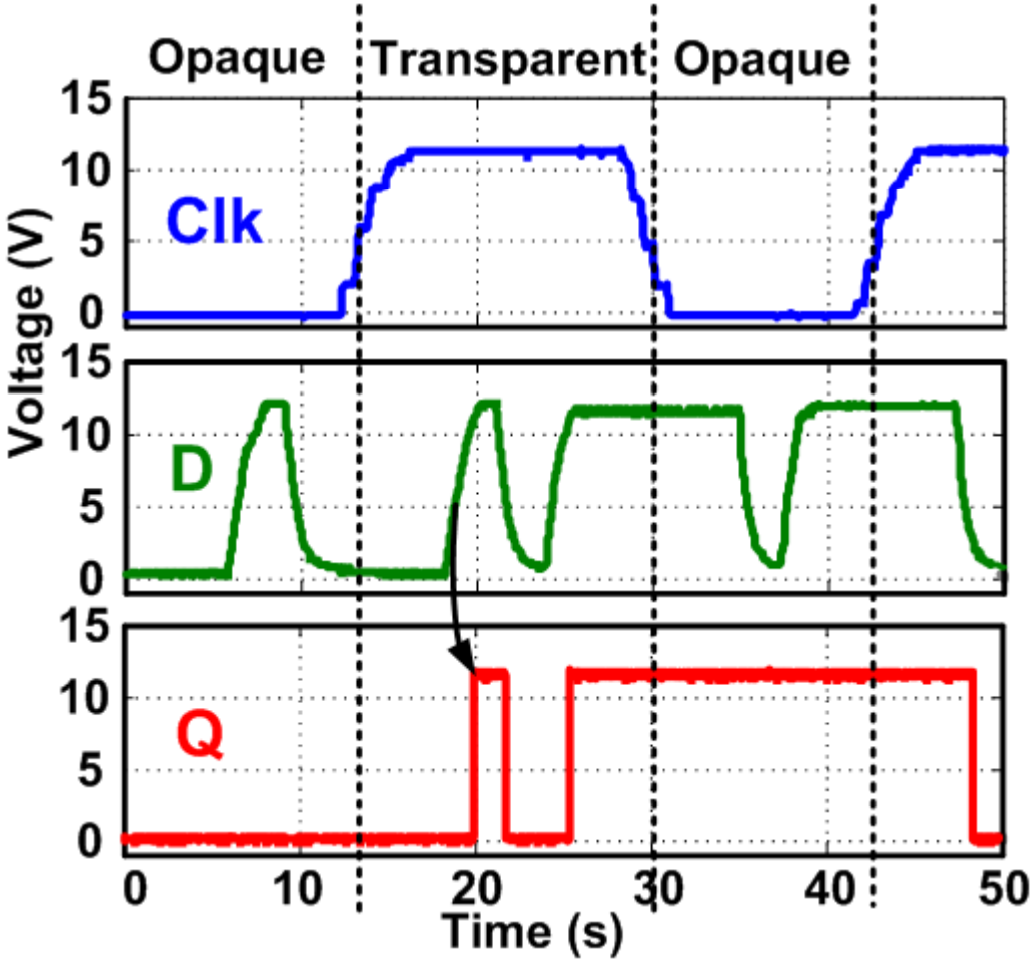
Measured Inverter VTC

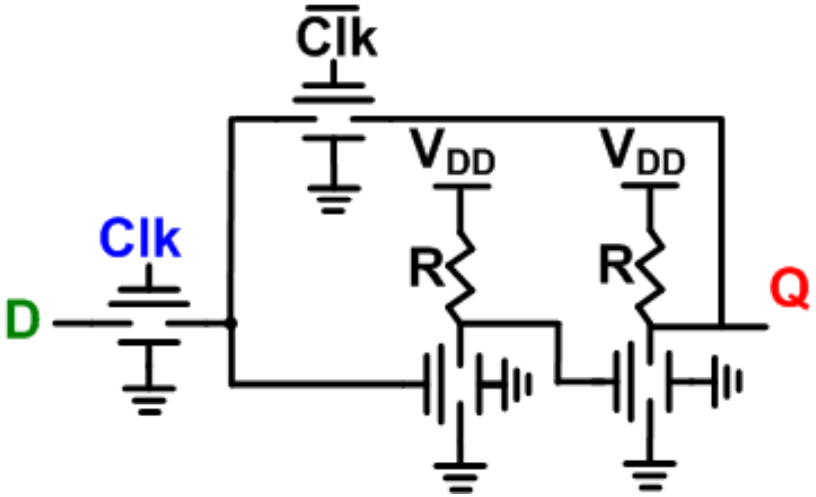




- VTC looks digital, suggests composability

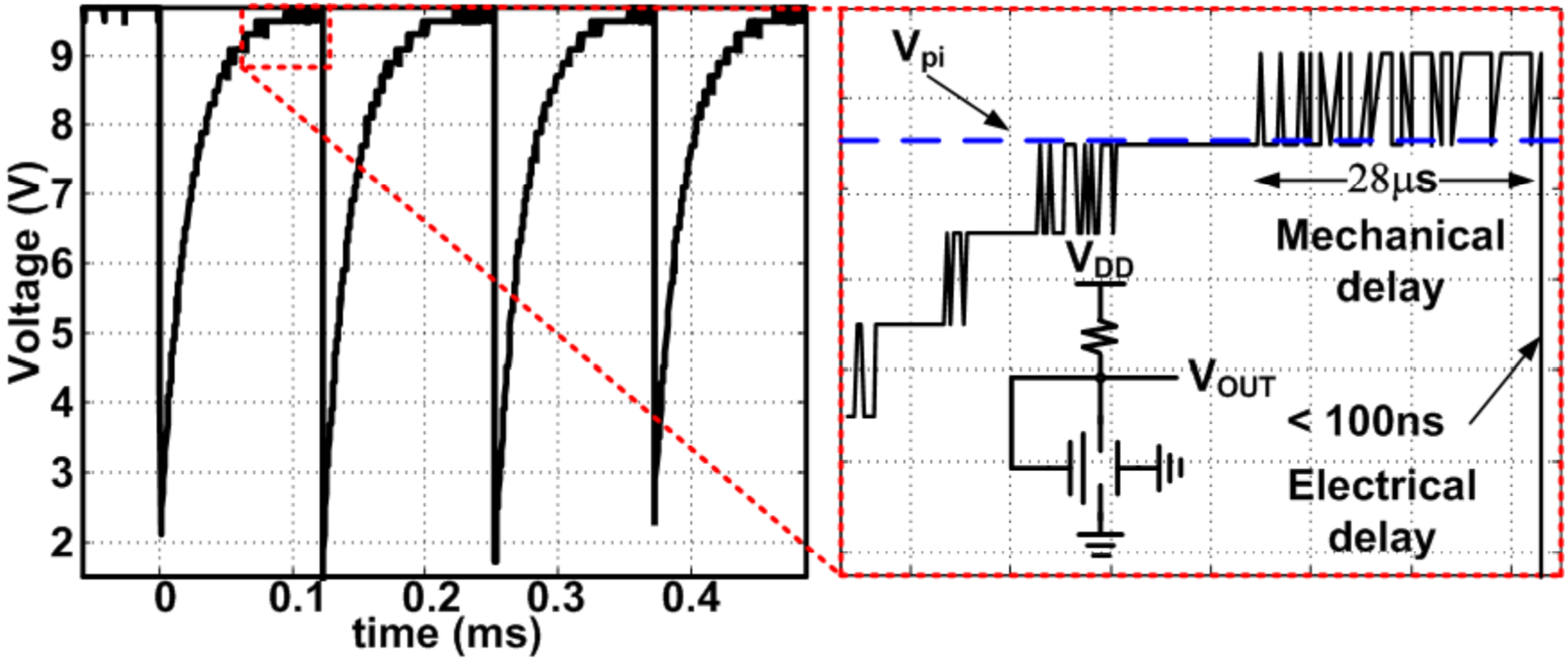
MEMS Latch Shows Composability





- Designed as if we used MOSFETS, but that is not always optimal…

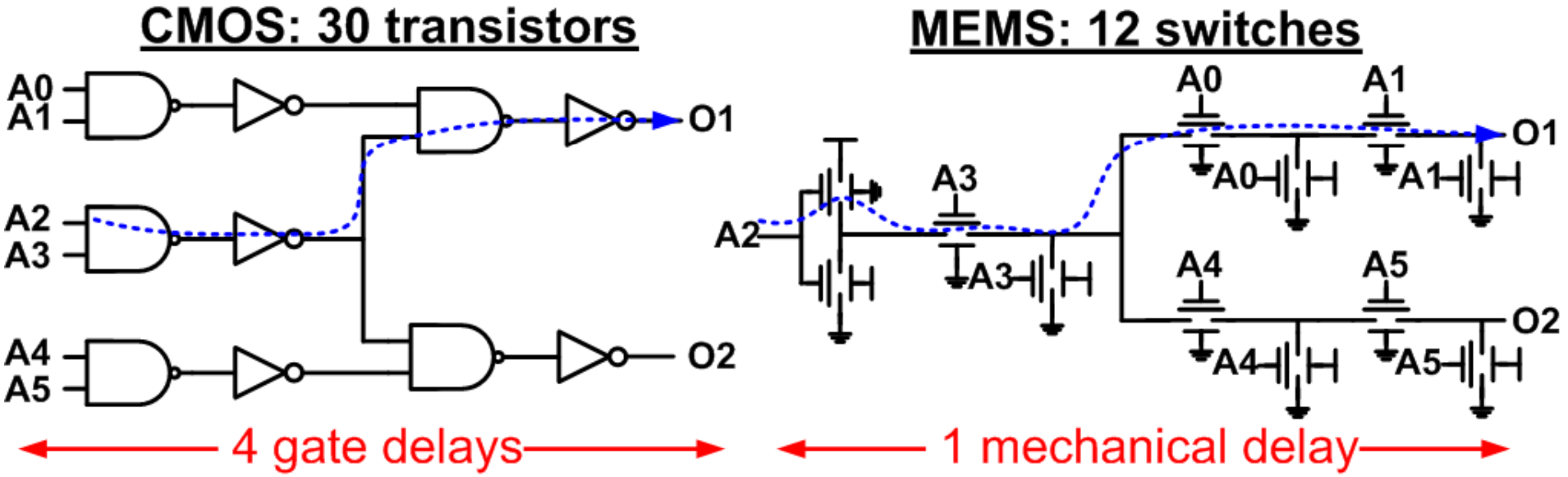
Oscillator Illustrates Delay Characteristics



- Mechanical time constant (τ_{mech}) >> electrical (τ_{elec})
- Contact resistance only affects τ_{elec}, not τ_{mech}.
  - Little impact on overall delay since τ_{mech} is large.
  - Higher $R_{contact}$ (1-10kΩ) improves reliability (>10^9 cycles [2])

[2] Kam, et al. *IEDM '09*

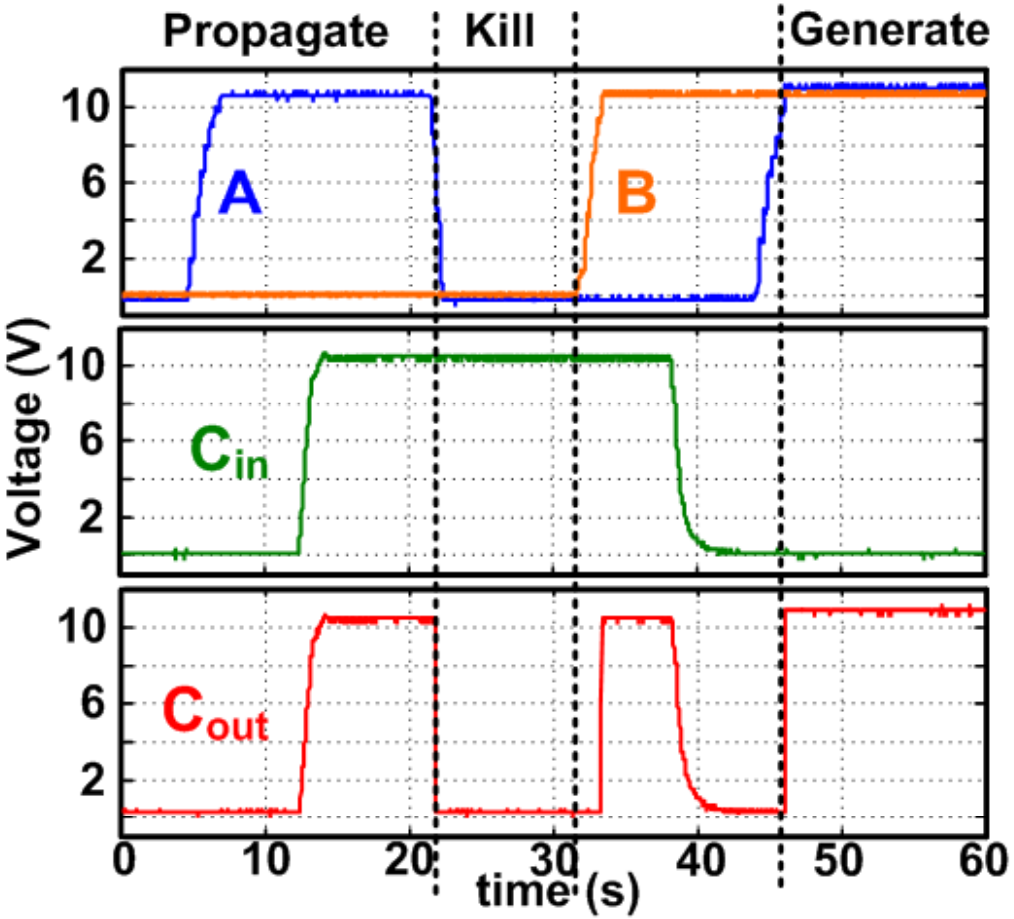
Digital Circuits with MEM Switches

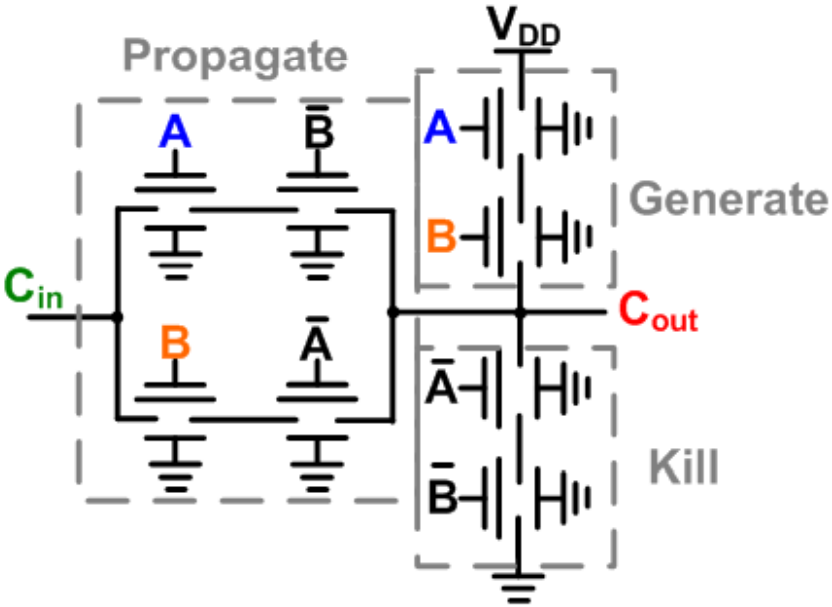


- MEMS: Implement logic as a single complex gate
  - Minimize number of mechanical delays
  - Improves area, device count, throughput
- Performance gap to CMOS shrinks to ~10x for 32-bit add (10ns delay at 90nm) [3]

[3] Chen, et al. *ICCAD '08*

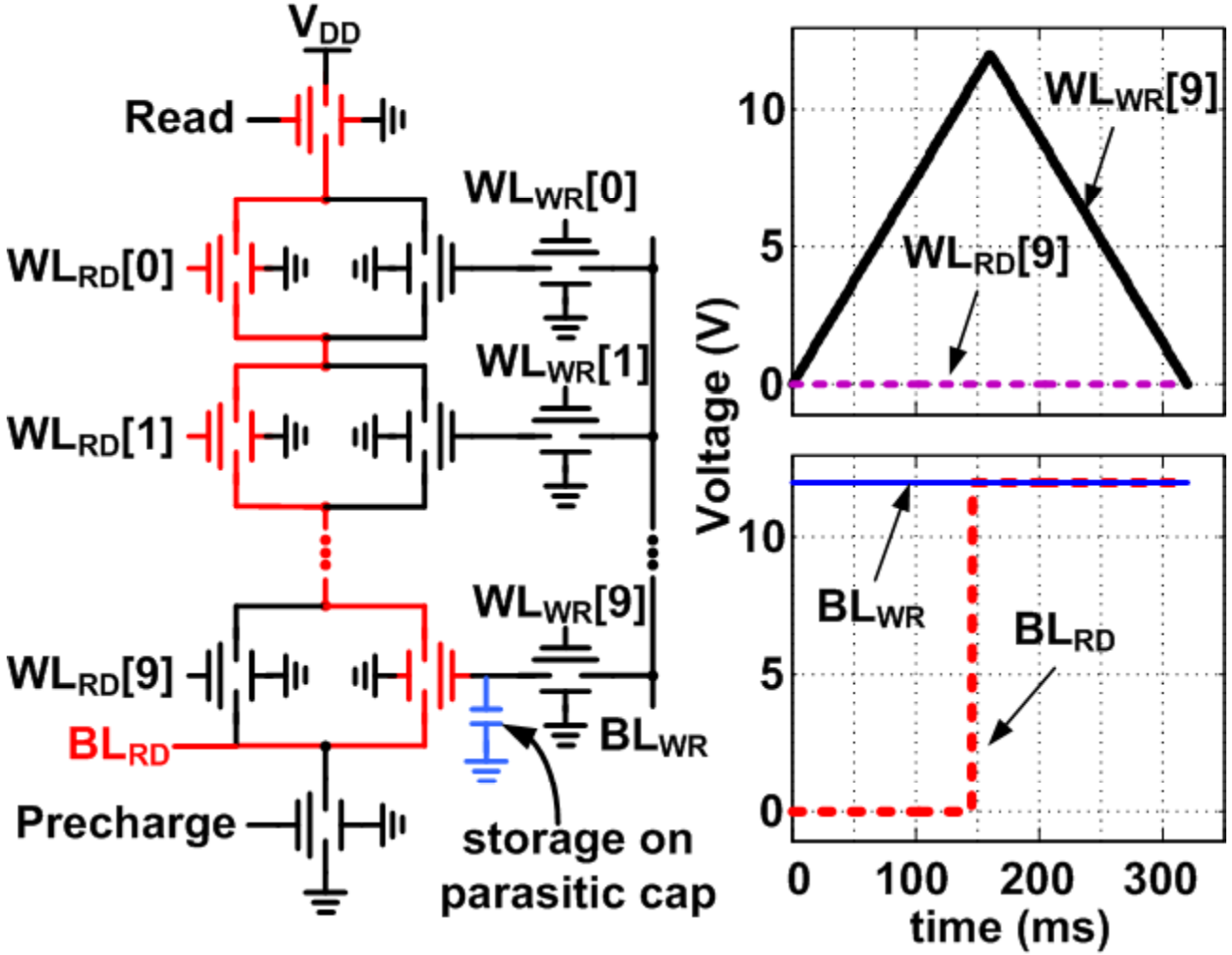
Switch-based Carry Generation





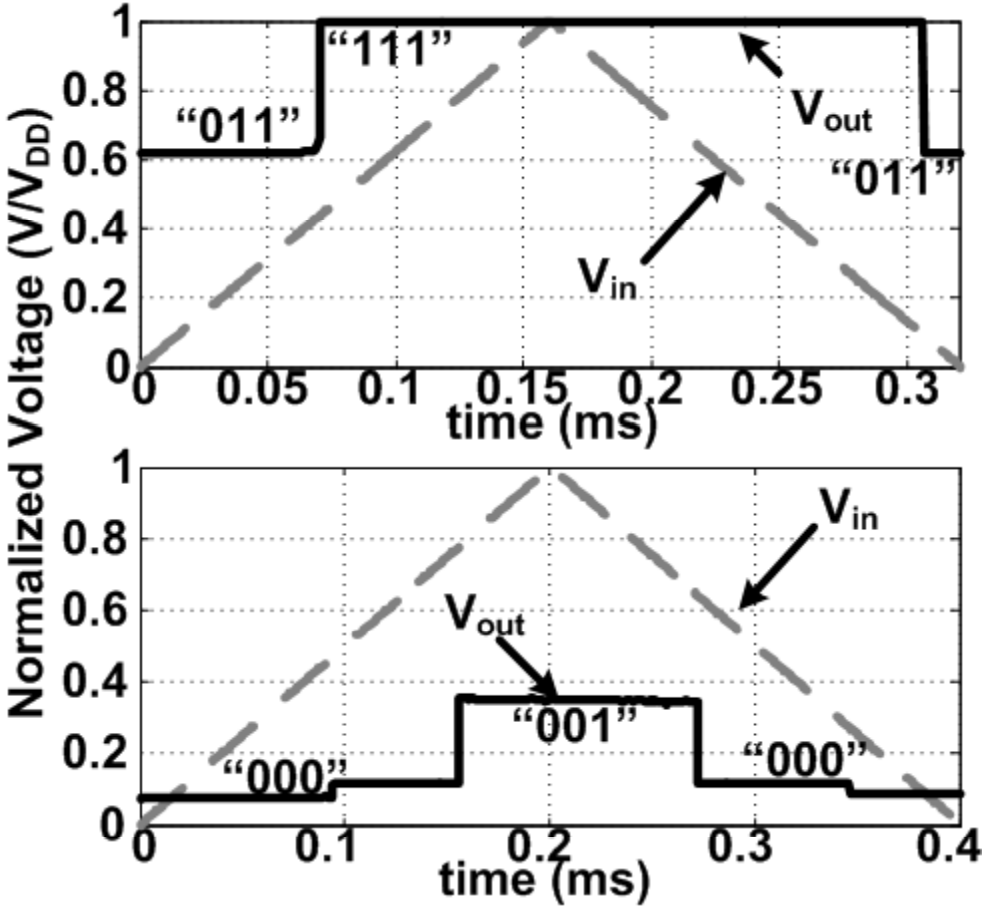
- Demonstrates propagate-generate-kill logic as a single complex gate

Measured DRAM Results

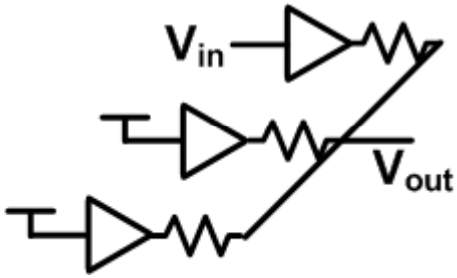


- Simultaneous read and write of DRAM
  - Read latency: $\tau_{mech,on} + \tau_{mech,off}$.

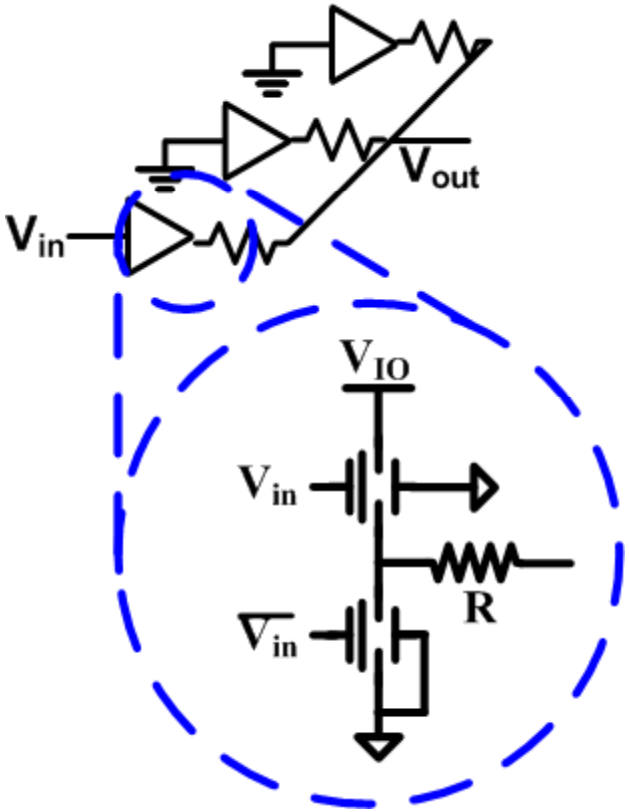
Measured DAC Results



Code = "Vin" 1 1



Code = 0 0 "Vin"



- Resistive divider based DAC
  - 2-bit thermometer coded output

Conclusions

- MEM switches offer a lower minimum E/op than CMOS
- Reliability of MEM switches improving
  - Demonstrated simple circuits
  - Can start to think about building more complex systems
- Next steps: scaling and improving device design
  - Realize potential energy-efficiency benefits over CMOS

Acknowledgements

- DARPA NEMS program
- BWRC Sponsors
- MIT CICS
- Focus Center Research Program (C2S2, MSD)
- NSF Infrastructure Grant #0403427