4.1 A Serial-Link Transceiver Based on 8GSample/s A/D and D/A Converters in 0.25μm CMOS

William Ellersick[1,3], Chih-Kong Ken Yang[2], Vladimir Stojanovic[1], Siamak Modjtahedi[2], Mark A. Horowitz[1]

[1]Stanford University, Stanford, CA
[2]University of California, Los Angeles, CA
[3]Analog Devices, Inc., Wilmington, MA

This 8GSymbol/s equalized transceiver is based on time-interleaved DACs and ADCs. The symbol time of 1 fanout-of-4 (FO-4) gate delay matches the speed of the fastest binary transceivers [2], while the ADCs and DACs support digital communication techniques to overcome wire losses, interference, and impedance discontinuities. The limitations of the relatively simple, fast converter circuits are digitally corrected. Inductors reduce low-pass filtering due to I/O capacitance.

The transmitter (Figure 4.1.1-right) consists of eight 8b time-interleaved DACs, each clocked with a phase-shifted 1GHz clock to generate 8 output pulses every clock cycle. Although the DACs are not designed to achieve 8bs of absolute accuracy (INL), the extra resolution reduces the step size and improves calibrated performance. The DACs use a current-steering architecture with 5 lower binary bits and 3 upper thermometer-encoded bits (Figure 4.1.2). The outputs of an array of current sources sums at the on-chip 50Ω termination resistor for a swing from V_{DD} to V_{DD}-1V. Each current source consists of 2 transistors in series [2], with the output swing adjusted by regulating the predriver V_{DD} to control the gate voltages. To interleave, each current source is enabled by the overlap of two 1GHz clocks that are phase shifted by 45°, with the bottom clock ANDed with the data. Similarly, the receiver (Figure 4.1.1-left) consists of eight 4b flash A/D converters each clocked with a phase-shifted 1GHz clock for an overall sample rate of 8GSample/s. Voltage offsets are digitally corrected by a 3b DAC in each comparator. Linearity is improved over the prior implementation [3] with better matching of clock coupling and larger devices in the offset correction DAC. Input bandwidth is improved with lower sampler load impedance, and the use of inductors.

To use inductors to distribute parasitic capacitances, the transceiver input and output each use 4 pads, each wired to two of the 8 time-interleaved ADCs or DACs. These pads can be shorted with short bondwires, or connected with inductors made from loops of bondwire. The inductors separate the parasitic converter capacitances, improving frequency response and impedance matching [4].

The multiple clock phases for the converters are generated from 2 PLLs locked to an external divided-by-4 reference clock running at 250MHz. Each PLL is based on a ring of 4 differential stages, with the 8 internal clock phases from the ring sent to digitally-controlled phase interpolators (phase resolution of $T_{symbol}/15$)[1]. The transmitter is provided with 16 independently adjusted clock phases, to control the start and end time of each of the 8 time-interleaved output pulses. The receiver uses 8 clock phases to establish the 8 time-interleaved sample times, and also dynamically adjusts the phase of the receive PLL feedback clock to align the 8 output phases with the received signal. The adjustments allow compensation for timing mismatches and delays between converters due to the inductors.

The calibration of the transceiver corrects for 3 effects: timing errors in the clock phases, DC errors or coupling in the transceiver, and parasitic filtering. The phases of the two clocks for each of the 8 time-interleaved DACs are adjusted for equal pulse width and spacing, reducing timing errors from 55ps to 12ps p-p. The sample time of each time-interleaved ADC is then aligned to the received pulse from the corresponding DAC.

Voltage errors are caused by random or systematic mismatches in the transistors, and reference ladder. Coupling causes additional noise due to clock switching. These coupling errors appear as different but fixed values at each symbol time and repeat over the period of the divide-by-4 reference clock (32 symbols). The transmitter compensates voltage errors by transmitting an anti-error sequence. Coupling errors of 36mV are reduced to 6mV (Figure 4.1.3), limited by the DAC DNL (Figure 4.1.4). The receiver compensates voltage offsets over 8 symbols by adjusting the offset correction DACs in each comparator [3], minimizing errors from 150 to 50mVp-p. 25mV of the residual error is due to the input clock noise that repeats every 32 symbols. The correction DAC quantization causes the remaining 25mV. Since the transmitter can compensate with higher resolution and longer sequence, the transmitter corrects both for transmitter errors and residual receiver errors, reducing the total to <20mVp-p.

The transmitter also equalizes the filtering effects of parasitics. Without using inductors, parasitics and finite transition rates limit measured bandwidth to 1.5GHz and 3.5GHz for transmitter and receiver respectively, leading to a channel bandwidth of 1.4GHz. However, the transceiver still operates at 8GSample/s (20dB of attenuation at Nyquist rate of 4GHz) by transmitting a high-pass pre-distorted sequence. The sequence is calculated using MATLAB and programmed into the on-chip transmit memory. To determine the equalizer weights, the pulse response of each DAC-ADC pair is measured. The responses vary between the time-interleaved converters due to gain errors from timing quantization and frequency response variations. A matrix based on interleaving each pulse response computes the weights using a variant of standard zero-forcing equalization algorithms. At 8GSample/s, a data eye height of 30mV is received. Equalization error is 35mV due to errors in measuring the pulse response.

Using inductors, the high frequency response of the transceiver improves significantly (Figure 4.1.5). The loss at 4GHz is improved by more than 10dB. The LC delays between pads are compensated by the clock phase adjustments. Coupling noise increases, but compensation reduces voltage noise from 180 to 20mVp-p. The equalizer adjusts for the increased frequency response variation. Transceiver operation with inductors is demonstrated with the pulse responses with and without equalization, and with the overlay of the received eyes of all 8 converters (Figure 4.1.6). With inductors, the eye becomes 60ps wide (122ps T_{symbol}) and 200mV high.

Acknowledgments:
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References:
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[2] Yang, C.K., et al, "A 0.5-μm CMOS 4.0-Gb/s Serial Link Transceiver with Data Recovery Using Oversampling," JSSC, May 1998.
[3] Ellersick, W., et al, "GAD: A 12-GS/s CMOS 4-bit ADC for an Equalized Multi-Level Link," VLSI Symp., Jun. 1999.
[4] Kleveland, B., et al, "Monolithic CMOS distributed amplifier and oscillator," ISSCC Digest of Technical Papers, Feb 1999.

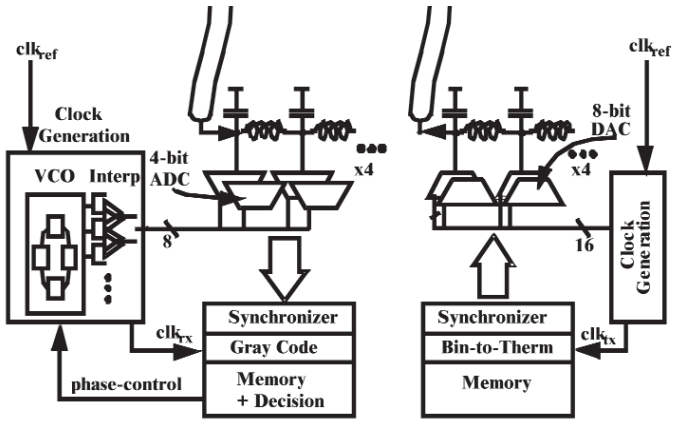

Figure 4.1.1: System architecture.

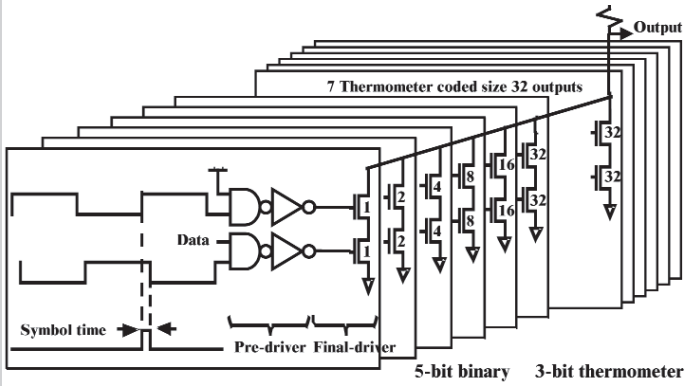

Figure 4.1.2: D/A converter implementation.

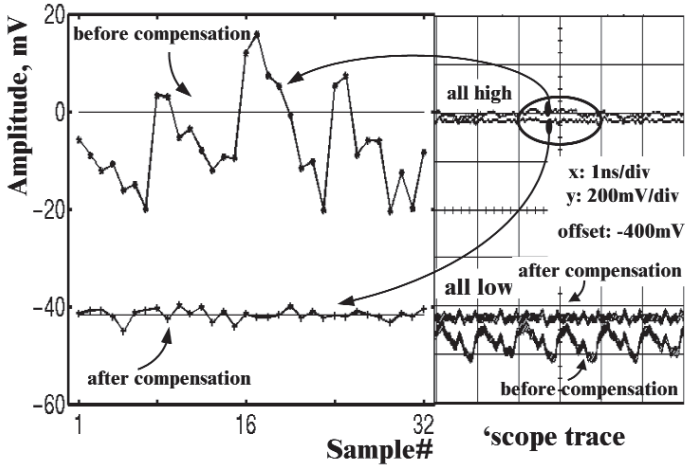

Figure 4.1.3: Transmitter DC coupling.

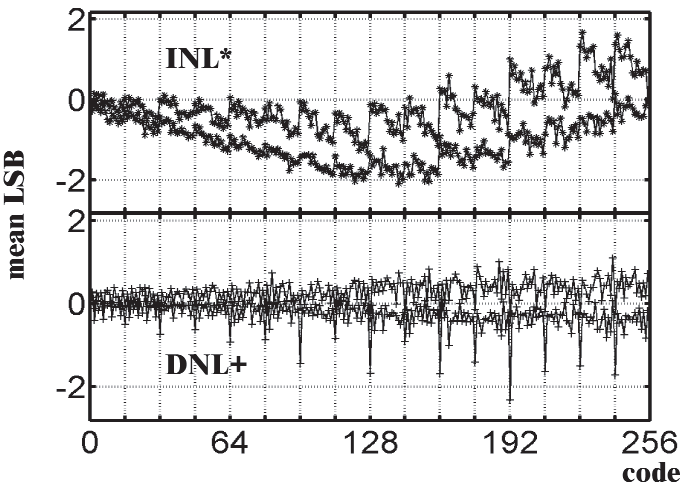

Figure 4.1.4: INL/DNL envelopes for DACs, LSB=2.2mV.

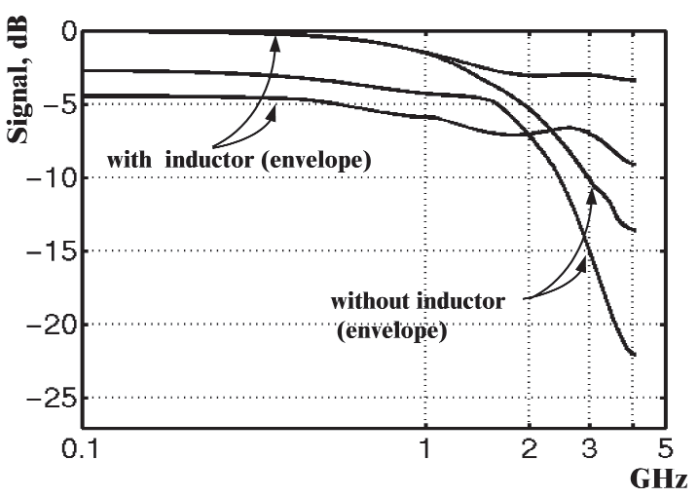

Figure 4.1.5: Transceiver frequency response w/ & w/o inductors.

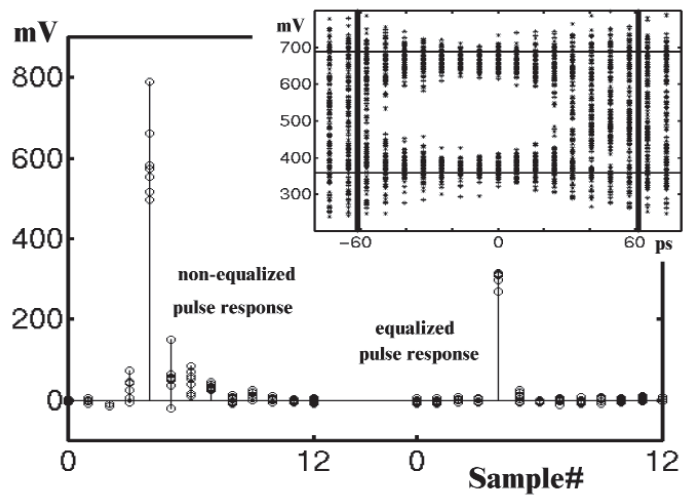

Figure 4.1.6: Transceiver pulse response and equalized eye.

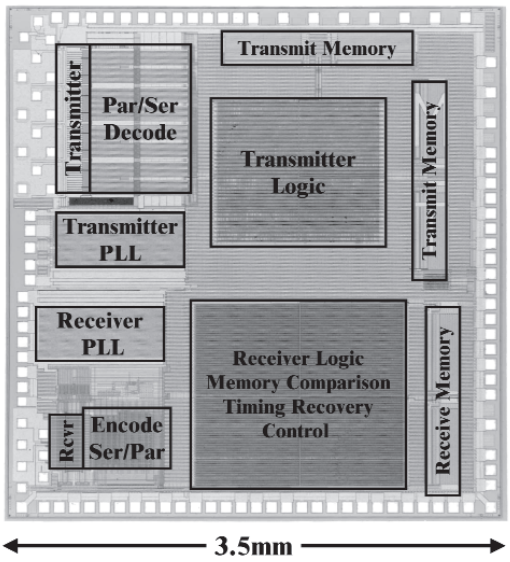

Figure 4.1.7: Chip micrograph.