A 1-10Gbps PAM2, PAM4, PAM2 Partial Response Receiver Analog Front End with Dynamic Sampler Swapping Capability for Backplane Serial Communications

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Abstract

A 1-10Gbps receiver analog front end in 0.13µm CMOS enables a SERDES cell for backplane serial communi-cations using differential PAM2, PAM4, or PAM2 partial response signaling with adaptive equalization. Dynamic sampler swapping and various built-in diagnostic capabil-ities enable receiver calibration and self-characterization with accuracy of < 0.4% UI in timing and < 2mV in voltage while receiving live data. Self-characterization results motivate modifications enabling communications at a BER of 10^{-15} with receiver sensitivity of +/-15mV.

Keywords: Analog front end, receiver, serial links, and backplane communications

Introduction

A 1-10Gbps receiver for backplane serial link communications has been designed in a 0.13um CMOS process. The receiver is part of an adaptively equalized transceiver system including 5 taps of transmit pre-emphasis and 10-20 taps of receiver decision feedback equalization (DFE) per serial link [1]. The system is configurable for communication using differential PAM2, PAM4, or PAM2 partial response signaling [1,2] in the high-speed forward direction simultaneously with common mode return-to-null signaling in the low-speed, reverse direction (for pre-emphasis adaptation) [3]. Example eye diagrams of these three signaling modes along with the decision thresholds required of the data samplers is shown in Fig. 1. These signaling and adaptive equalization options enable extremely low BER communication across diverse backplane traces [2]. Providing this flexibility along with built-in diagnostic and BER measurement capabilities requires a complex receiver architecture with analog front end (AFE) circuitry meeting an unusually diverse set of performance specifications. In this paper, we examine the receiver AFE architecture and circuit design choices, including provisions for dynamic sampler swapping which enables AFE calibration and margin testing while receiving live data. We also demonstrate the use of the receiver's diagnostic capabilities to characterize its performance and motivate architectural and circuit improvements for subsequent versions of the receiver.

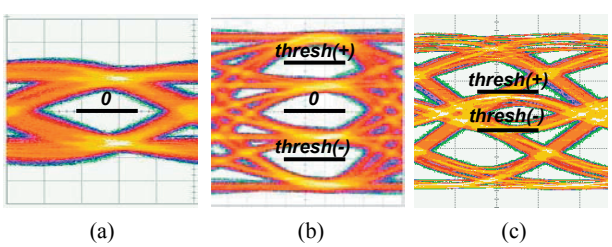

Fig. 1 Eye diagrams with data thresholds for the three signaling modes: (a) PAM2, (b) PAM4, and (c) PAM2 partial response.

Receiver AFE Architecture

The receiver AFE architecture is shown in Fig. 2. Because three signal samples are required per sampling point in order to operate in PAM4 mode, the receiver includes three data-sampling and three edge-sampling AFE slices per complementary clock phase for receiving data and edge samples from alternating input symbols (i.e. "even" and "odd" symbols). The edge-sampling AFE slices provide timing information for the transceiver's clock and data recovery circuit (CDR), while the data-sampling AFE slices provide data information to the deserializer datapaths, the DFE datapaths, and the CDR. An additional AFE slice (A-AFE) per clock phase driven by a separate complementary sampling clock is included for calibration, adaptation, and measurement capabilities. The A-AFE slices and some of the data and edge AFE slices (according to the selected signaling mode) can be powered down to save power.

Control of the 14 AFE slices' sampling instances and decision threshold voltage levels are key features of this receiver architecture. While the three independent sampling clocks are normally slaved together according to CDR timing updates, the relative timing between each of the three clocks is fully register-adjustable in increments of $1/256^{th}$ of a symbol time unit interval (UI). A single 8-bit,

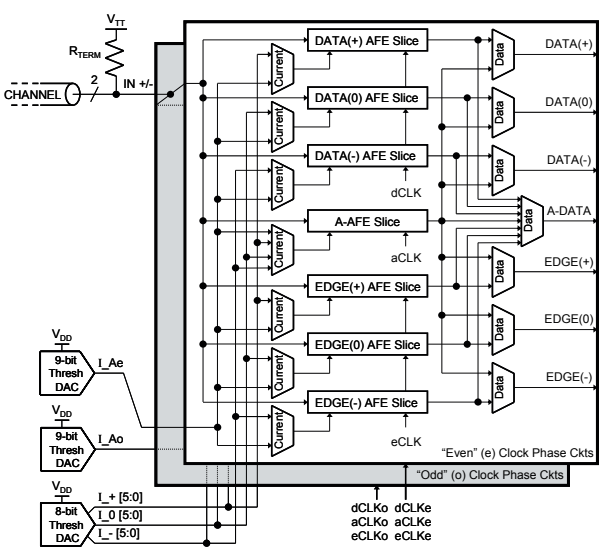

Fig. 2 Receiver AFE architectural block diagram showing options for multiplexing threshold DAC currents and sampled bitstreams.

multi-output differential current DAC sets the positive, negative, and zero-level decision thresholds of the 12 edge and data AFE slices, allowing the setting of these decision thresholds over a 9-bit (+/- 8-bit) differential range. The two A-AFE slices have dedicated 9-bit differential current DACs that enable independent roaming throughout this voltage space.

The fully independent voltage and timing (V/T) control of the A-AFE slices relative to the edge and data AFE slices enables the recovery of input signal level information for equalizer adaptation and for edge and data AFE threshold determination as described in [1]. This A-AFE V/T control coupled with associated test circuitry is also used to operate the receiver as an equivalent time oscilloscope for capturing repeating input waveform patterns as seen by the AFE circuits themselves. The test circuitry keeps track of the percentage of ones sampled by the A-AFEs at a given V/T point in the repeating pattern. The V/T coordinates are then incremented and more sampling statistics taken. Recognizing that the V/T points having close to 50% ones density form the trajectory of the waveform through the V/T space, these two steps are repeated until the waveform can be drawn. Information about the system's timing and voltage noise characteristics can also be determined from the sampling statistics taken throughout the V/T space by examining the spread of the ones density. This diagnostic capability is profoundly useful for input signal and receiver characterization, as shown in the "Performance Characterization" section below.

The receiver architecture also includes multiplexers for the threshold DAC currents and multiplexers for the AFE slice output data bitstreams. These multiplexers allow for dynamic swapping of each A-AFE slice with any of the other 6 AFE slices in its clock phase, even while receiving live data. When dynamically swapping AFE slices during live data operation, a make-before-break procedure is employed to prevent generating bit errors in the data or edge bitstreams. For example, to swap the odd A-AFE slice with the odd DATA(+) AFE slice, the A-AFE clock timing is set equal to that of the data AFE slices. The A-AFE decision threshold is then set equal to that of the DATA(+) AFE slice by selecting for the A-AFE a threshold current from the 8-bit multi-output DAC that is a copy of the current provided to the DATA(+) AFE. Now that both AFE slices are operating at the same V/T point, the DATA(+) bitstream multiplexer is set to first pass data from both slices and then pass data only from the A-AFE slice. This prevents bit errors which might occur if the DATA(+) bitstream multiplexer were switched directly from the DATA(+) AFE to the A-AFE. The DATA(+) AFE is now free to receive the threshold current from the odd phase 9-bit DAC and provide sampled data to the A-DATA output.

This swapping capability enables live voltage margining (shmooing) of any of the 12 data and edge AFE slices. By using the 9-bit threshold DAC to adjust its decision threshold, the swapped AFE slice's output bitstream can be compared to that of another AFE slice operating at the same timing instance for margin testing such as finding the height of a data eye or determining the sensitivity of the swapped sampler. Alternatively, the swapped AFE slice's output bitstream can be evaluated to search for a desired level (e.g. for calibration to a desired level). This evaluation can include data filtering to identify when the input signal is at the desired level so that the AFE slice's output bits are meaningful. For example, to test for the highest PAM4 level using a swapped edge AFE slice, the previous and succeeding symbols must both be 11. The value of sampled data from the swapped AFE slice then indicates if its threshold is too high or too low.

By moving an A-AFE slice throughout the V/T space while comparing its bitstream to a selected data bitstream, the receiver architecture can be used for margin testing in all three signaling modes to determine the effective eye openings as a function of BER. For margin measurement of PAM2 partial response data eyes, data filtering circuitry is provided for selecting only the appropriate data bits for comparison. For example, when margining the upper eye, only data symbols for which the previous symbol was a "1" should be used. The right-hand portion of Fig. 3 shows BER margin measurements obtained in this way for an adaptively equalized 6.4Gbps PAM2 partial response input signal. The figure also shows the signal's corresponding eye diagram measured at the input pins of the receiver.

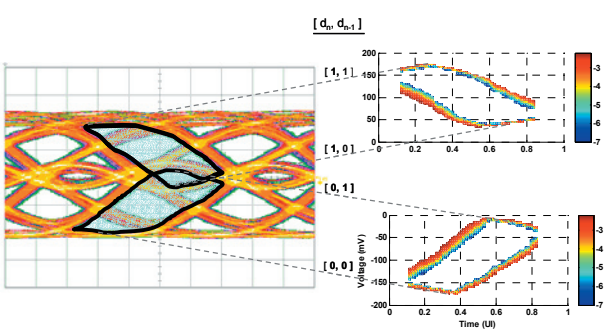

Fig. 3 Receiver operation for 6.4Gpbs PAM2 partial response signaling through a 26" FR-4 bottom trace channel: (a) Measured oscilloscope eye at the receiver input pins. (b) BER shmoo plots measured using the receiver's on-chip diagnostic circuitry.

AFE Circuit Design

As illustrated in Fig. 4, each AFE slice includes a double-mismatched differential pair preamplifier with tail current steering between the two mismatched pairs in order to set the differential voltage threshold of the AFE slice [4]. The preamplifier is followed by a sense-amp based sampler. The net offset of each AFE slice is compensated

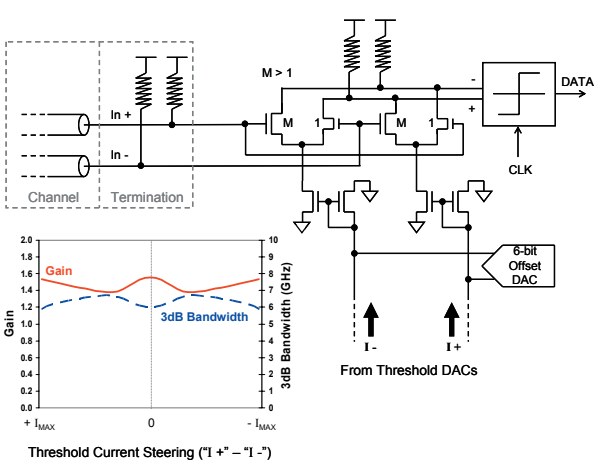

Fig. 4 AFE slice including preamplifier and offset cancellation DAC. Plot of simulated preamplifier gain and 3dB bandwidth at decision threshold as a function of threshold current setting.

by a dedicated 6-bit DAC which provides an offset-compensating output current that combines with the current from one of the threshold DACs to bias the preamplifier and set its effective differential input offset voltage. This arrangement both cancels the inherent offset of each AFE slice and sets its decision threshold. The magnitude of the total preamplifier bias current (i.e. the sum of the currents from the threshold DAC and the currents from the offset DAC) is set by a bias circuit that uses a replica preamplifier and DACs to fix the full-scale differential preamplifier decision threshold at +/-485mV.

Since equalizer adaptation and sampler swapping rely on all AFE slices having similar characteristics regardless of their threshold settings, the following design choices were made. The preamplifier with adjustable threshold was selected because it applies the desired AFE slice decision threshold and offset compensation to the input signal while maintaining a constant common mode voltage at the sampler inputs. This minimizes the effect of input common mode on the AFE slices' sensitivity, including any common-mode to differential-mode conversion from the backchannel to the forward channel [3], because the preamplifier has less common-mode sensitivity than the sampler. This also avoids the addition of offset correction directly at the sampler. However, this arrangement shifts most of the AFE design challenges to the preamplifier. Fortunately, its simple, symmetrical structure performs well, having a relatively linear operation. The sampler's switching point corresponds to equal current steering between the two preamplifier loads and equal input voltages to the sampler, conditions at which the preamplifier has maximum gain and linearity, and the sampler has maximum sensitivity. Furthermore, at this switching point the preamplifier shows a relatively small variation in signal gain and 3dB bandwidth as a function of the AFE slice's threshold, as shown by the simulated curves in Fig. 4.

Simulations predicted approximately 4 LSBs of systematic INL in the current steering to threshold voltage transfer function of the preamplifier itself. This simulated transfer function as well as a measured transfer function are shown in Fig. 5(a). The INL of the measured curve is shown in Fig. 5(b) indicating a total INL of 6.7 LSBs and DNL of 5.6 LSBs due to additional DAC non-linearity. Despite these modest linearity results, the linearity of this transfer function affects only the linearity of the control of the AFE decision thresholds, and not the sensitivity of the AFE slices or the receiver itself.

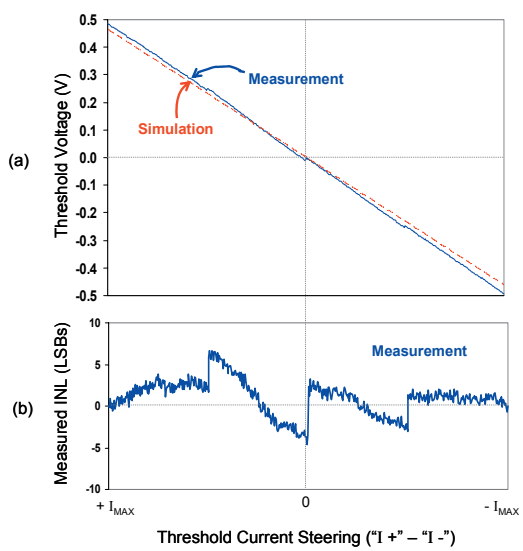

Fig. 5 Preamplifier characteristics: (a) Measured and simulated transfer function of preamplifier current steering to AFE sampling threshold. (b) Measured INL.

Performance Characterization

The receiver AFE was integrated with the rest of the transceiver into a 1mm x 1mm SERDES cell [1,3], and four instances of the cell along with other SERDES and switching circuitry were fabricated onto a test chip. The flexible diagnostic capabilities of the receiver were then used to characterize several aspects of the receiver's performance, including offset correction, sensitivity, and systematic noise, as illustrated in Fig. 6. By looking at the mean of the distribution of ones at the A-AFE output as a function of input signal differential DC offset at zero threshold setting as shown in Fig. 6(a), the effectiveness of the offset cancellation was confirmed to be within 1 LSB (2mV) of the DAC resolution, meeting design specifications.

The cumulative distribution functions (CDFs) of the A-AFE output were compared as a function of DC offset, for zero and large threshold settings, as shown in Fig. 6(a)-(b). The spread of these statistical representations of the receiver's sensitivity was unexpectedly larger (i.e. the slope of the curves in Fig. 6(a)-(b) was unexpectedly smaller) for threshold voltages away from zero. The CDFs in Fig. 6 resemble chopped Gaussian distributions with a difference in variance of 0.85mV rms due to the threshold setting.

To investigate this unexpected reduction in sensitivity, the waveform capture capability was used to margin the A-AFE across the V/T space to measure the effective threshold for the A-AFE as a function of time, relative to the edge and data sampling times. Comparing the magnitude and frequencies of the threshold variation for both zero and large threshold settings shows a stronger presence of various clock signatures at the large threshold, as can be seen in Fig. 6(c)-(d). This verifies that as the threshold level increases, the preamplifier becomes less balanced and allows more noise to couple to its output.

This effect was expected for transmitter-induced noise, input common-mode noise, and sampler kick-back noise as

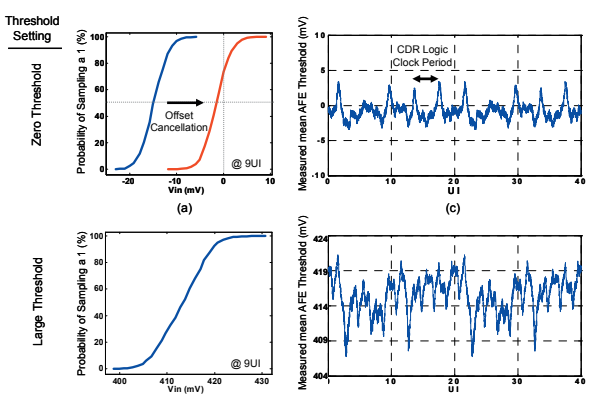

Fig. 6 Receiver self-characterization measurements using the waveform capture capability showing (a) receiver sensitivity at zero threshold before and after offset cancellation, (b) receiver sensitivity at large threshold, and power supply noise coupling into the AFE slice at (c) zero threshold and (d) large threshold.

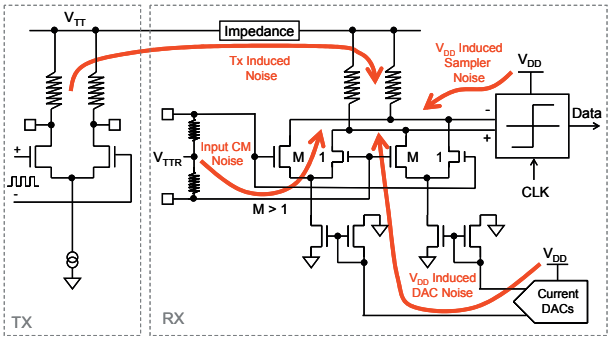

Fig. 7 Noise injection paths in an AFE slice.

illustrated in Fig. 7. However, the sensitivity degradation as a function of threshold setting was much worse than expected from sampler kick-back noise given that the adjacent transmitters as well as the common-mode backchannel transmitter were shut off in this test, making these noise sources negligible. Therefore, the presence, identity, and magnitude of core logic clock frequencies in Fig. 6(c)-(d) indicated the existence of additional noise paths. Simulation confirmed a significant unanticipated noise path to the AFE slices from the DACs, which were powered from the core supply as shown in Fig. 7.

Although successful operation of the transceiver cell was demonstrated across multiple backplane links operating from 1-10Gbps, its sensitivity performance was limited by the aforementioned noise path. The receiver was designed for +/- 15mV sensitivity at a BER of 10^{-15}, but calculations including this noise path predicted a degraded sensitivity at this BER level of +/-23mV. This value correlated well with measured results. The simulated current consumption of the receiver AFE circuits operating at 6.25Gbps is 25.6mA in PAM2 mode, 29.5mA in PAM4 mode, and 34.1mA in PAM2 partial response mode.

Design Improvements

The self-characterization performed using the built-in diagnostic capabilities of this receiver motivated two major architectural changes to the receiver AFE. These changes, as shown in Fig. 8, are being incorporated into the next revision of the SERDES cell.

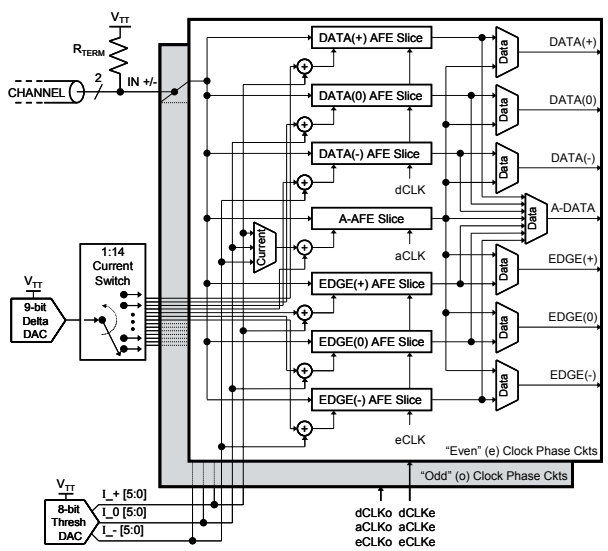

Fig. 8 Architectural block diagram of a modified receiver AFE incorporating modifications suggested from measurements taken using the receiver's built-in measurement capabilities.

The first change was motivated by the discovery of the significant noise path from VDD through the threshold and offset DACs. This problem is being addressed by moving the DACs to the VTT supply. While measurements show this supply to be an order of magnitude quieter than VDD, the change comes at the cost of higher power consumption, as VTT is 1.25V compared to 1.0V for VDD.

The second change was motivated by the realization that mis-matches in the current levels provided from the three threshold DACs led to unrecoverable calibration errors. In the architecture of Fig. 2, the 12 data and edge AFE slices are calibrated while using a current from a 9-bit A-AFE threshold DAC but are operated while using currents from the 8-bit multi-output DAC. The one sigma mis-match in effective AFE decision threshold due to this current swapping was 14mV at zero threshold.

To eliminate this issue, the two 9-bit threshold DACs have been replaced by a single 9-bit "Delta" DAC and a 1:14 current switch, as shown in Fig. 8. In this modified arrangement, each AFE slice always receives its own dedicated threshold current, allowing for the removal of all the current multiplexers except for the one supplying the A-AFE slice (since this slice must select between a positive, negative or zero-level threshold current from the 8-bit DAC for swapping). The Delta DAC has push-pull current outputs for modifying the decision threshold of the connected AFE slice relative to the level set by the 8-bit threshold current. Calibration is performed by applying the Delta DAC to each AFE slice and using it to measure two signal levels at equal positive and negative difference from the level to which the calibration is being performed. The associated offset DAC is adjusted until equal magnitude, opposite sign Delta DAC codes are required to sample at the two levels.

Simulations incorporating these and other minor changes into a newer version of the receiver AFE predict a receiver sensitivity of +/-15mV at a BER of 10^{-15}, a performance level enabling reliable communication across many more backplane channels.

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