

Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk Si CMOS Processes

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Abstract: A novel post-processing fabrication technique, based on XeF₂ etching, has been developed to locally remove the silicon substrate beneath polysilicon waveguides, enabling integration of low-loss strong-confinement microphotonics into standard bulk-silicon CMOS process flows.

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1. Introduction

The recent advances in strong-confinement microphotonic devices, allowing for higher performance and denser integration, have made photonics attractive to the information processing sector in addition to the telecom industry [1-4]. This has led to the emergence of electronic-photonic integrated circuits that utilize electronic and photonic devices together in a synergistic way to achieve better performance than with current technology. However, present approaches to integrated electronic-photonic components and systems involve significant customization of the bulk CMOS fabrication process flow to support low-loss photonic devices, which compromises electronic performance (including thermal issues), throughput, and cost. Some examples of these customizations include thick low-index cladding layers, silicon-on-insulator technology and electron-beam lithography [3-5]. While tolerable for some applications, these customizations are not acceptable for high-performance, high-volume devices such as processors and DRAM. In order to integrate photonics monolithically with these devices one must be able to work completely within the constraints of commercial bulk CMOS process flows, which means utilizing the given material layers, thicknesses, processing steps and tools, with the addition of minimal post-processing steps that meet the requirements of back-end processing. Enabling monolithic integration of photonics into mainstream bulk CMOS promises major implications for high-performance circuit technology.

It is possible to fabricate strong-confinement waveguides out of the polysilicon layer (used to form both transistor gates and poly-resistors) when deposited above the shallow trench isolation (STI) layer, working completely within the constraints of commercial bulk CMOS process flows [5]. Without post-processing, such waveguides will have a propagation loss of the order of 1000 dB/cm since the STI layer (<400 nm of oxide) alone is not thick enough to prevent the optical mode guided by the silicon core from “tunneling” (leaking) into the high-index Si substrate. In order to eliminate this leakage loss it is necessary to remove the Si substrate that is within ~5 μm, radially in the cross-sectional plane, of the photonic device (Fig. 1).

In this study, we developed a novel post-processing technique using XeF₂ to locally remove the silicon substrate to create an air tunnel beneath polysilicon waveguides. The presence of this air tunnel eliminates propagation loss due to leakage into the substrate. Removing the substrate locally minimizes impact on the electrical, thermal, and mechanical performance characteristics of the integrated (electronic) circuits. XeF₂ gas is used as the silicon etchant

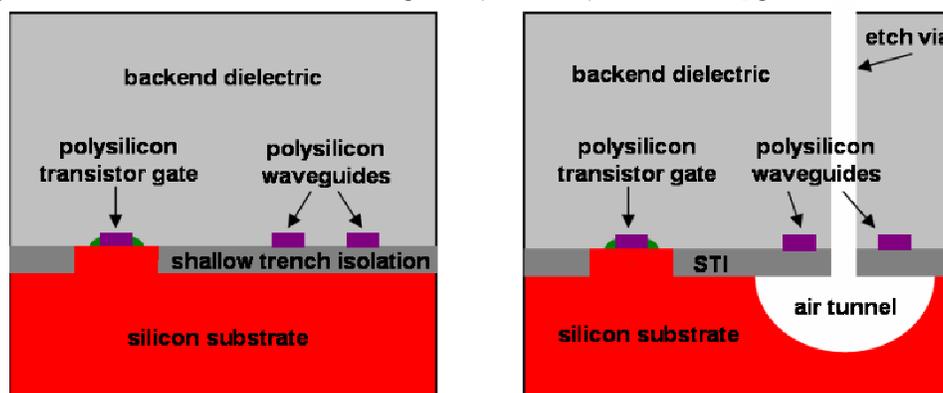


Fig. 1. (left) Sketch of a standard bulk CMOS stack up with fabricated polysilicon waveguides. (right) Sketch after locally removing silicon substrate to eliminate propagation loss due to substrate leakage.

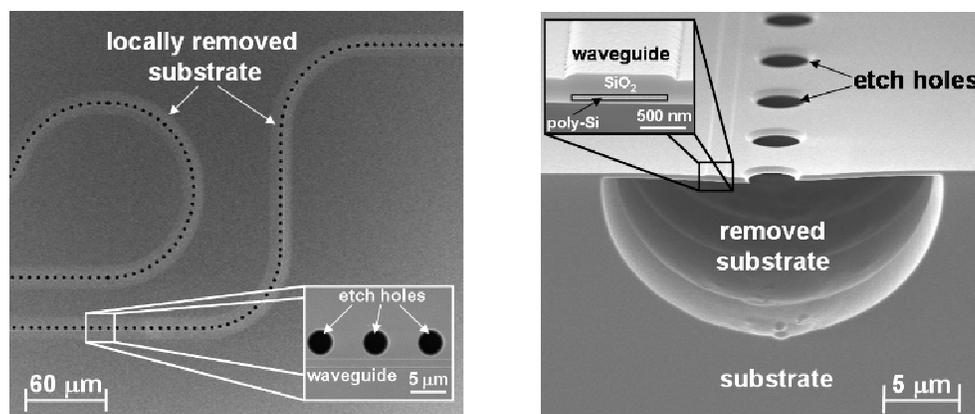


Fig. 2. (left) Top and (right) cross-sectional scanning-electron micrographs of polysilicon waveguides with locally removed substrate. The etch holes are 3 μm in diameter spaced 8 μm apart and the substrate has been removed to depth of 10 μm .

because it is completely isotropic, it can undercut large areas without the stiction problems characteristic of wet etches, and has a high silicon etch-rate selectivity over SiO_2 (1000:1) [6]. We have used this method to fabricate waveguides using polysilicon-on-oxide films supplied by a major semiconductor manufacturing company. The propagation loss of these waveguides was measured to be approximately 10 dB/cm at 1550 nm, which is thought to be due to a combination of material absorption, and scattering from the surface and sidewall roughness.

2. Fabrication method and results

Polysilicon films, 80 nm thick, were deposited on 50-nm-thick thermally grown SiO_2 . Using contact lithography, straight and curved waveguides were patterned into a novolak photoresist. These patterns were then transferred into the polysilicon layer using a Cl_2 based reactive-ion etch, taking care not to etch through the 50 nm thick SiO_2 layer. The photoresist was then stripped and oxide was deposited over the polysilicon waveguide using plasma-enhanced chemical-vapor deposition (PECVD). The sample was then annealed at 1000°C for 60 minutes to remove pinholes in the PECVD oxide layer. A second contact lithography step was performed to open etch holes along side the waveguides. The PECVD and thermal oxide layers were cleared from the etch holes using a buffered-oxide etch to expose the silicon substrate. The sample was then placed in a XeF_2 etcher and was subjected to multiple pump-etch-pump cycles until the substrate was locally removed underneath the waveguides. The photoresist was then removed with an oxygen plasma. Top view and cross-sectional view scanning-electron micrographs of the fabricated waveguide structure are shown in Fig. 2. The propagation loss of the fabricated waveguides was measured by the cut-back method using paperclip-like waveguide structures with a progression of lengths (Table 1). These measurements clearly show that this method of localized substrate removal is successful in eliminating the order of 1000 dB/cm propagation loss caused by leakage into the proximate silicon substrate. The remaining propagation loss of 10 dB/cm at 1550 nm is thought to be due to a combination of material absorption, and scattering from the surface and sidewall roughness. This same post-processing technique, with slight modification to the method for clearing the etch holes, can be applied to the fabrication of microprocessor chips.

Table 1. Propagation Loss for Poly-Silicon Waveguides

Wavelength (nm)	1260	1310	1450	1520	1550	1600
Loss (dB/cm)	16	8	9	12	10	9
Error (dB/cm)	+/-6	+/-5	+/-5	+/-4	+/-4	+/-4

3. Acknowledgments

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References

- [1] M. Lipson, "Silicon photonics: An exercise in self control", *Nature Photonics* **1**, 18-19, (2007)
- [2] M.A. Popović, T. Barwicz, *et al.*, "Strong-confinement microring resonator photonic circuits (Invited)," in Proceedings of the 20th Annual Meeting of the IEEE Lasers and Electro-Optics Society (LEOS), Lake Buena Vista, Florida, Oct. 2007, paper TuCC3.
- [3] L.C. Kimmerling *et al.*, "Electronic-photonic integrated circuits on the CMOS platform," in Proceedings of SPIE **6125**, 612502, 2006.
- [4] C. Gunn, "Fully Integrated VLSI CMOS and Photonics 'CMOS Photonics'," in 2007 IEEE Symposium on VLSI Technology, pp.6-9, 2007.
- [5] T. Barwicz *et al.*, "Silicon photonics for compact energy-efficient interconnects," *J. Opt. Netw.* **6**, 63-73, (2007).
- [6] J.S. Orcutt *et al.*, "Demonstration of the first electronic photonic integrated circuit in a commercial scaled bulk CMOS process," submitted to the Conference of Lasers and Electro-Optics (CLEO), San Jose, California, May 2008.
- [7] P.B. Chu, *et al.*, "Controlled pulse-etching with xenon difluoride," *Solid State Sensors and Actuators* **1**, 665-668 (1997).