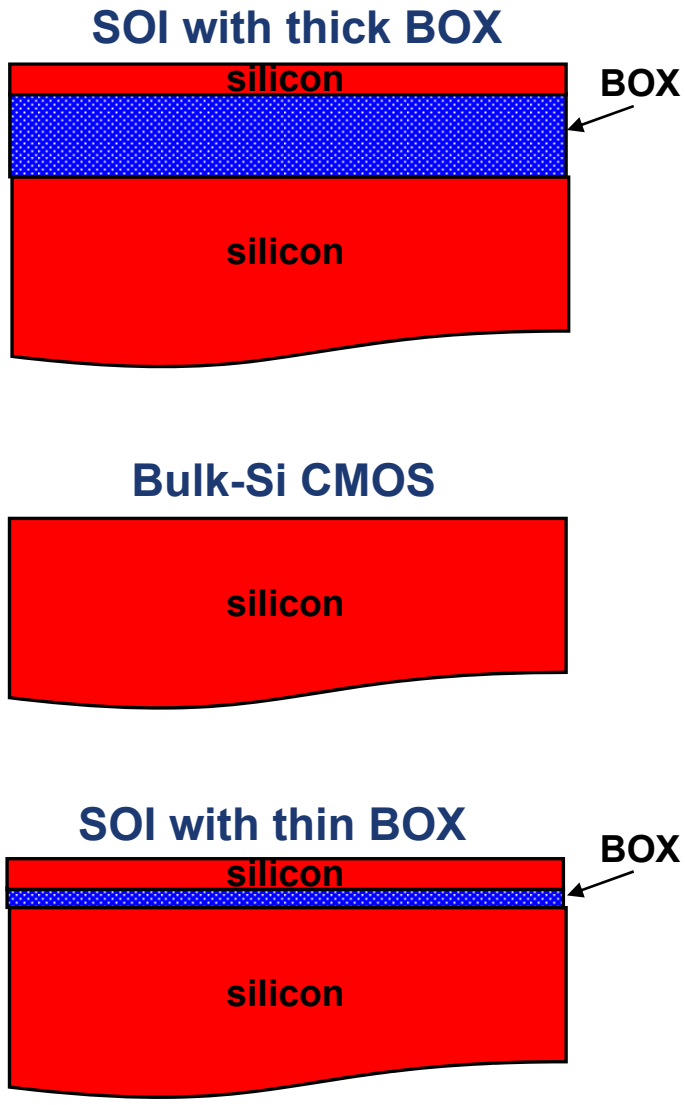
Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk-Si CMOS

Charles W. Holzwarth, Jason S. Orcutt, Hanqing Li,
Miloš A. Popović, Vladimir Stojanović, Judy L. Hoyt
Rajeev J. Ram, and Henry I. Smith

Research Laboratory of Electronics
Massachusetts Institute of Technology, Cambridge MA, USA

CMOS Compatible → CMOS Enabled

- Why CMOS compatible?
  - preexisting tools and techniques
  - integrate electronics and photonics
- Current Si photonics
  - SOI with thick buried oxide (BOX)
  - customized processing
- Mainstream VLSI
  - bulk-Si CMOS
  - same material stack
  - transparent process flow
  - need enabling technology

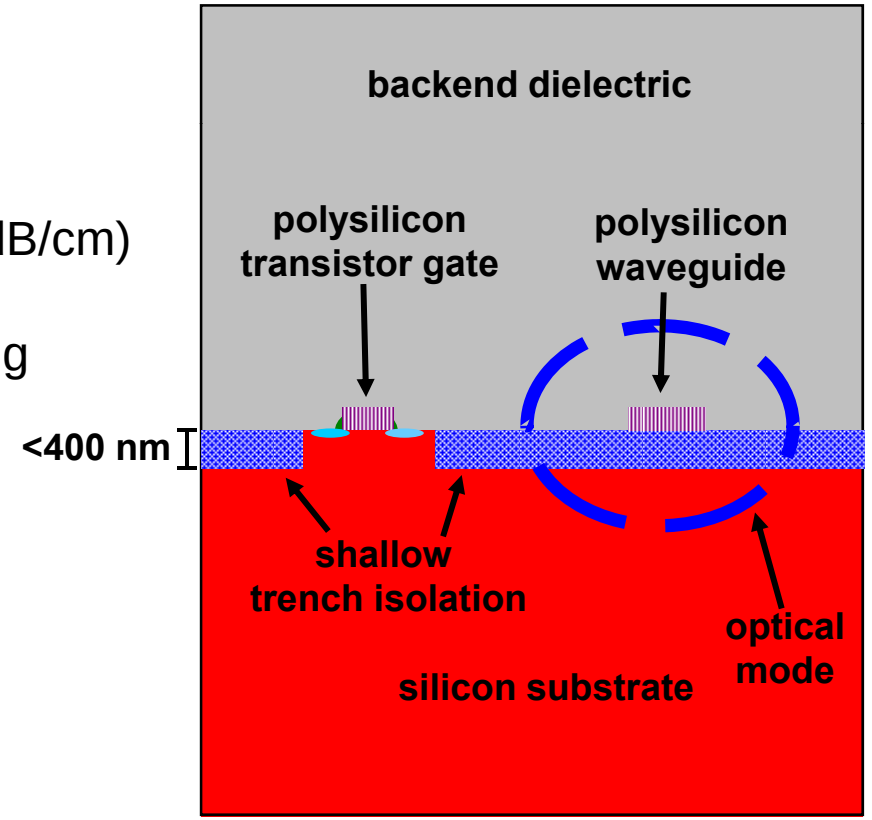


Strong-Confinement (SC) Photonics in Bulk CMOS

- Photonic integration: bulk CMOS
  (J.S. Orcutt *et al.* CTuBB3)
  - poly-Si on shallow trench isolation
  - no production changes

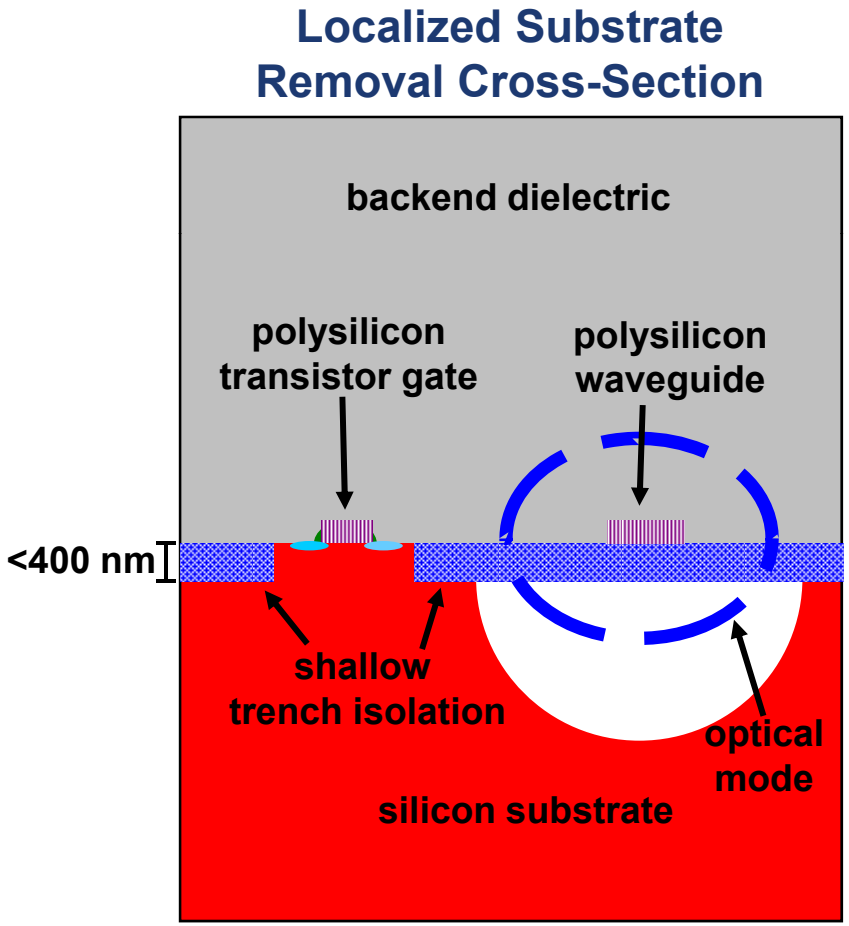
- Problems
  - leakage to the substrate (~1000 dB/cm)
  - material absorption (?? dB/cm)
  - limited to post-backend processing

Bulk CMOS Electronic-Photonic Integration Cross-Section



Localized Substrate Removal

- Locally remove the substrate
  - eliminates leakage to substrate
  - does not affect electronics
  - mechanically stable
- Use XeF_2 isotropic etch
- Is this allowed in CMOS?
  - post-backend processing
  - low temperature
  - does not affect the electronics

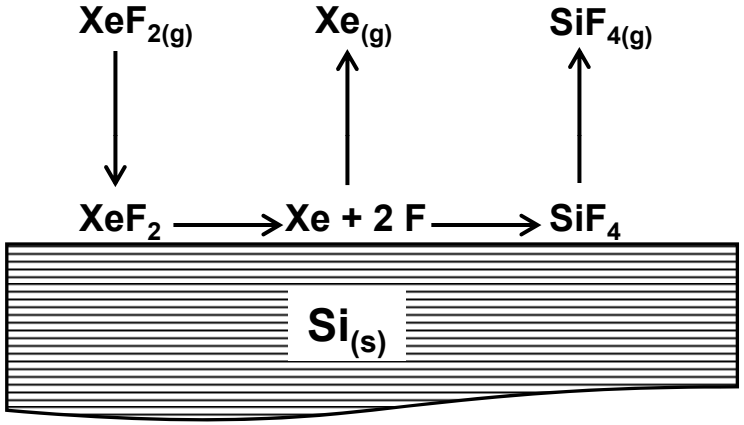


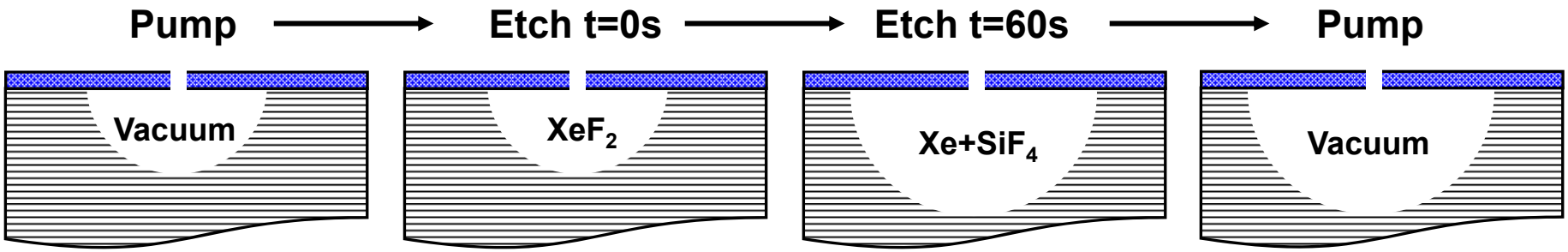
How Does XeF_2 Work?

- Plasmaless dry etch
  - 100% chemical; isotropic
  - selectivity >1000:1 for SiO_2, Si_3N_4, polymers, etc.
  - no stiction

$$2\ XeF_{2(g)} + Si_{(s)} \rightarrow 2\ Xe_{(g)} + SiF_{4(g)}$$

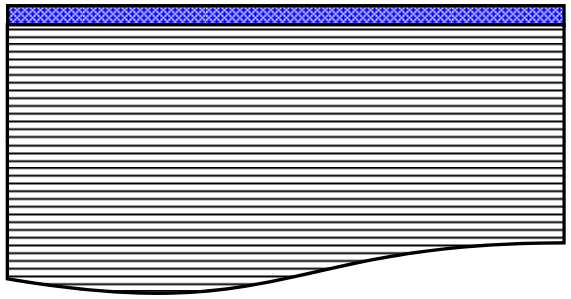
- Pulse etch method
  - pump/etch/pump
  - large undercuts
  - etch rate controlled by aperture size



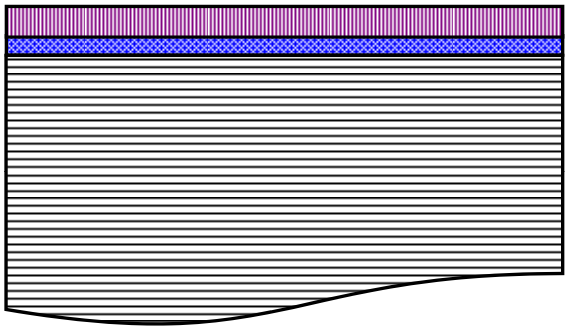


Localized Substrate Removal: Process Flow

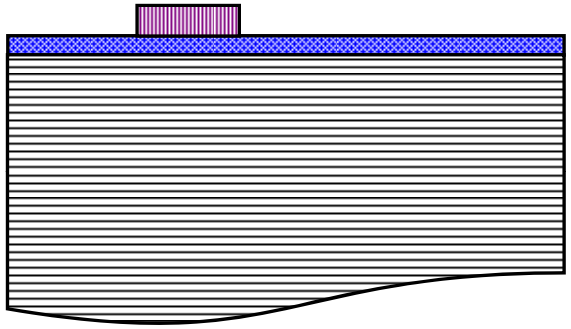
1. Grow 50 nm SiO_2



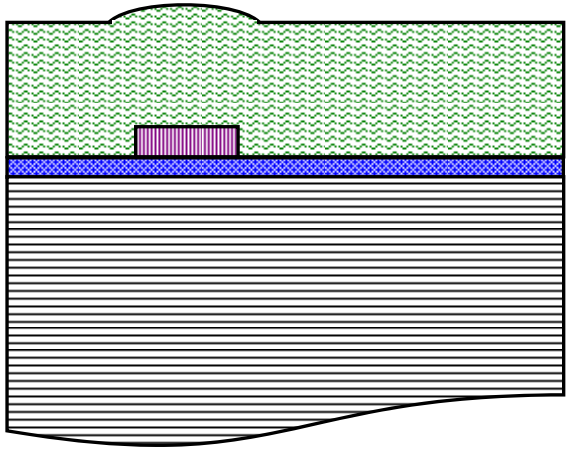
2. Deposit 80 nm poly-Si
(Supplied by Texas Instruments)



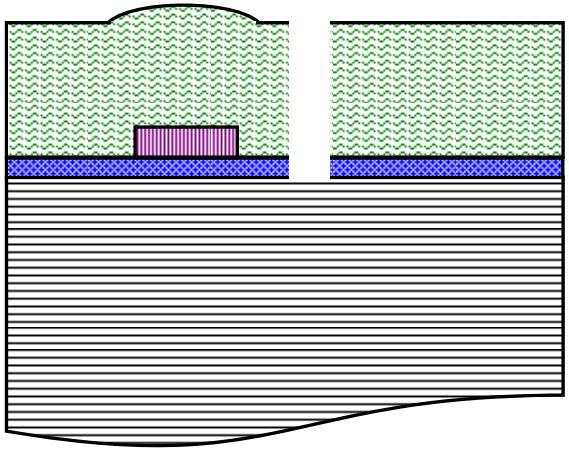
3. Define waveguide core



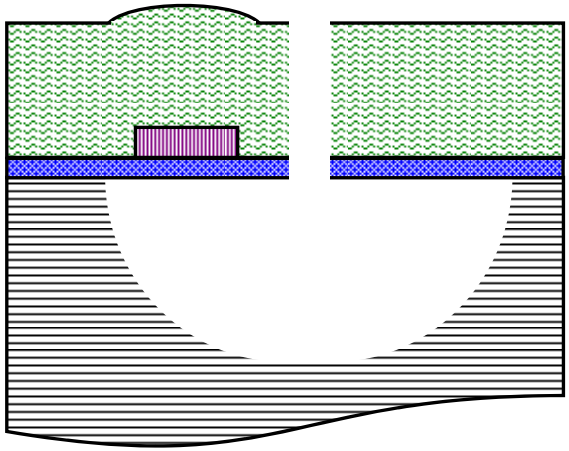
4. Deposit 450 nm SiO_2



5. Define etch hole



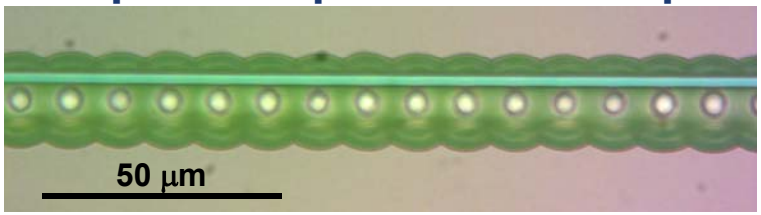
6. Locally remove substrate



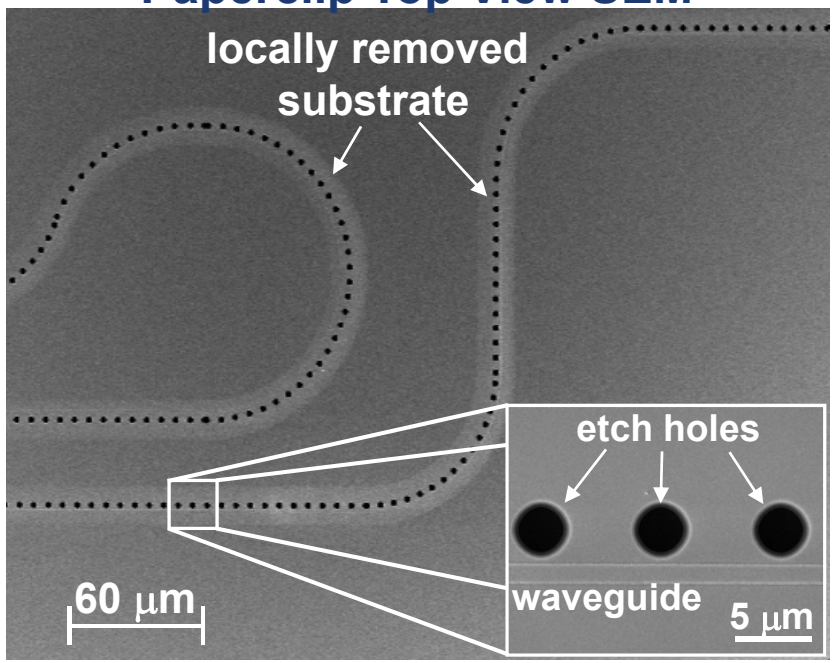
Fabricated Devices

- Undercut arbitrary shapes
  - > 1 cm in length
  - optical monitoring
- Mechanically Stable

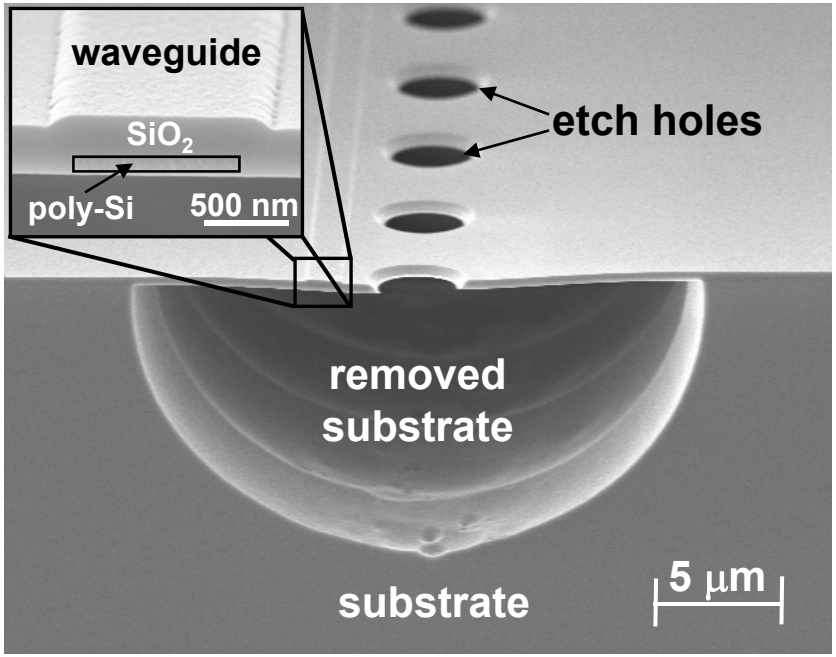
Top View Optical Microscope



Paperclip Top View SEM

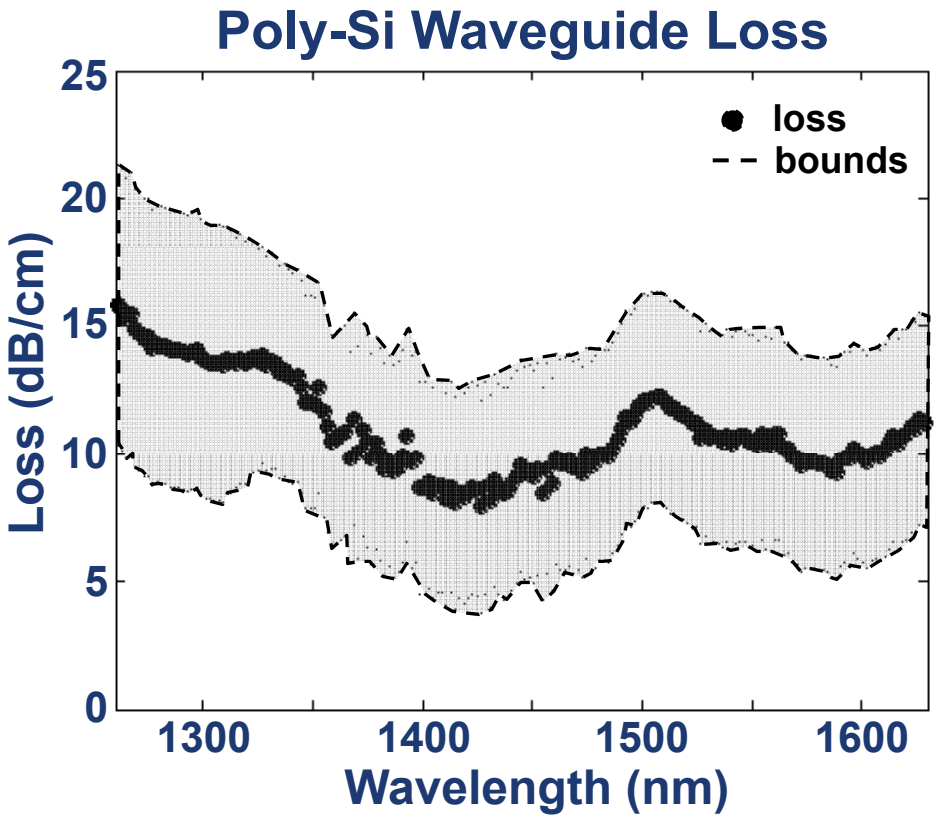


Cross-Section SEM



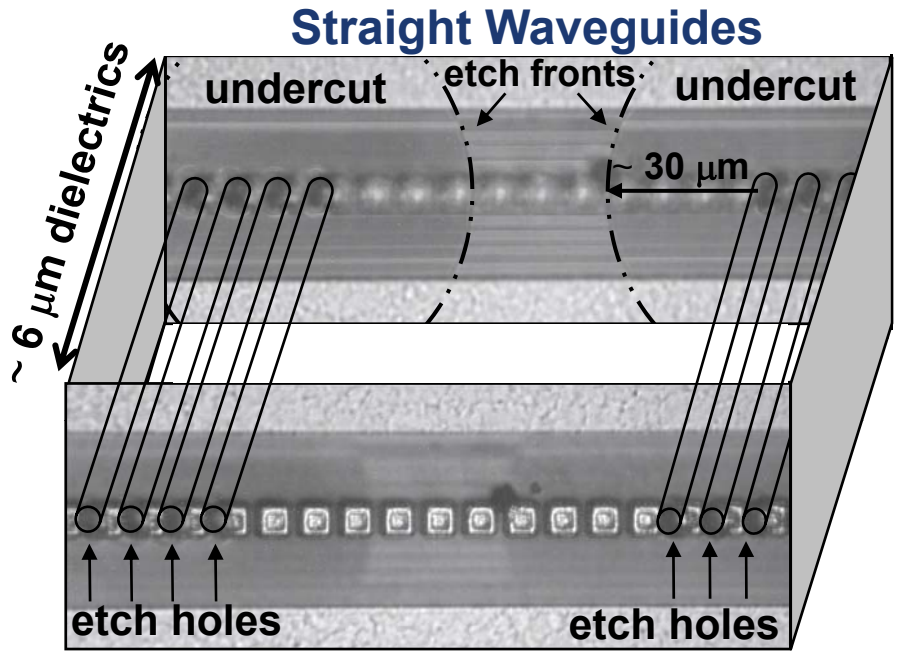
Measured Results

- Loss results
  - broadband
  - paperclip structure
- Localized removal
  - no leakage
  - ~1000 → ~10 dB/cm
- Reasons for loss
  - surface/sidewall roughness
  - material absorption
  - facet variation
- Suitable for VLSI applications

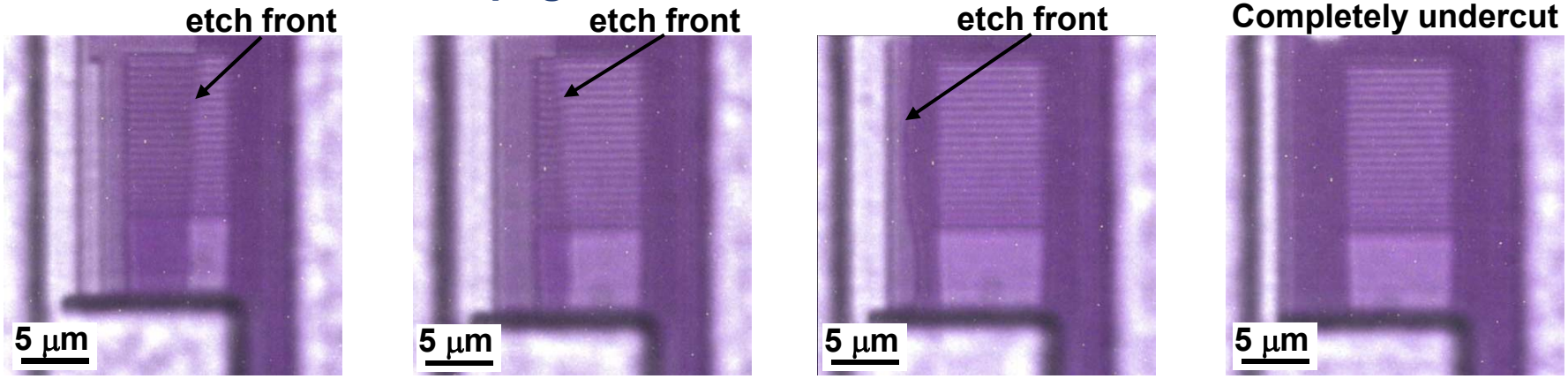


Preliminary Experiments on CMOS Chips

- Etch dielectrics
- Mechanically stable
  - low stress
  - >80 μm widths
- Testing underway



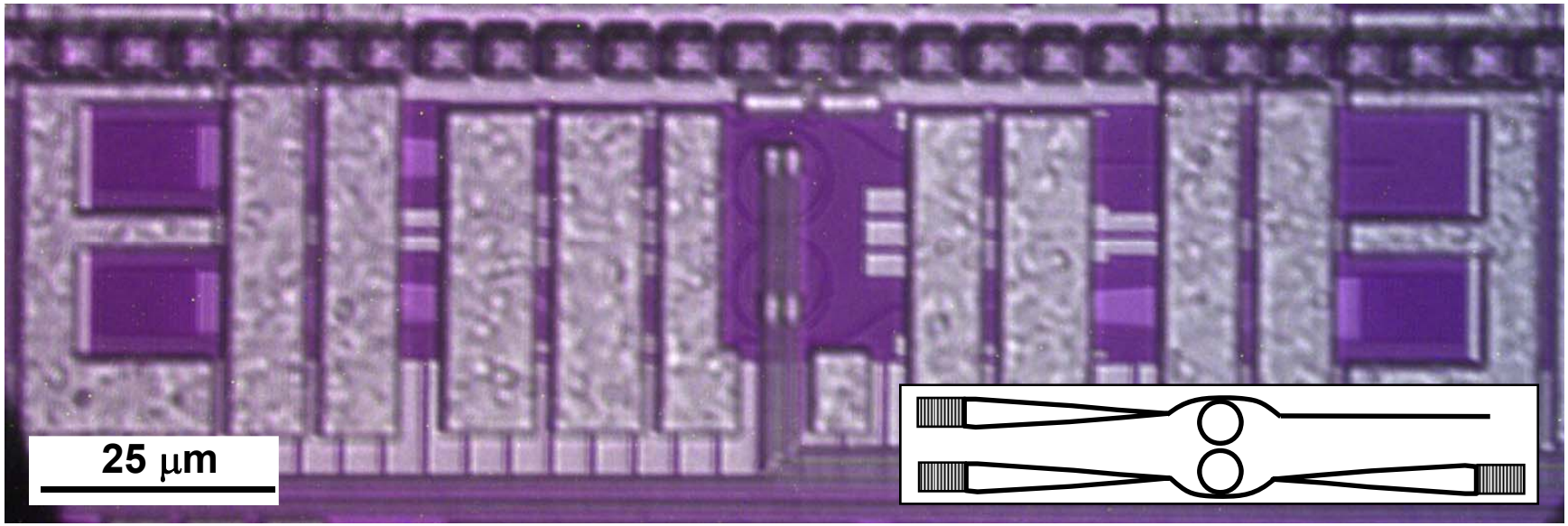
Propagation of Substrate Etch Front



Implications for High-Performance ICs

- SC Photonic devices in bulk-Si CMOS
- Optical intrachip communication
  - higher speeds
  - lower power

Second-Order Ring Resonator Built in 65 nm Bulk-Si CMOS



Conclusions

- Localized substrate removal enables bulk CMOS photonics
- XeF_2 for local substrate removal
- Propagation loss of ~10 dB/cm is achievable
- Process works on ICs

Acknowledgments

- We would like to thank Texas Instruments for supplying the polysilicon films and ICs for these experiments