A 4Gb/s/ch 356fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Transimpedance Receiver in 90nm CMOS Technology

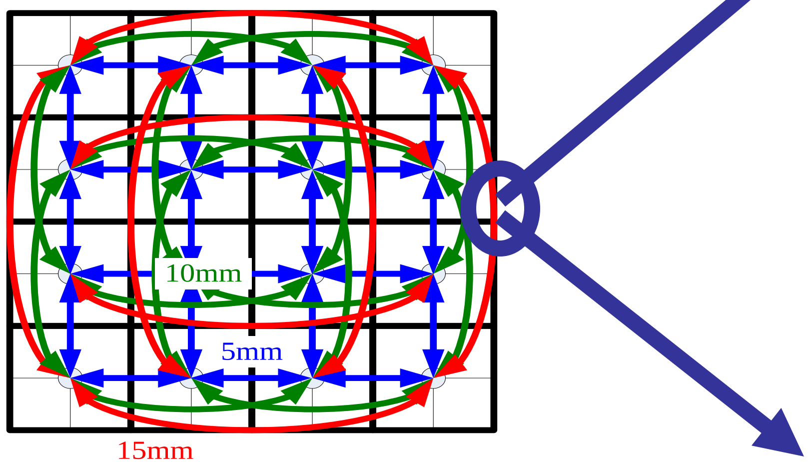
Byungsub Kim

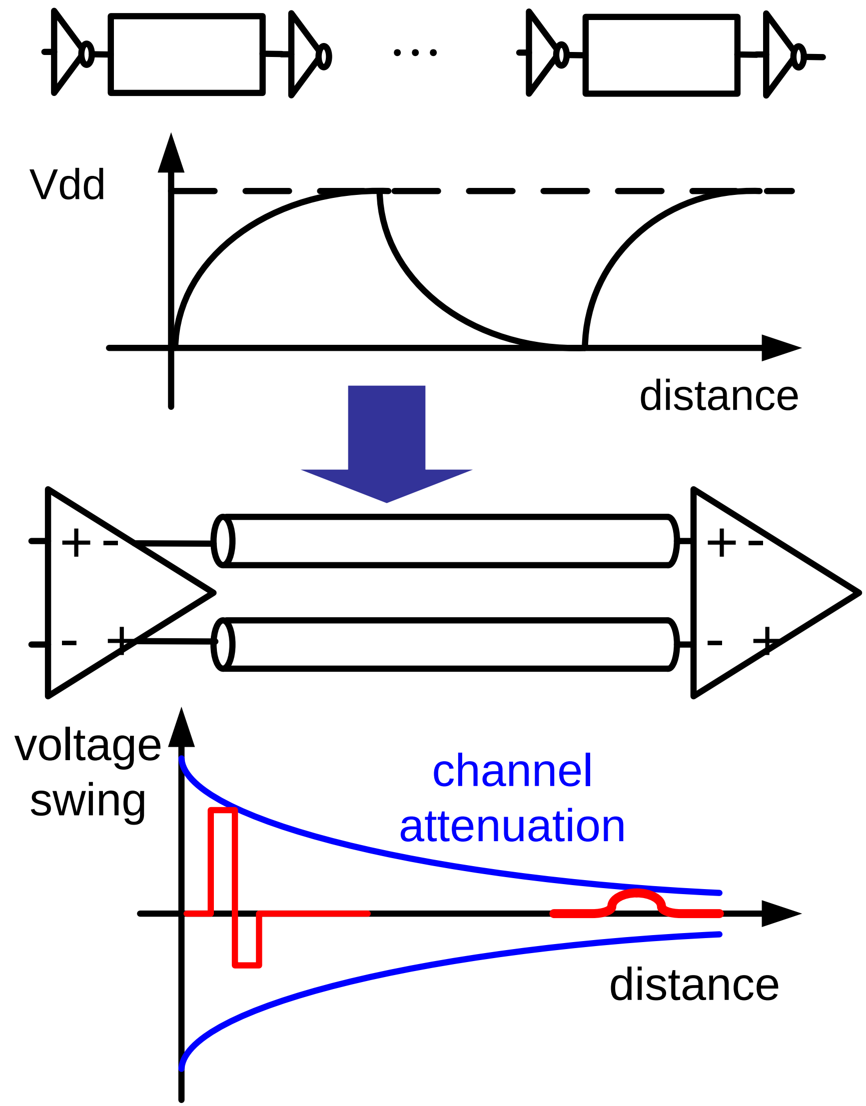
Vladimir Stojanović

Massachusetts Institute of Technology

Application

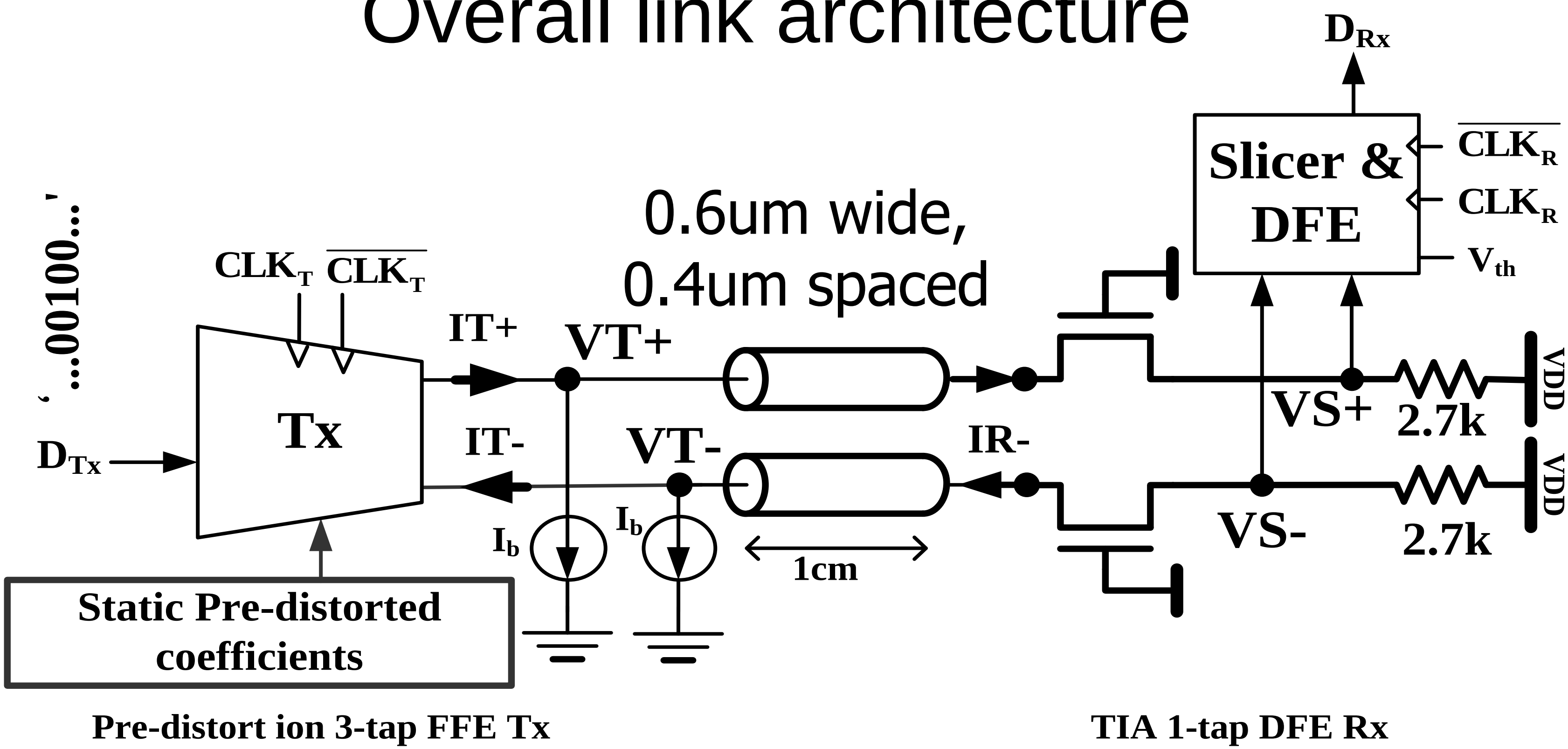
Flattened Butterfly NoC of 64 core processor





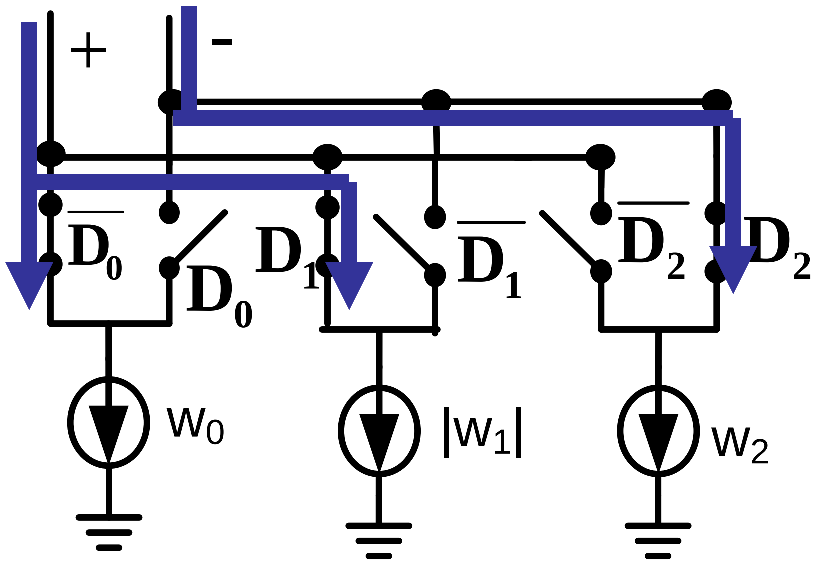
- Long distance interconnect for NoC of many-core processor
- Equalizer benefit
  - Better energy efficiency
  - Lower latency

Overall link architecture



- 3-tap Nonlinear Charge-Injecting Feed Forward Equalizer (FFE) improves driver power efficiency.
- Trans-impedance Amplifier (TIA) before 1-tap DFE improves the bandwidth-power-amplitude trade-off.

Power lost in linear analog subtraction

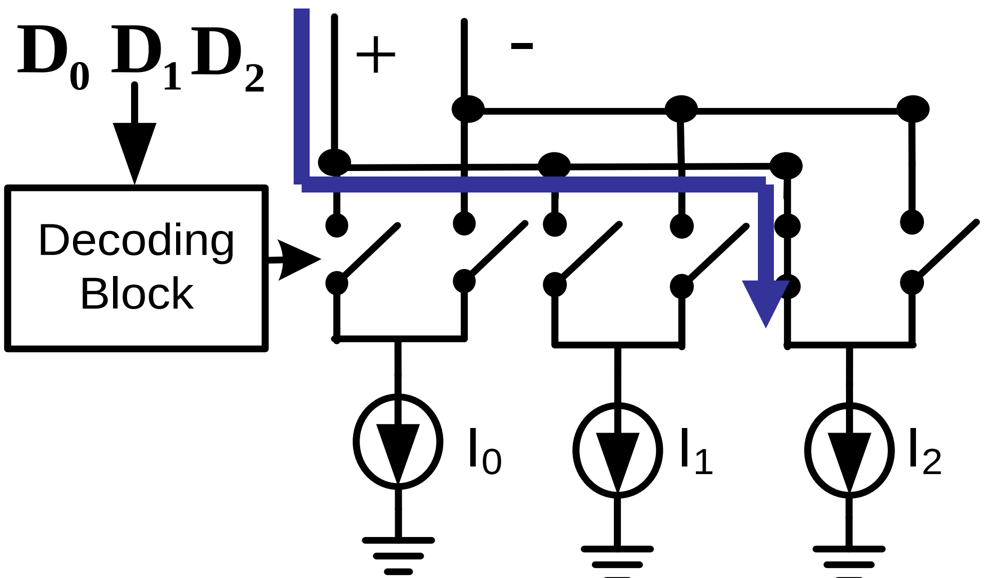


Analog FFE

$D_0D_1D_2$	FFE sum	IT+
1 1 1	$w_0+w_1+w_2$	I_0
1 1 0	$w_0+w_1-w_2$	$-I_1$
1 0 1	$w_0-w_1+w_2$	$I_0+I_1+I_2$
1 0 0	$w_0-w_1-w_2$	I_2
0 1 1	$-w_0+w_1+w_2$	$-I_2$
0 1 0	$-w_0+w_1-w_2$	$-(I_0+I_1+I_2)$
0 0 1	$-w_0-w_1+w_2$	I_1
0 0 0	$-w_0-w_1-w_2$	$-I_0$

- Linear analog subtraction wastes current
  - $Isup=|w_0|+|w_1|+|w_2|=I_0+I_1+I_2$, $w_1<0$
  - $Isig=-w_0+w_1+w_2=-I_2$, $w_1<0$

Charge Injecting FFE

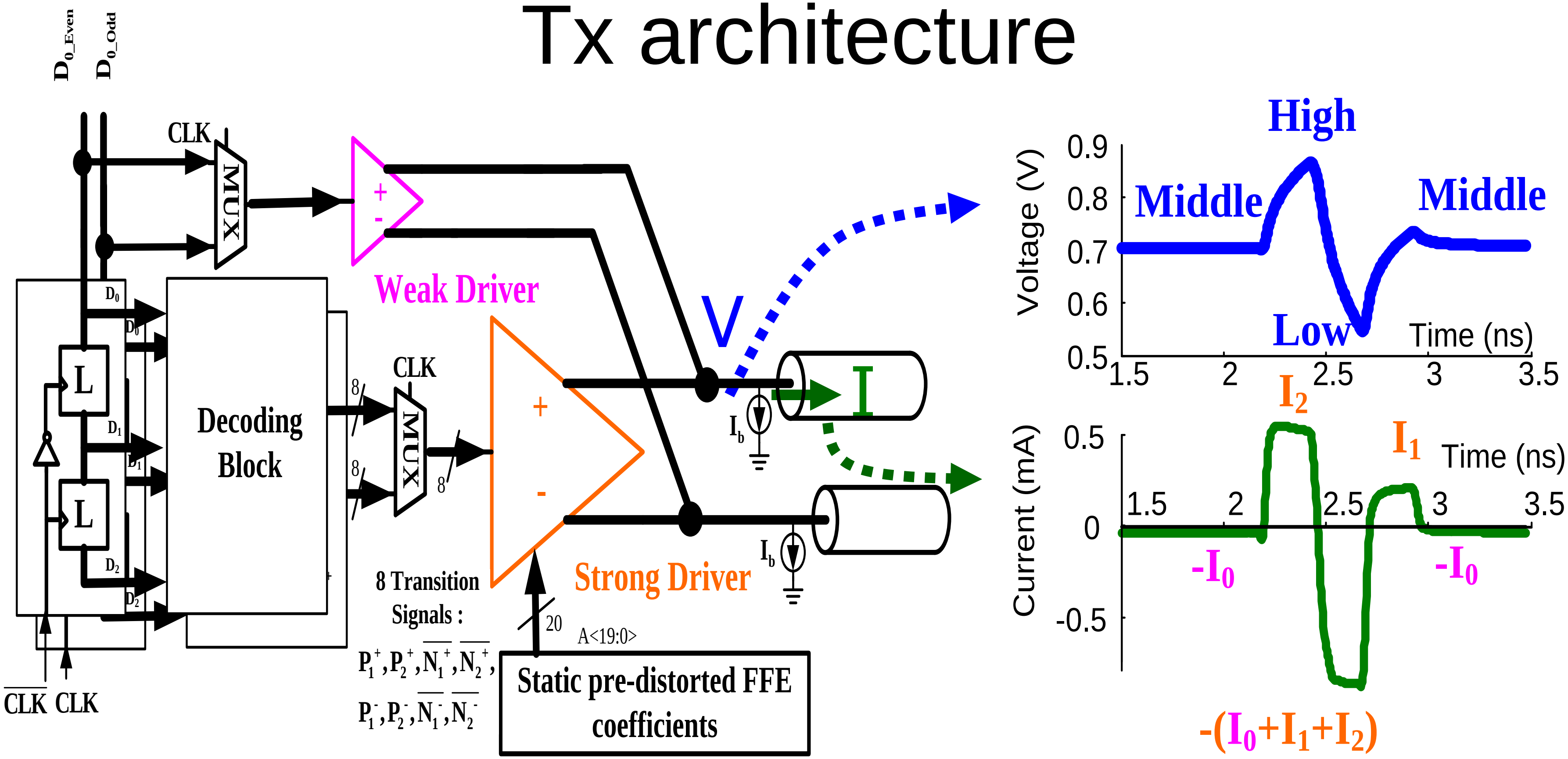


Charge injection FFE

$D_0D_1D_2$	FFE sum	IT+
1 1 1	$w_0+w_1+w_2$	I_0
1 1 0	$w_0+w_1-w_2$	$-I_1$
1 0 1	$w_0-w_1+w_2$	$I_0+I_1+I_2$
1 0 0	$w_0-w_1-w_2$	I_2
0 1 1	$-w_0+w_1+w_2$	$-I_2$
0 1 0	$-w_0+w_1-w_2$	$-(I_0+I_1+I_2)$
0 0 1	$-w_0-w_1+w_2$	I_1
0 0 0	$-w_0-w_1-w_2$	$-I_0$

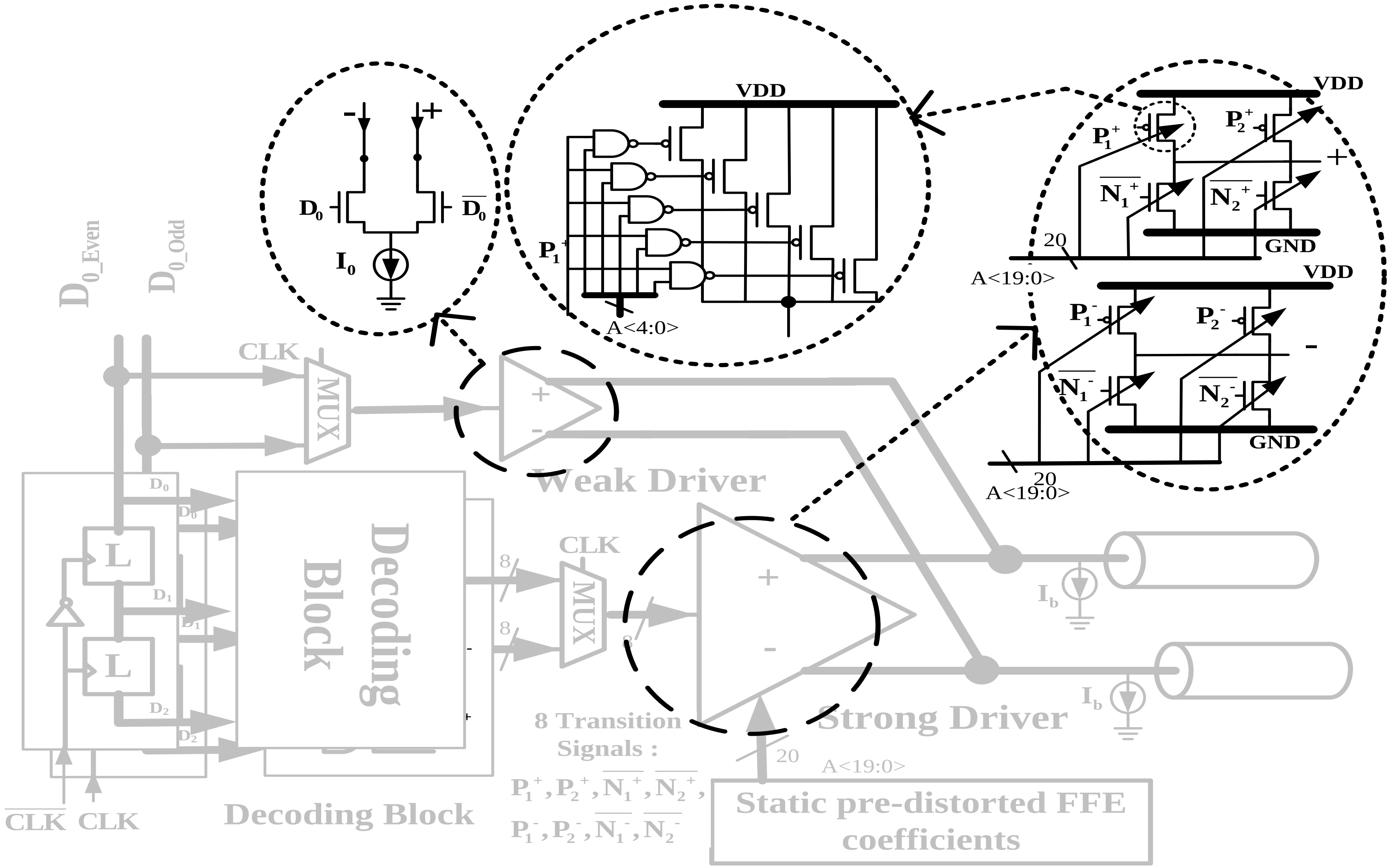
- Avoid linear analog subtraction ➔ linearity issue
  - $Isup=|-w_0+w_1+w_2|=I_2$, $w_1<0$
  - $Isig=-w_0+w_1+w_2=-I_2$, $w_1<0$

Tx architecture

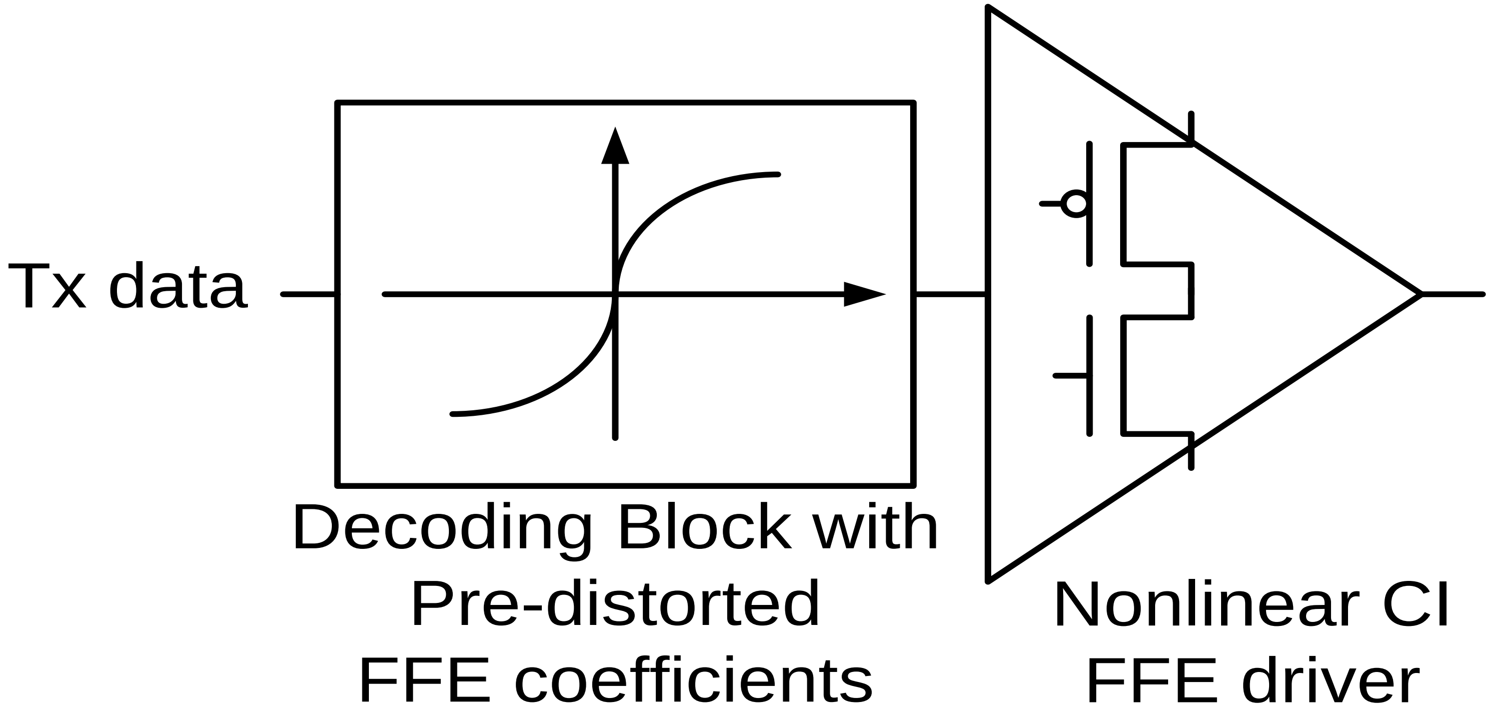


- Strong driver: Large current (I_1, I_2, I_1+I_2) at data transition (AC) ➔ channel attenuation relieves current resolution requirement (3-5bit)
- Weak driver: Small current (I_0) at static level (DC). ➔ accurate control of current resolution required (3-5bit)

Tx architecture detail



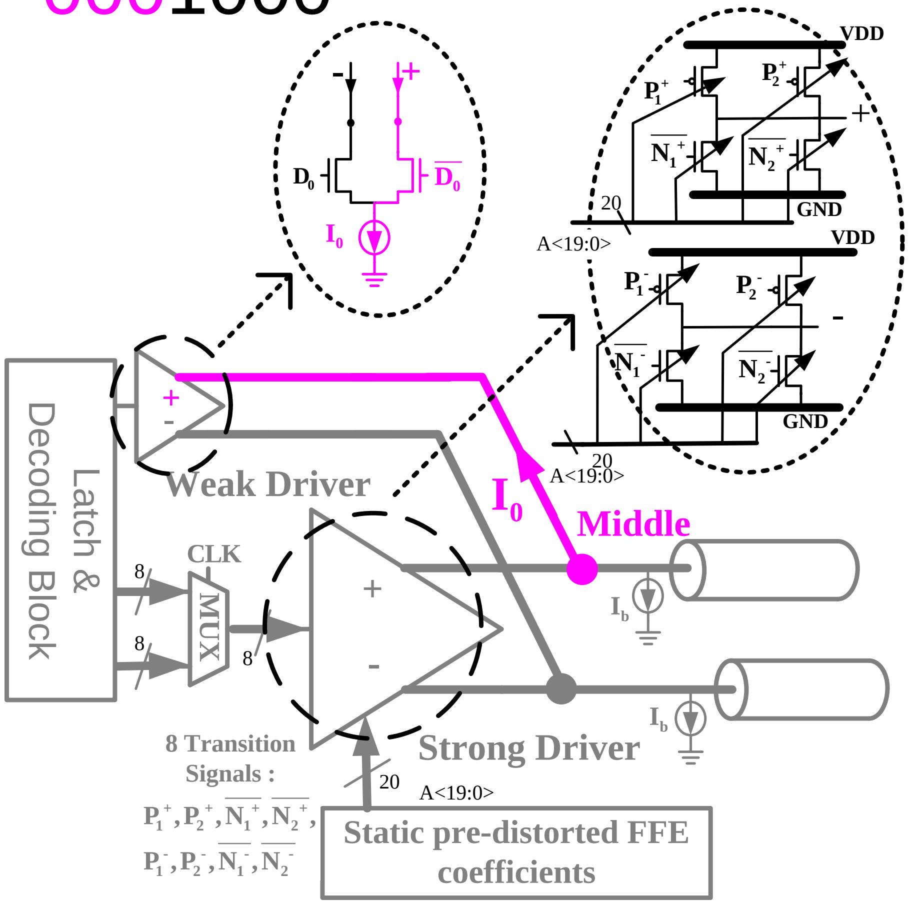
Nonlinearity compensation concept

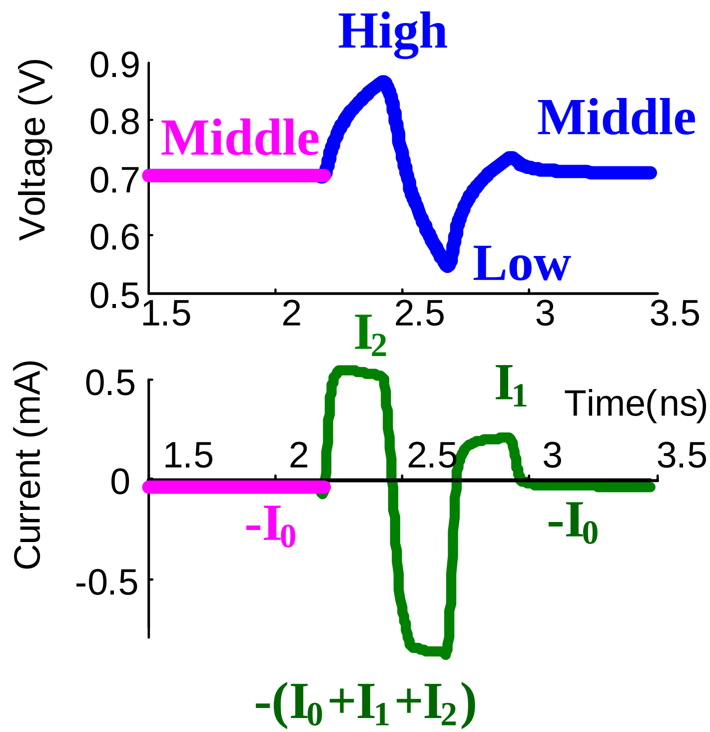


- Non-linear CI FFE driver
- Pre-distorted FFE coefficients in decoding block

Tx control and nonlinearity compensation

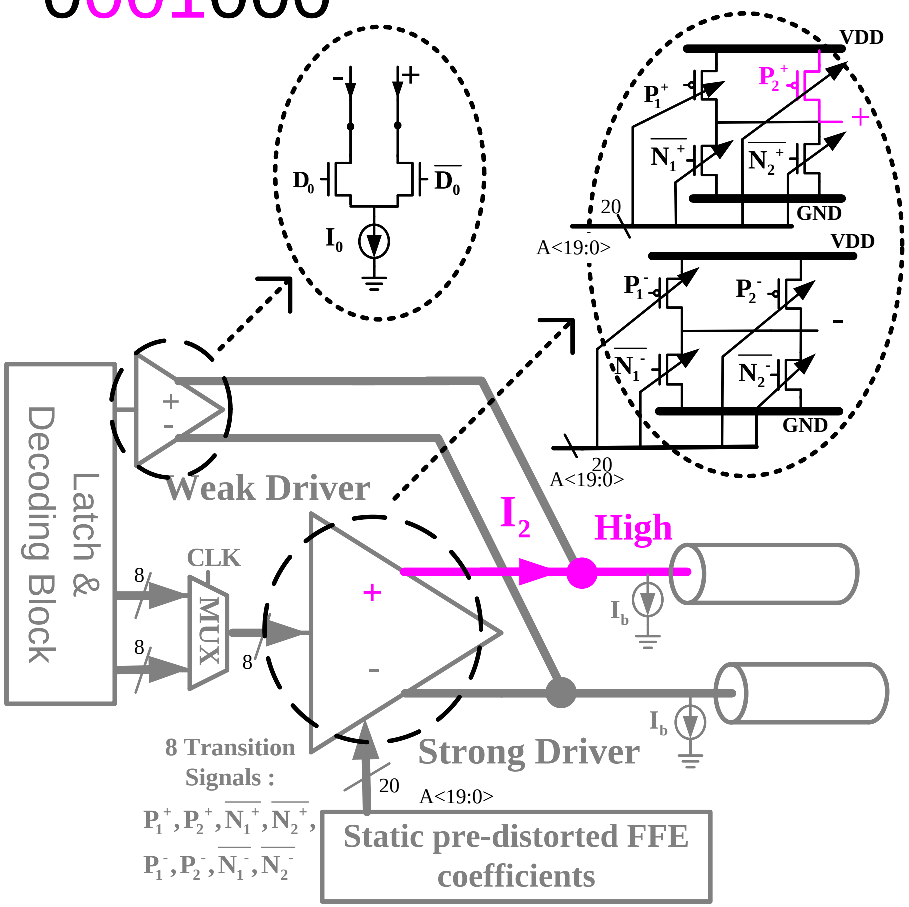
- 0001000

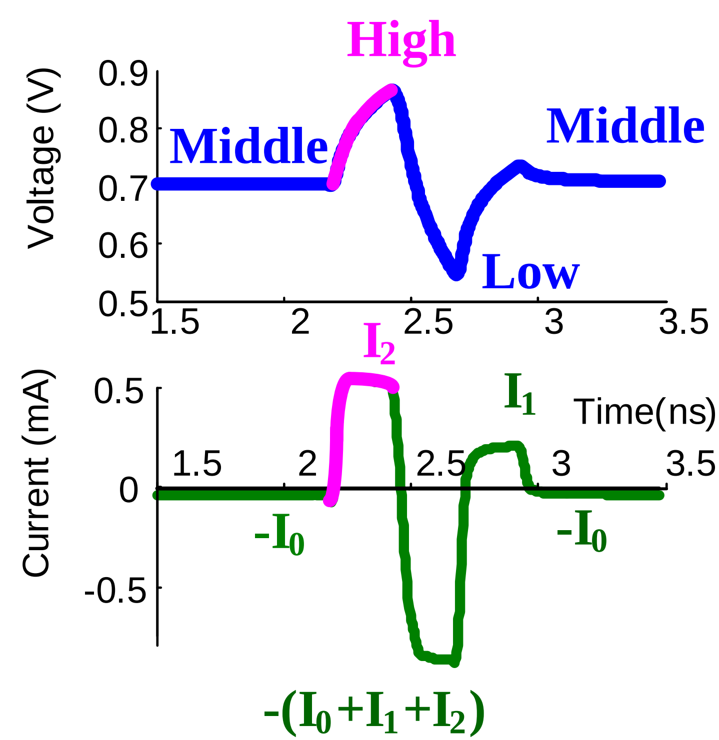




Tx control and nonlinearity compensation

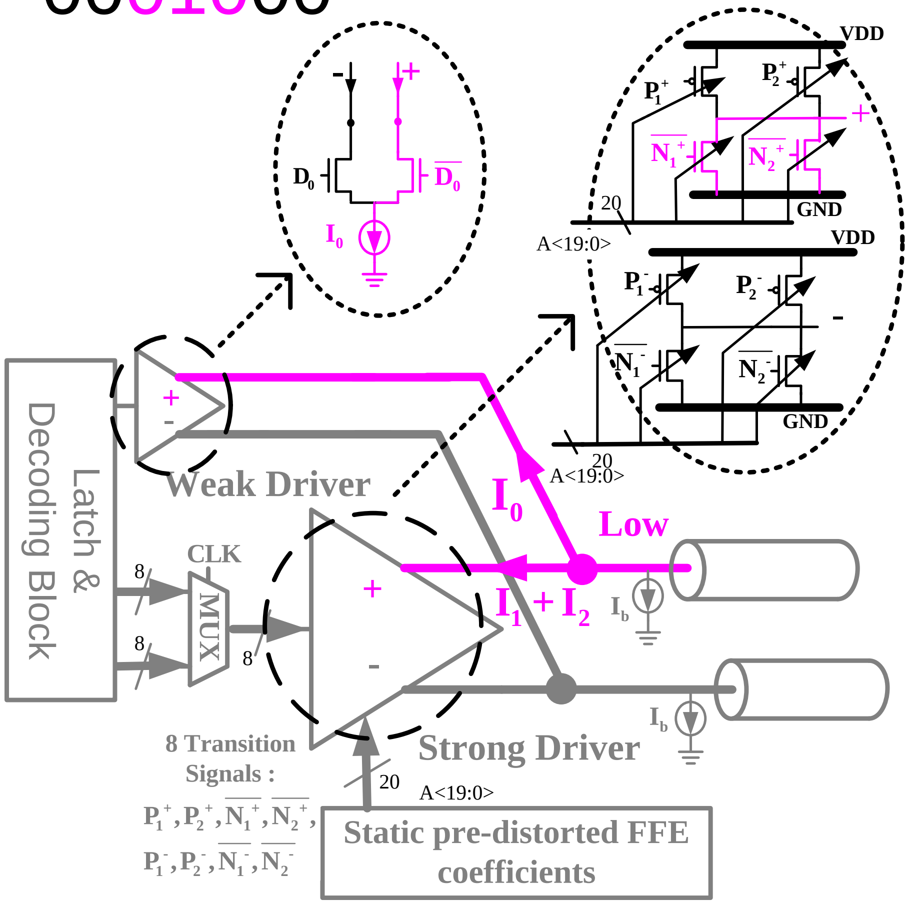
- 0001000

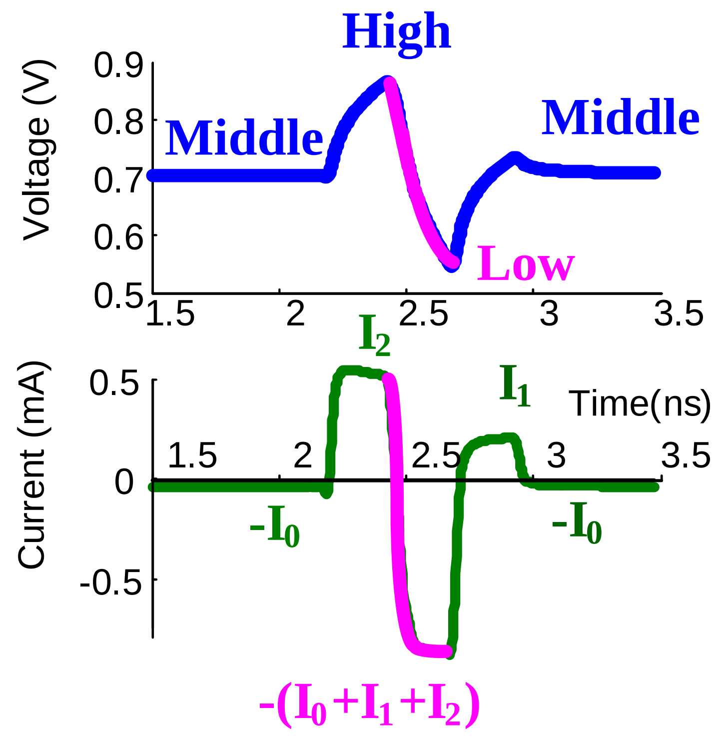




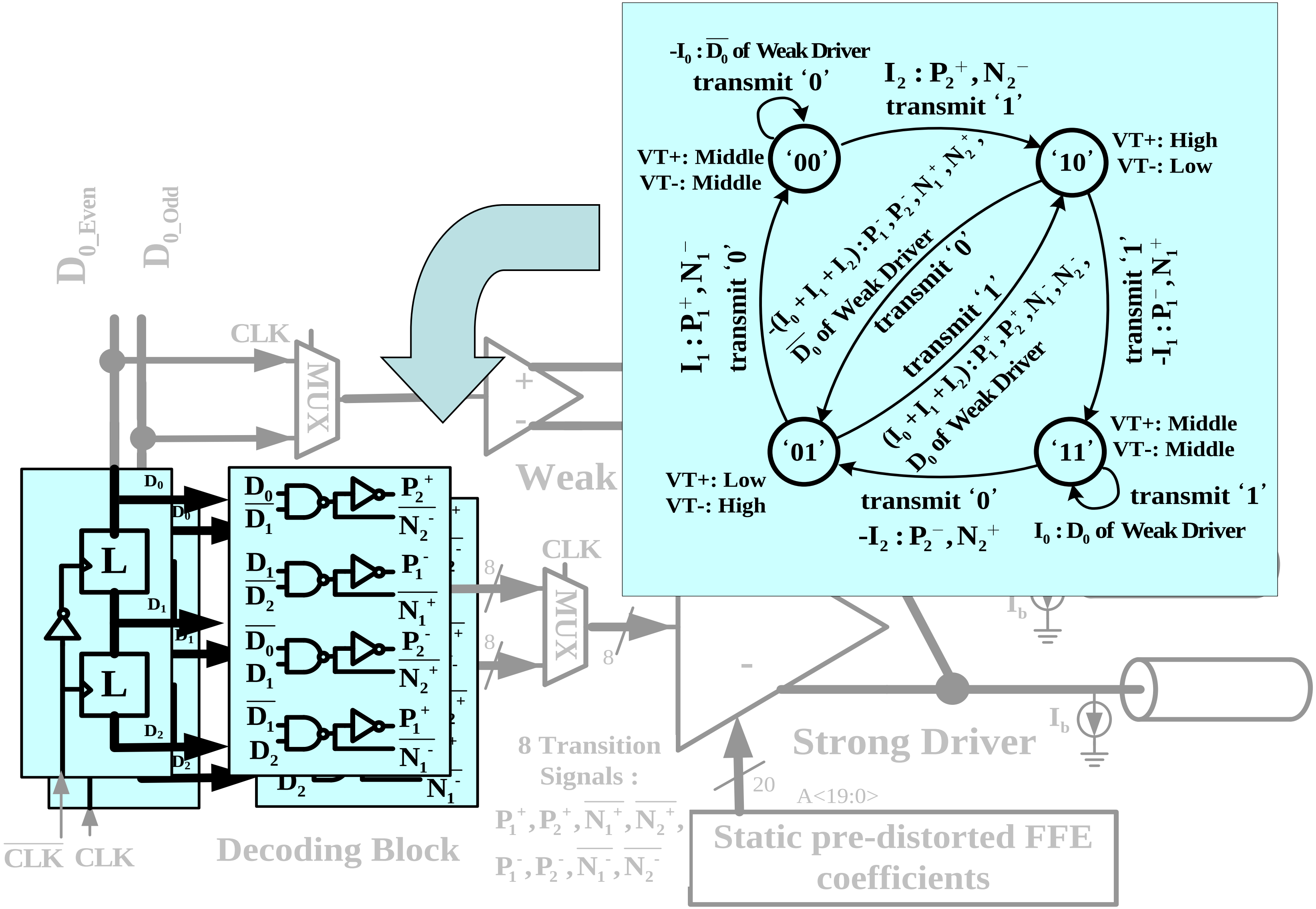
Tx control and nonlinearity compensation

- 0001000

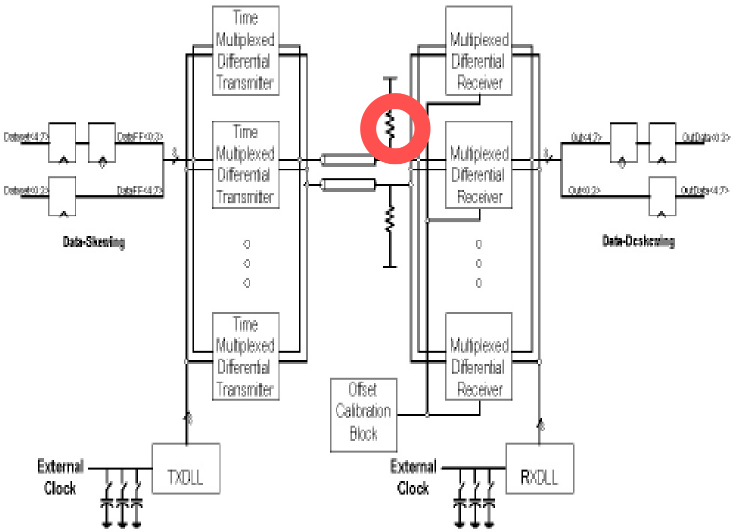


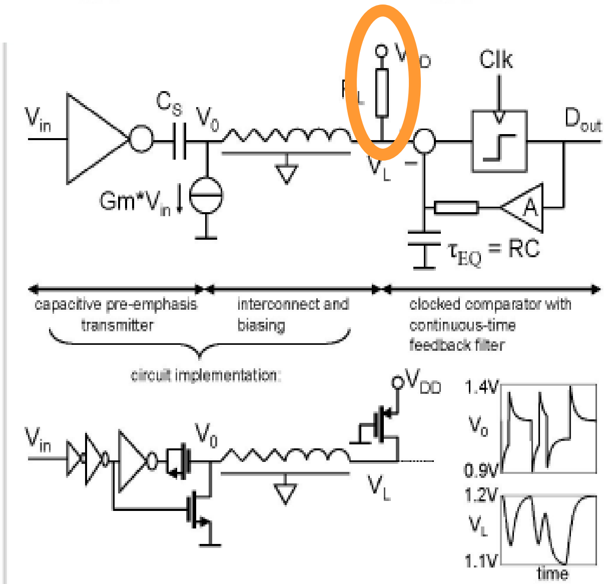


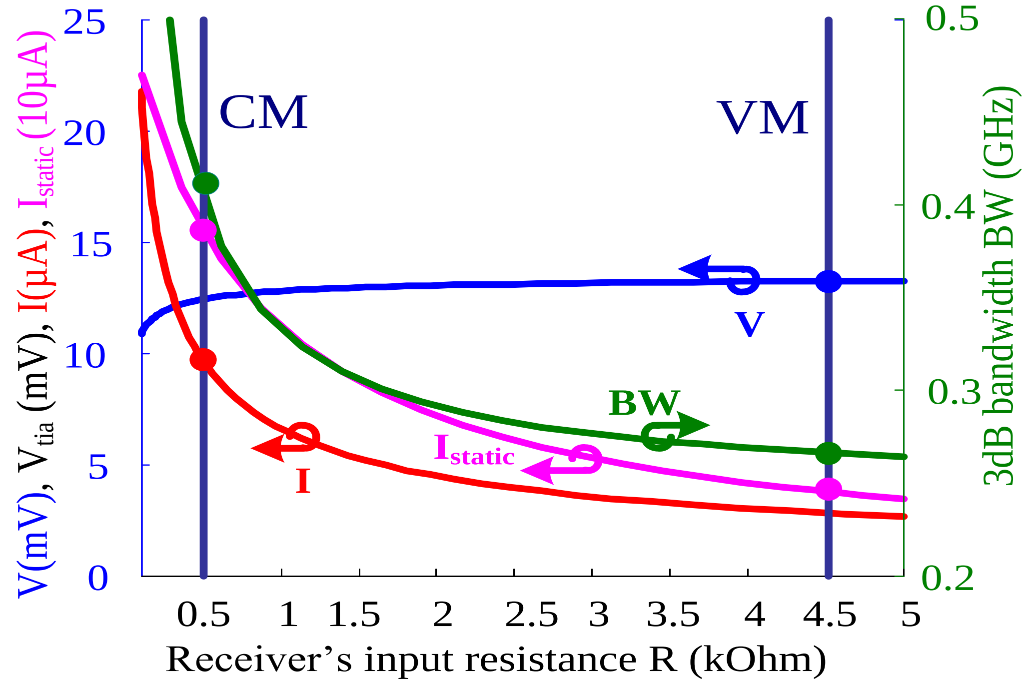
State diagram and decoding block



Receiver's termination trade off

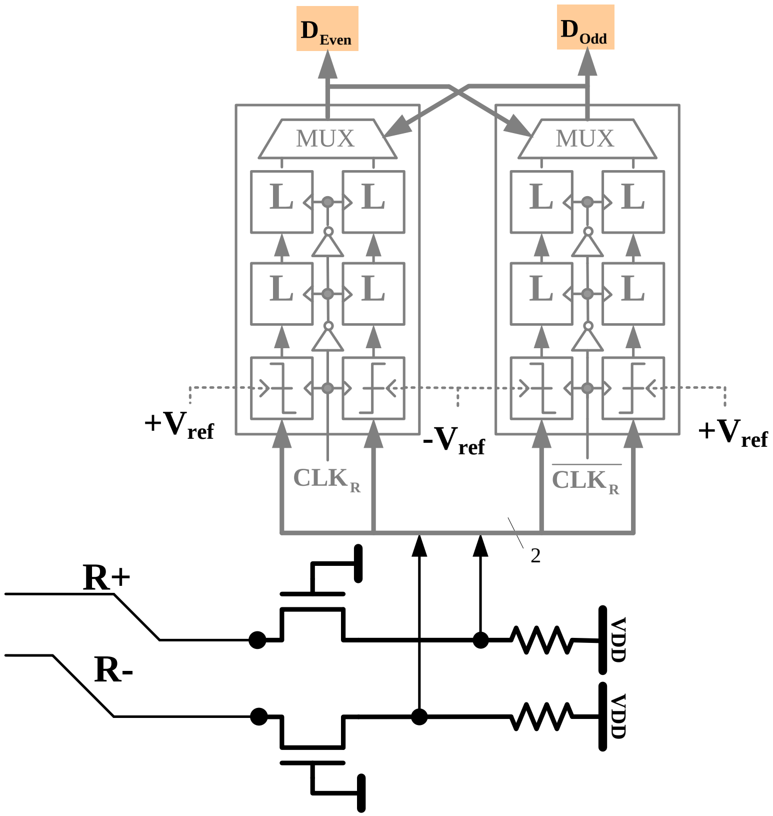




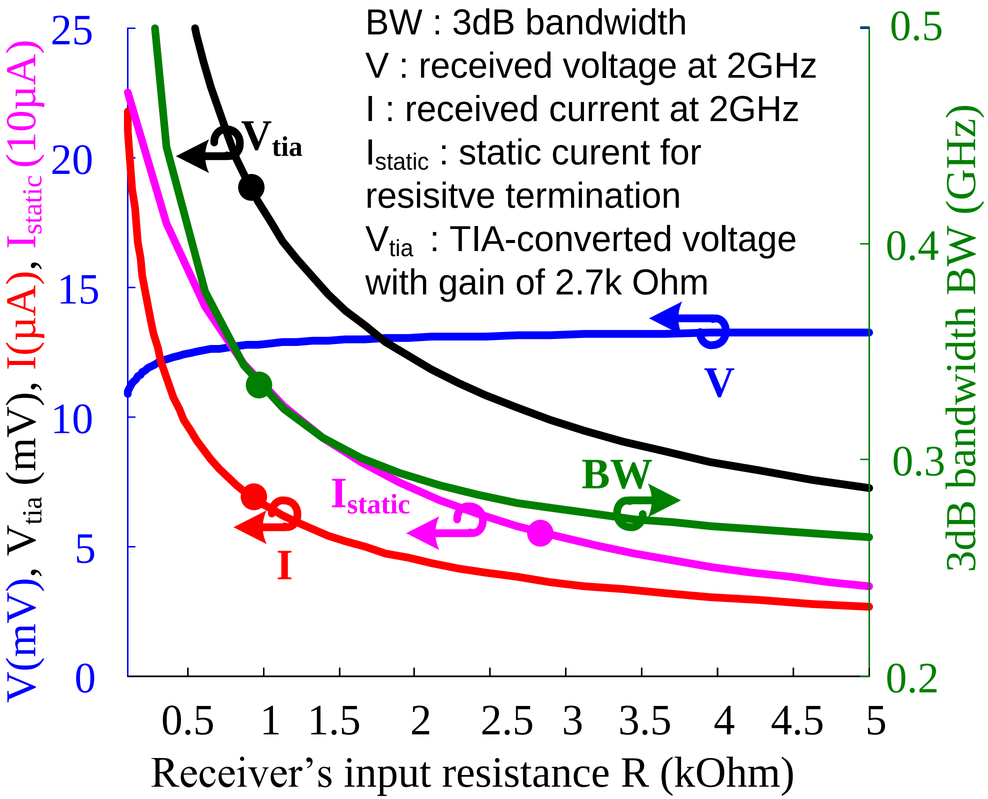


- Current mode (CM) : small R : A.P. Jose, VLSI'05
- Voltage mode (VM) : large R : E. Mensink ISSCC'07

Trade-off of trans-impedance amplifier (TIA)

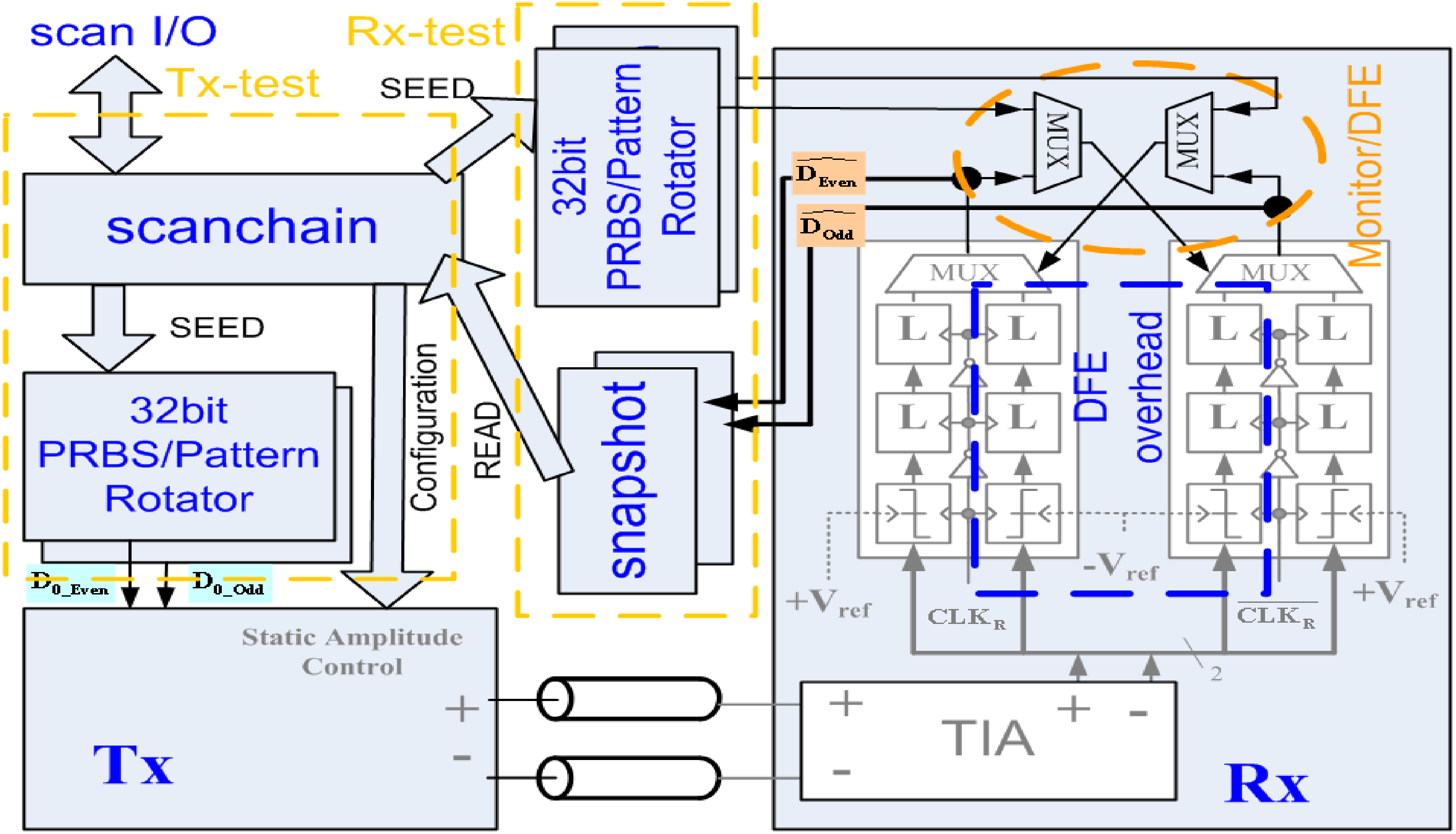


Transimpedance Receiver

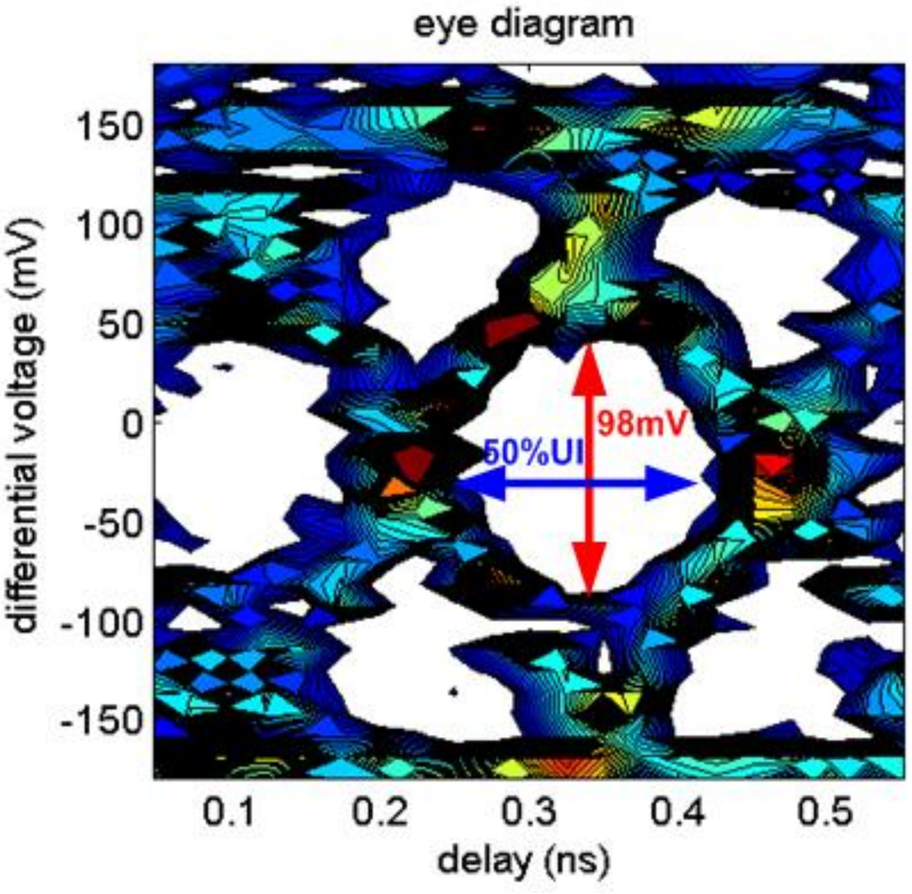


- TIA achieves high bandwidth, small static power, large amplitude simultaneously.
  - 50% static current, 150% voltage amplitude for the same bandwidth

Chip Infrastructure for *in-situ* characterization

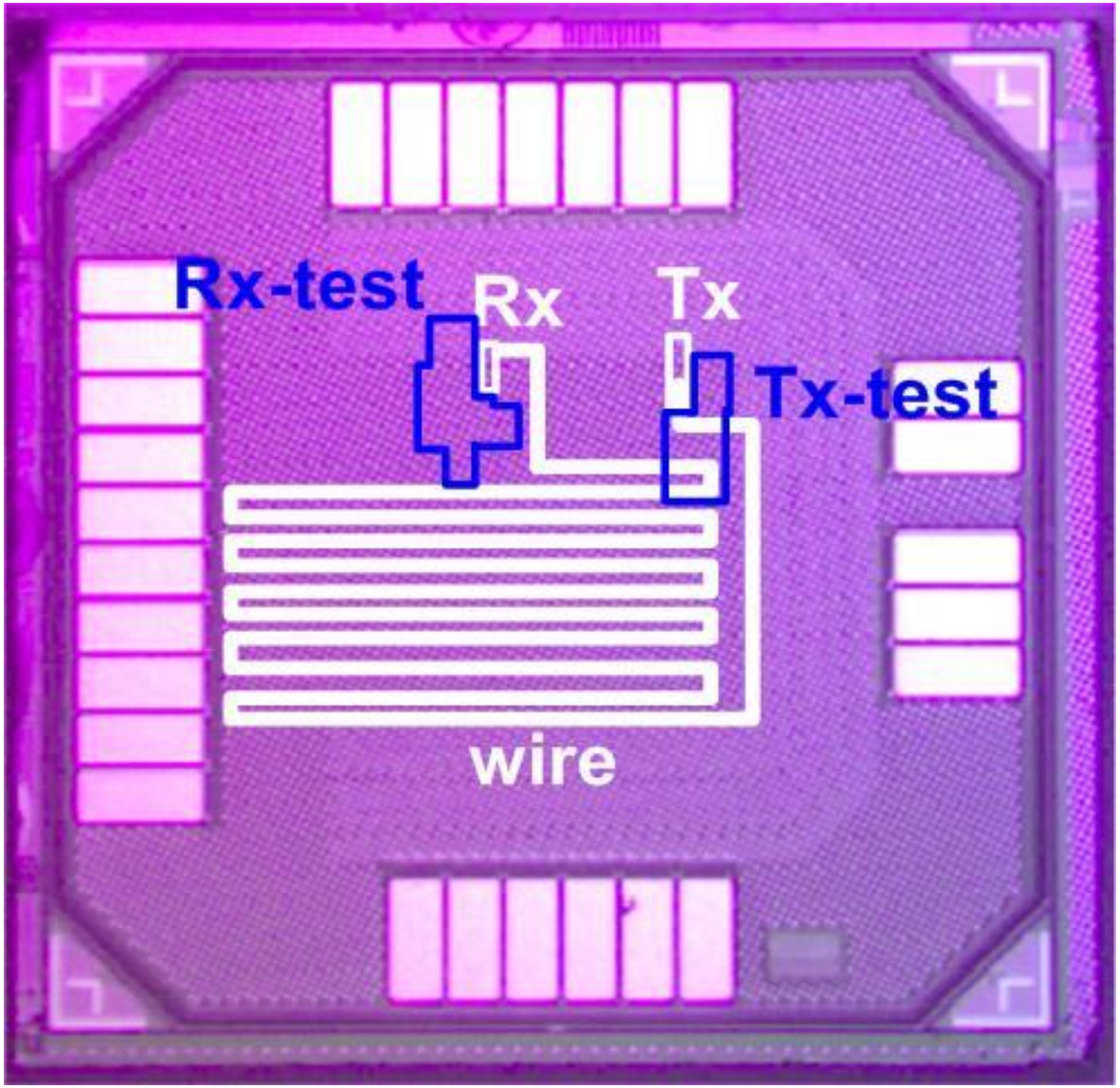


Eye diagram (4Gb/s/ch, 2Gb/s/um)



- 98mVdpp vertical
- 50%UI horizontal
- First measured *in-situ*
  - Sweep threshold
  - Sweep receiver delay
- FFE: only
- DFE: not necessary

Chip die photo



- 1mm x 1mm
- 90nm CMOS
- Tx core : 70um x 16um
- Rx core : 40um x 16um

Comparison to relevant work

<table>
<tr><th></th><th colspan="3">This work</th><th>Mensink
ISSCC07</th><th>Repeater
Kim ICCAD07</th></tr>
<tr><td>Data rate</td><td colspan="3">4Gb/s/ch</td><td>2Gb/s/ch</td><td>4Gb/s/ch</td></tr>
<tr><td>Data rate density</td><td colspan="3">2Gb/s/µm</td><td>1.1628Gb/s/µm</td><td>2Gb/s/µm</td></tr>
<tr><td>Channel length</td><td colspan="3">1cm</td><td>1cm</td><td>1cm</td></tr>
<tr><td>Vertical Eye</td><td colspan="3">98mV</td><td>N/A</td><td>rail-to-rail</td></tr>
<tr><td>Horizontal Eye</td><td colspan="3">50%UI@(4Gb/s)
measured on-chip</td><td>44%UI @
(1.75Gb/s) after
50Ohm buffer</td><td>N/A</td></tr>
<tr><td rowspan="10">Measured Energy Cost (fJ/b) at room temperature</td><td>total</td><td colspan="2">356</td><td rowspan="10">280</td><td rowspan="10">1500</td></tr>
<tr><td rowspan="6">Tx</td><td>total</td><td>277</td></tr>
<tr><td>Strong driver</td><td>51</td></tr>
<tr><td>Weak driver
+ TIA bias</td><td>48</td></tr>
<tr><td>Decoder</td><td>24</td></tr>
<tr><td>Clock</td><td>67</td></tr>
<tr><td>Pre-driver</td><td>87</td></tr>
<tr><td rowspan="3">Rx</td><td>total</td><td>79</td></tr>
<tr><td>Slicer/Latch</td><td>30</td></tr>
<tr><td>Clock</td><td>49</td></tr>
<tr><td>Technology</td><td colspan="3">90nm</td><td>90nm</td><td>90nm</td></tr>
</table>

- 30% more energy, x2 more speed

Summary

- Charge-injection + non-linear compensation reduces driver’s power (< 50%).
  - Avoid analog subtraction
  - Utilize efficient nonlinear driver
- Trans-impedance amplifier (TIA) achieves high bandwidth, small power, and large amplitude simultaneously.
  - 50% static power
  - 150% amplitude

Acknowledgement

- Trusted Foundry for chip fabrication
- Interconnect Focus Center (IFC)
- Semiconductor Research Corporation Program
- Intel Corporation
- Center for Integrated Circuits and Systems (CICS) at MIT

- Fred Chen, Sanquan Song