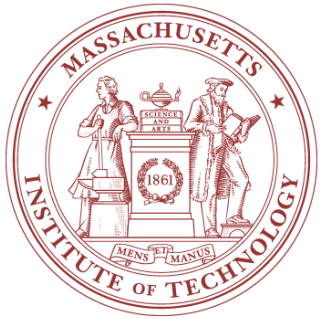
SRC/ATIC/NSF MEES 2020 Forum

Building Energy-Efficient Circuits with NEMS Devices

Vladimir Stojanović (MIT)

in collaboration with

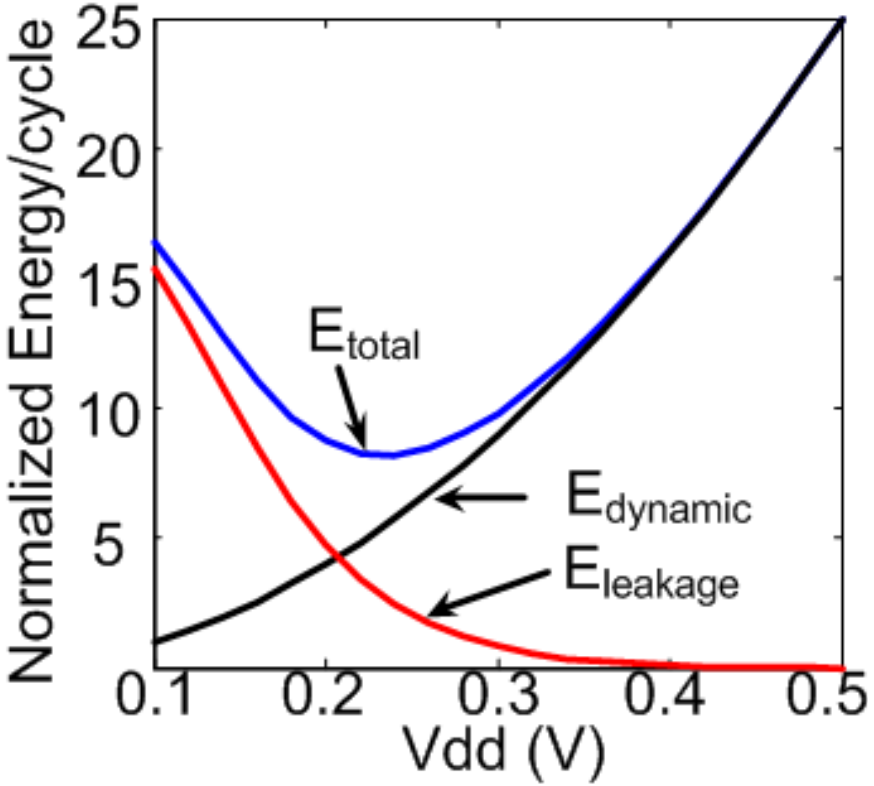
Tsu-Jae King Liu, Elad Alon (UC Berkeley)
Dejan Marković (UCLA)

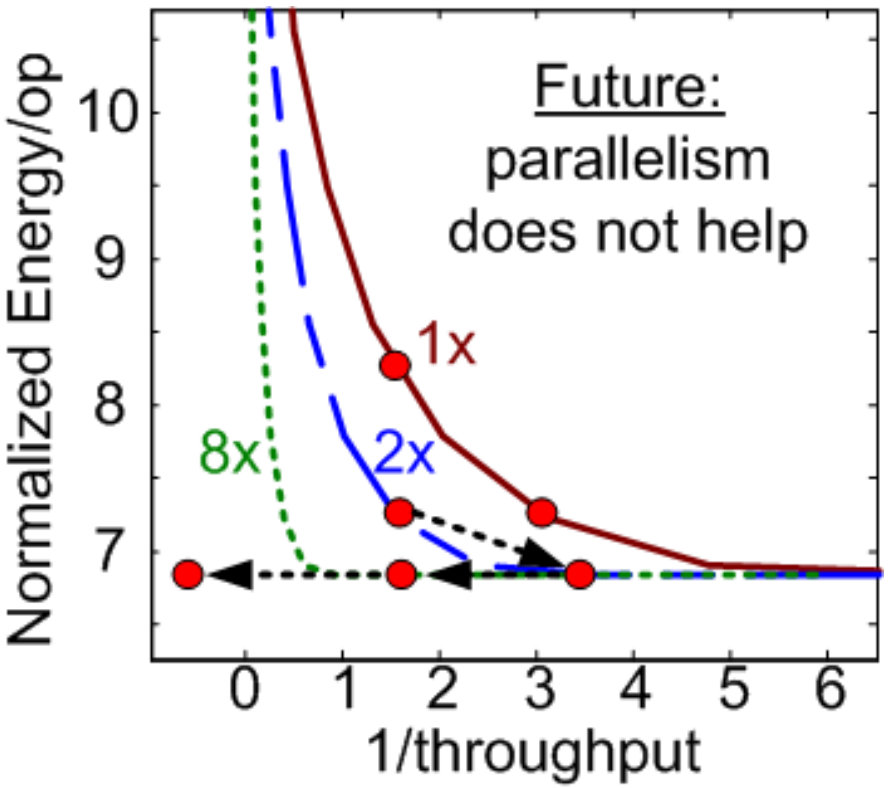


UCLA

May 23-24, 2010

Subthreshold Leakage: Game Over for CMOS

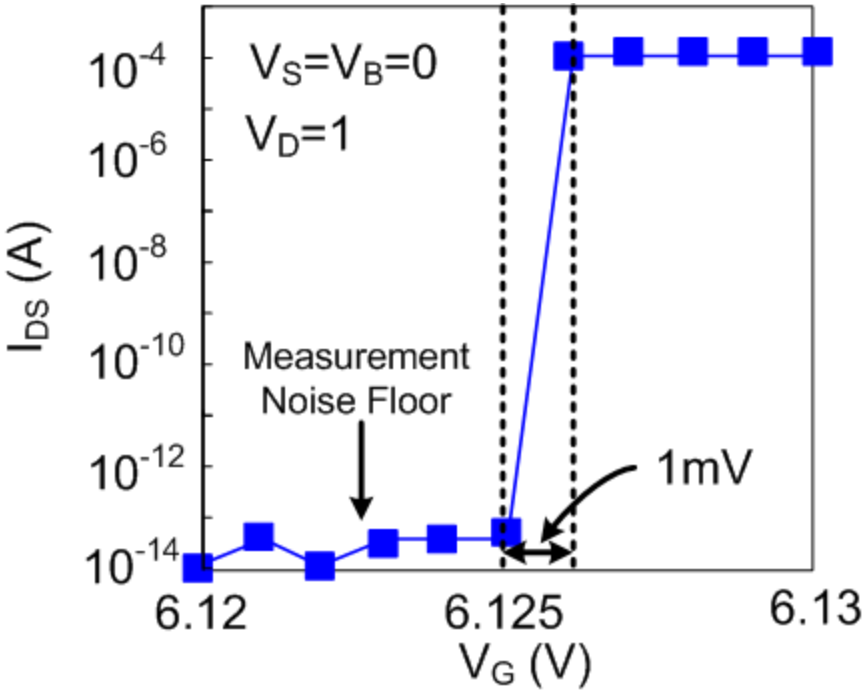




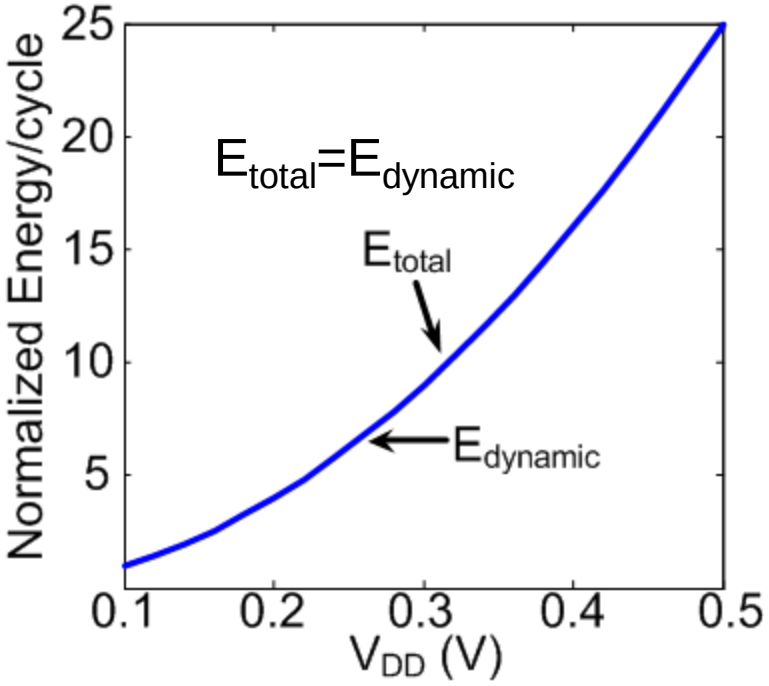
- Leakage and sub-threshold slope define minimum energy/op for CMOS
- Parallelism cannot reduce power/throughput if already operating at minimum energy

NEM Relays to the Rescue

Measured MEM Switch I-V Curve



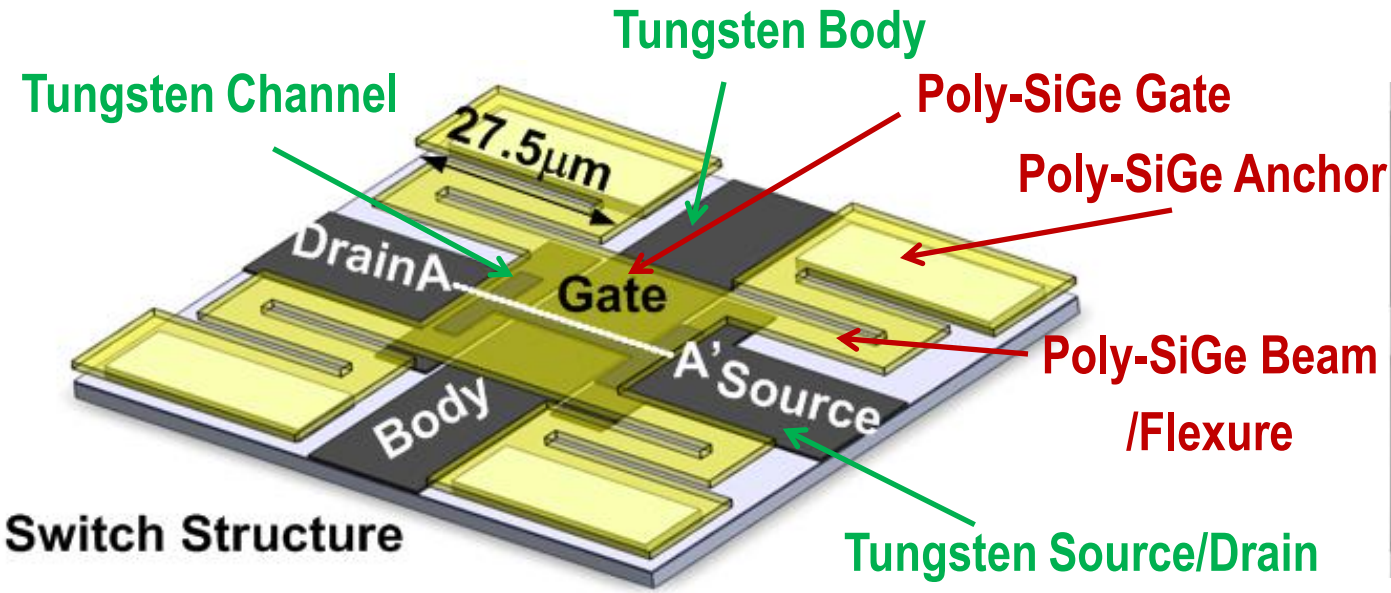
MEM Switch Energy vs. V_{DD}

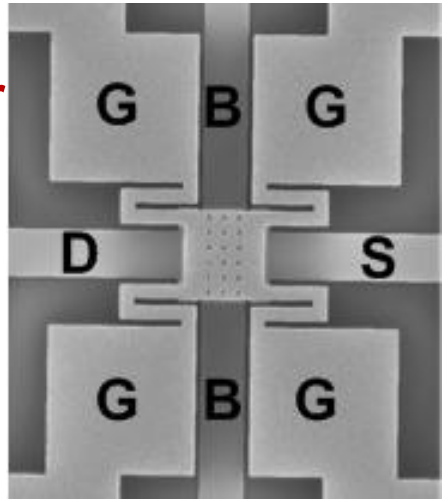


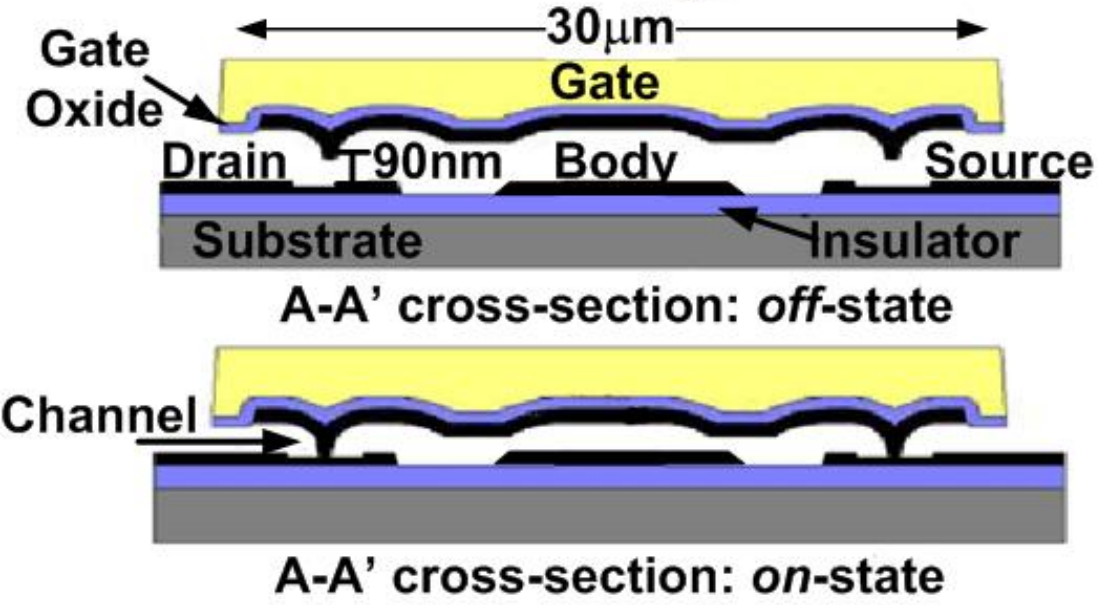
- NEM relays show zero leakage & sharp sub-threshold slope
- Could potentially enable reduced E/op with scaling
- E_{min} set by contact bond energy
  - ~4aJ/switch (10x better than 65nm CMOS)

R. Nathanael *et al*., "4-Terminal Relay Technology for Complementary Logic," *IEDM 2009*

NEM Relay Structure and Operation







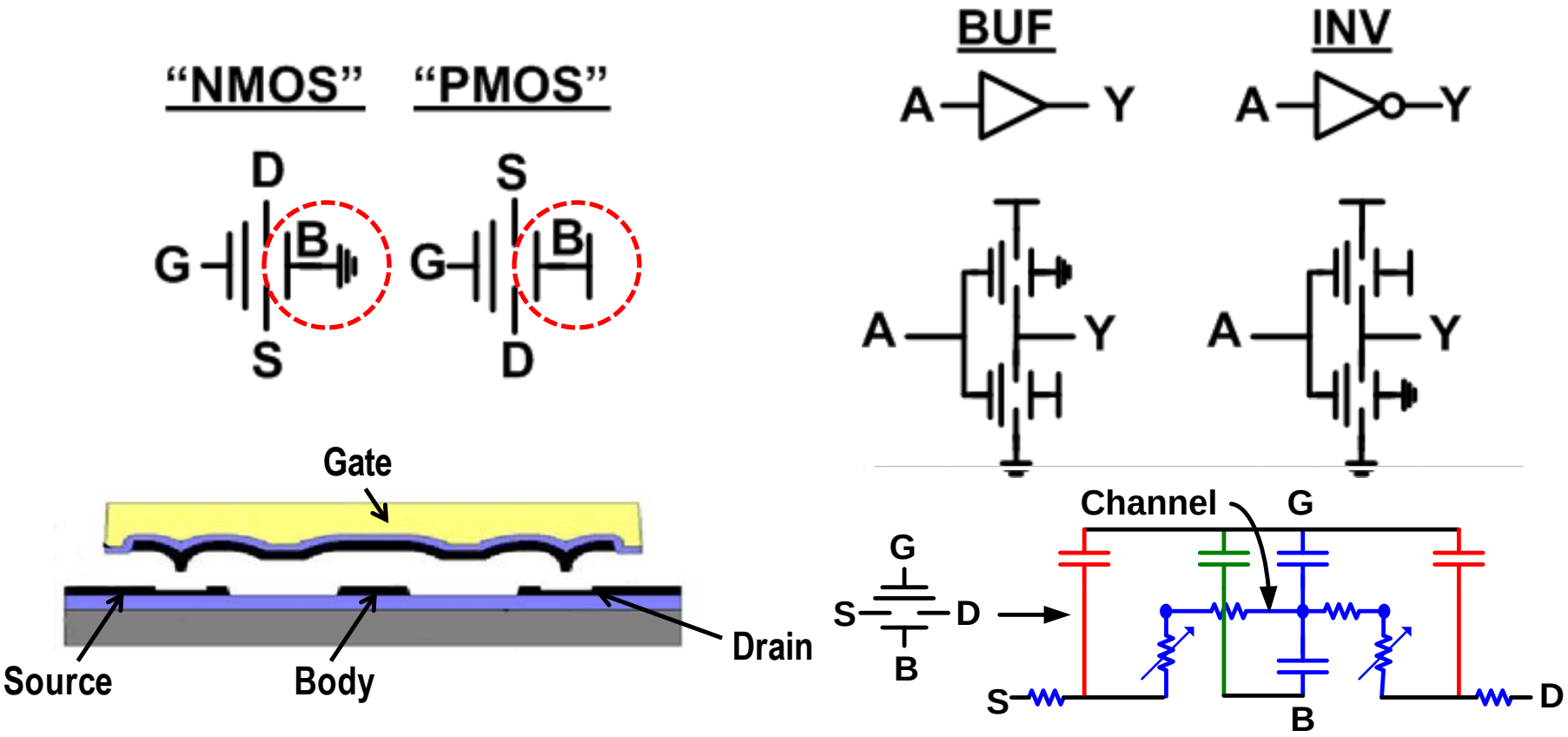
OFF Relay:

$|V_{gb}| < V_{po}$ (pull-out voltage)

ON Relay:

$|V_{gb}| > V_{pi}$ (pull-in voltage)

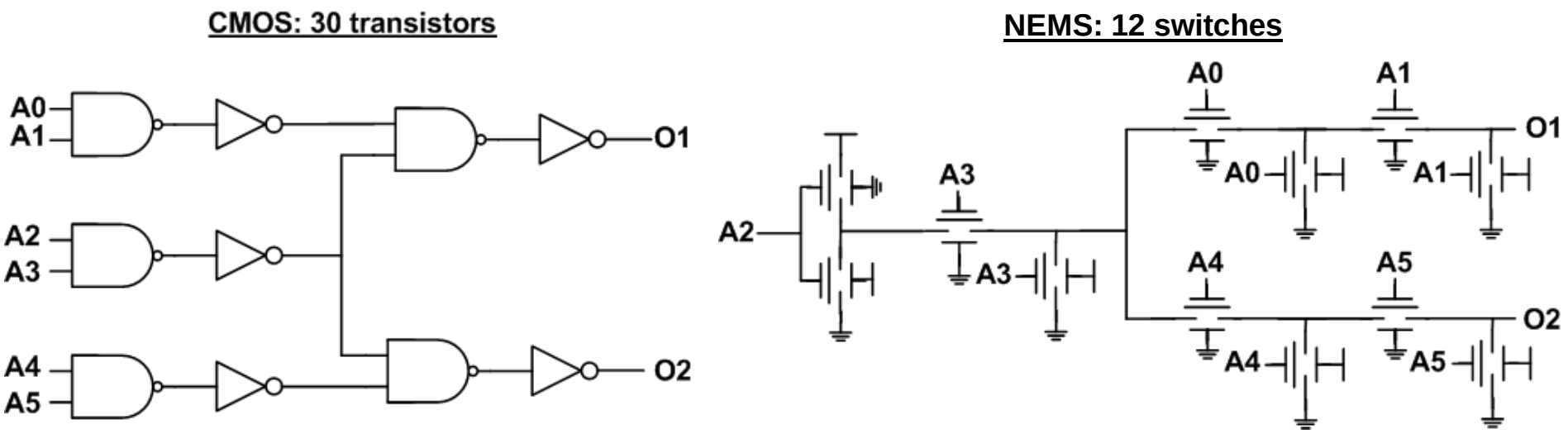
NEM Relay as a Logic Element



- 4-terminal design mimics MOSFET operation
  - Electrostatic actuation is ambipolar
- Non-inverting logic is possible
  - Actuation independent of source/drain voltages

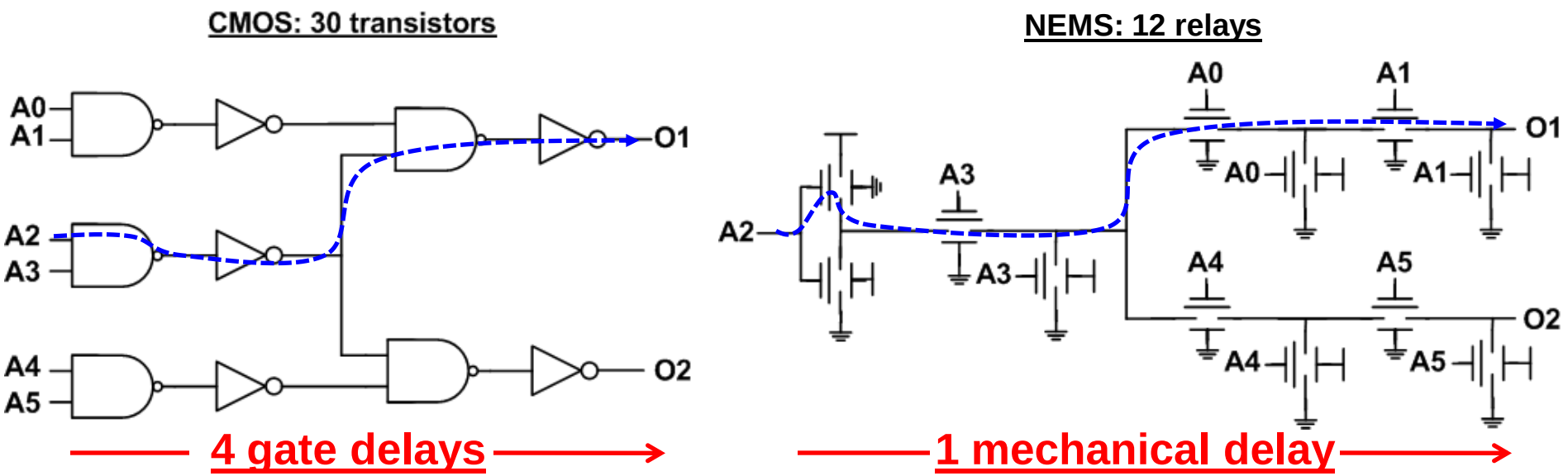
5

Digital Circuit Design with NEMS



- CMOS: delay set by electrical time constant
  - Quadratic delay penalty for stacking devices
  - Buffer & distribute logical/electrical effort over many stages
- NEMS: delay dominated by mechanical movement
  - Can stack ~100-200 devices before $t_{d,elec} \approx t_{d,mech}$
  - So, want all to switch <u>simultaneously</u>
  - → Implement logic as a single complex gate

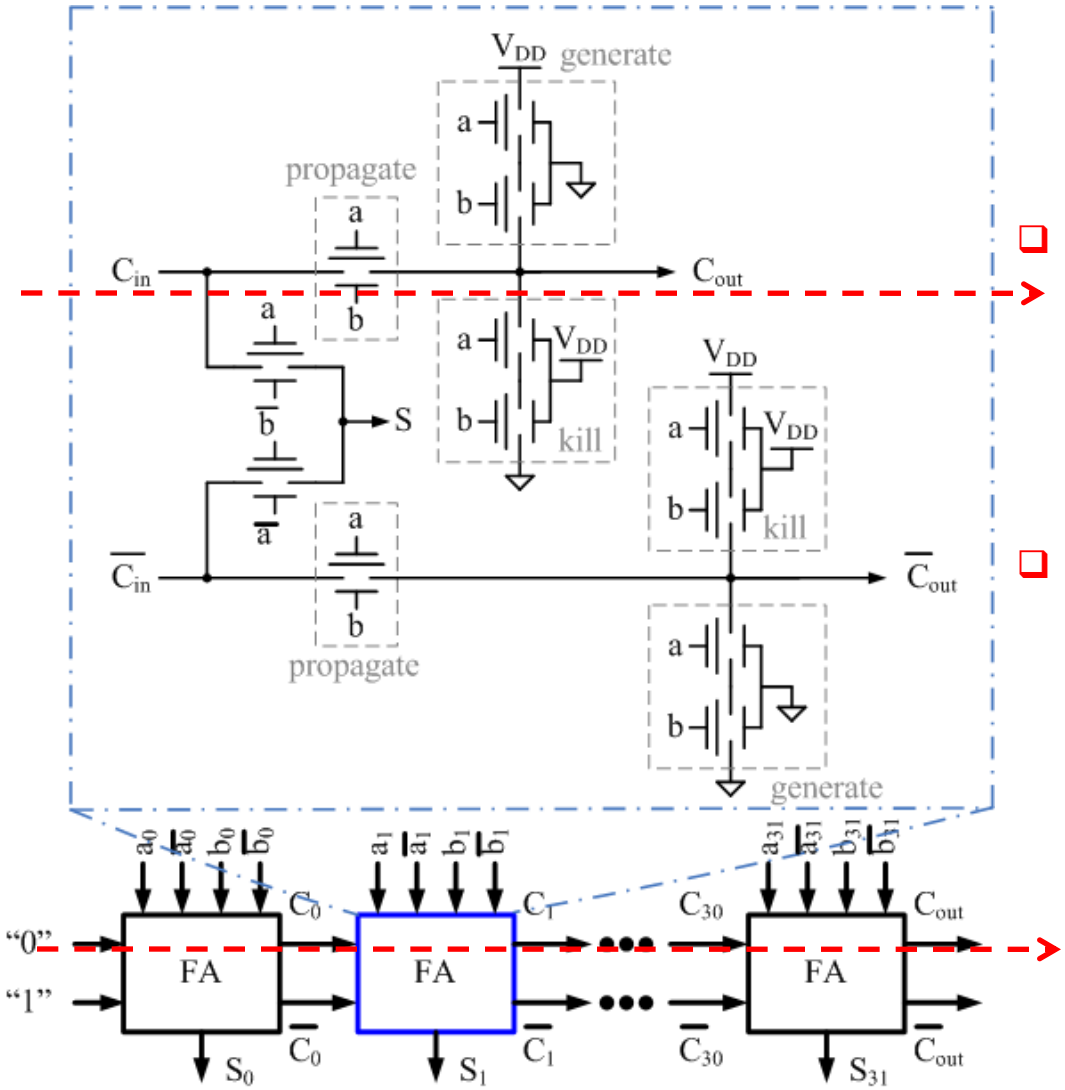
Need to Compare at Block Level



- Delay Comparison vs. CMOS
  - Single mechanical delay vs. several electrical gate delays
  - For reasonable load, NEMS delay unaffected by fan-out/fan-in
- Area Comparison vs. CMOS
  - Larger individual devices
  - But often need fewer devices to implement same function

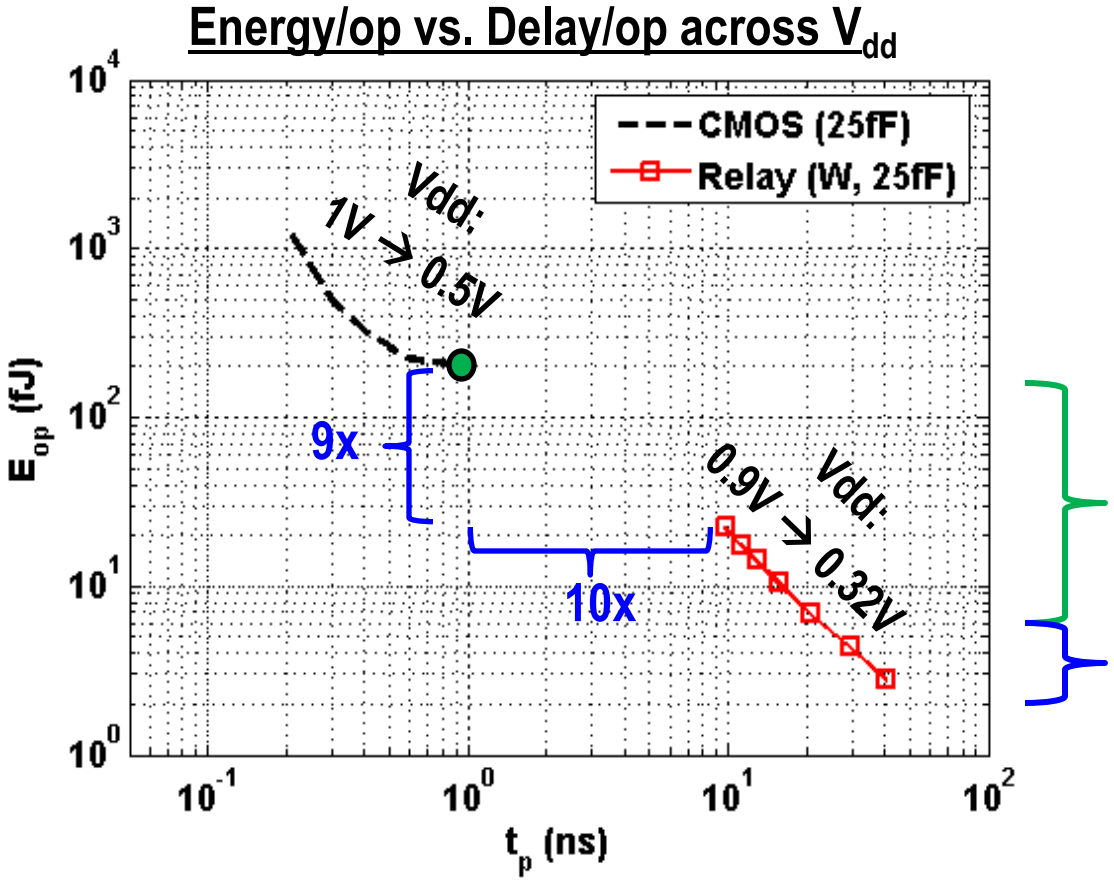
F. Chen *et al*., "Integrated Circuit Design with NEM Relays," *ICCAD 2008*

Example: 32-bit NEMS Adder



- Ripple carry configuration
  - Cascade full adder cells to create larger complex gate
- Stack 32 NEMS, but still single mechanical delay

Scaled NEMS vs. CMOS Adders



- Compare *vs*. Sklansky CMOS adder*
  - 90nm technology
- 30x less capacitance
  - Lower device C_g, C_d
  - Fewer devices
- 2.4x lower V_{dd}
  - No leakage energy

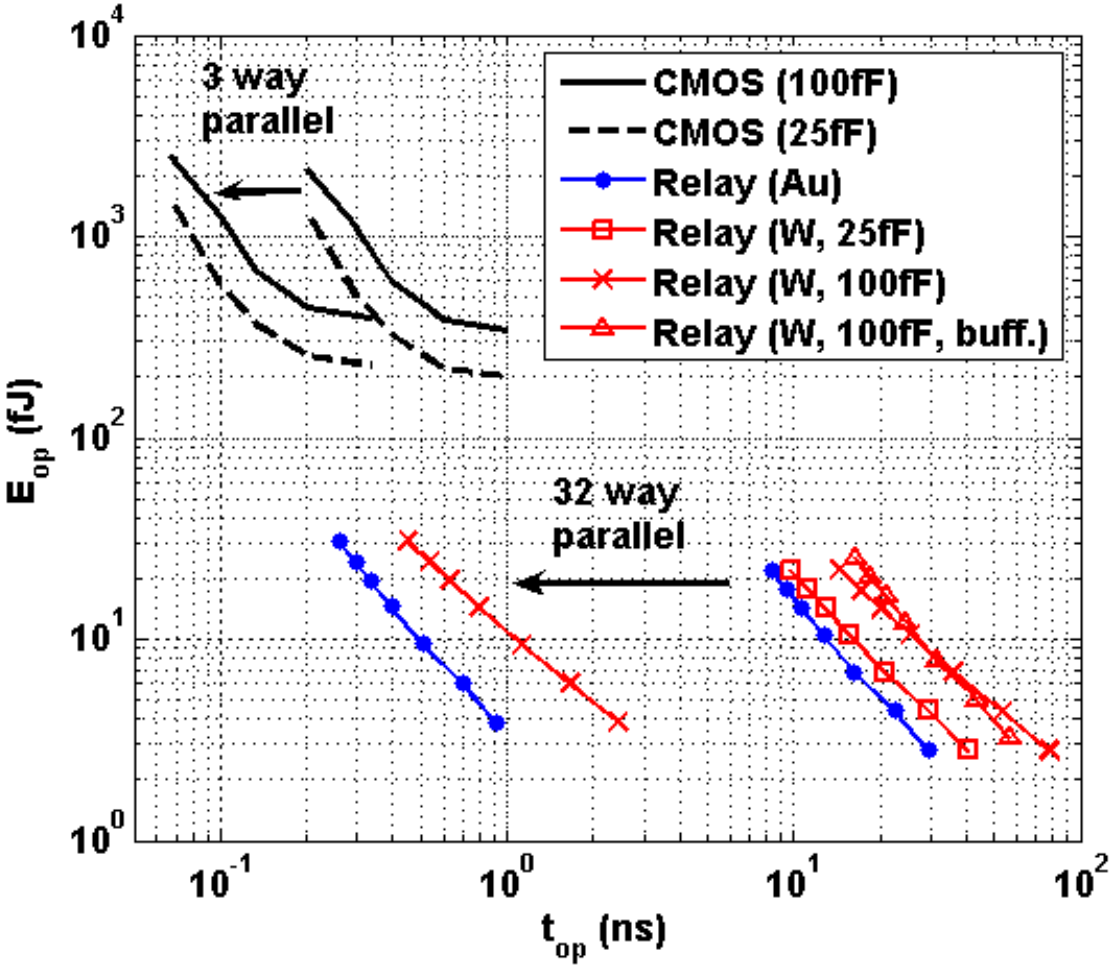
- For similar area: >9x lower E/op, >10x greater delay

F. Chen *et al*., "Integrated Circuit Design with NEM Relays," *ICCAD 2008*

*D. Patil et. al., "Robust Energy-Efficient Adder Topologies," in Proc. 18th IEEE Symp. on Computer Arithmetic (ARITH'07).

Parallelism: Trade Area for Performance

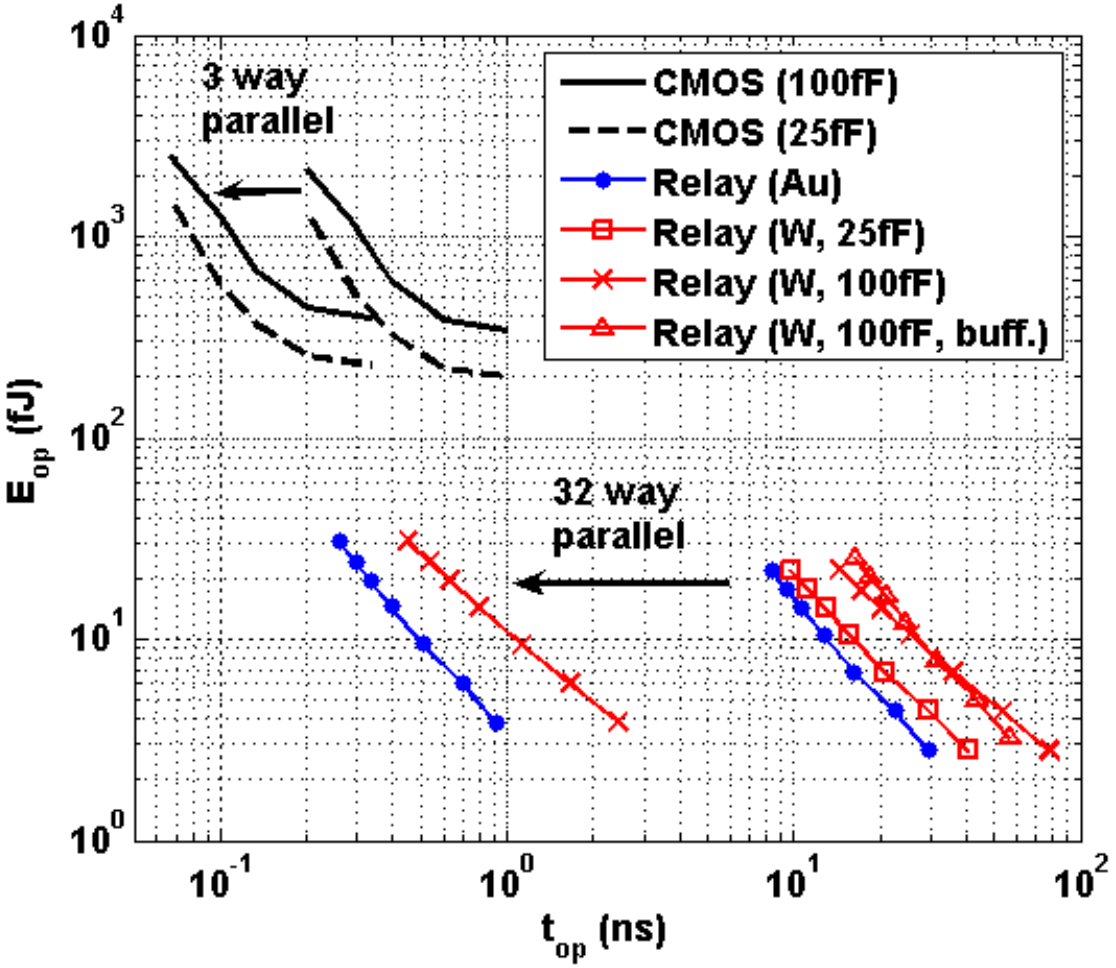
Energy/op vs. Delay/op across V_{dd} & C_L



- Can extend energy benefit up to GOP/s throughput
  - As long as parallelism is available
- Area overhead bounded
  - CMOS needs to be parallelized at some point too

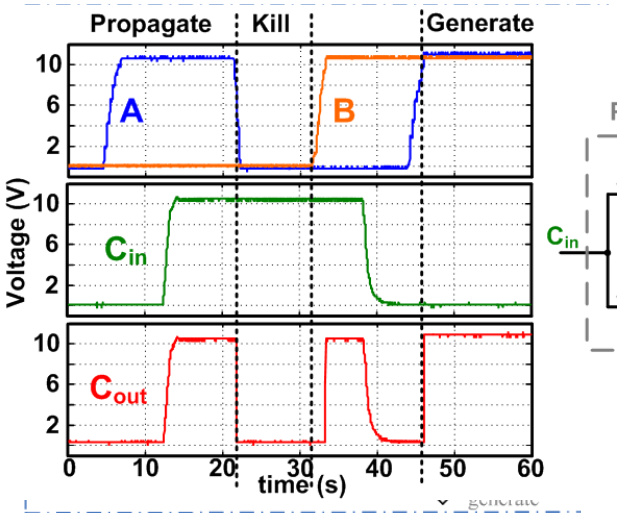
Contact Resistance

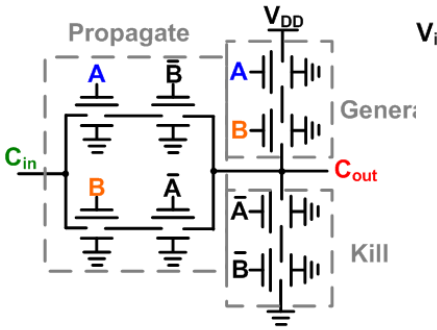
Energy/op vs. Delay/op across V_{dd} & C_L

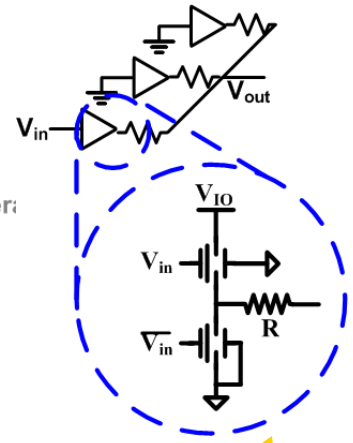


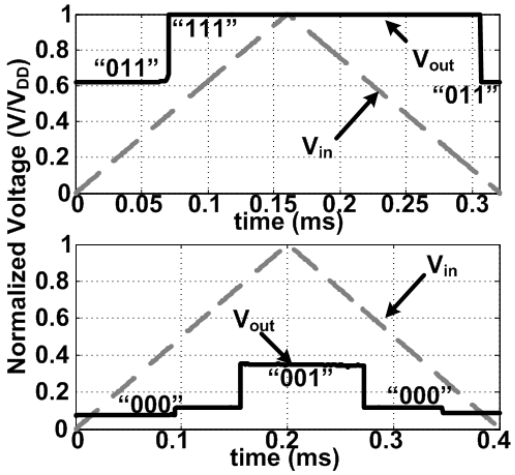
- Low contact R not critical
- Good news for reliability…
- Relays with W contacts lived through 65 B cycles

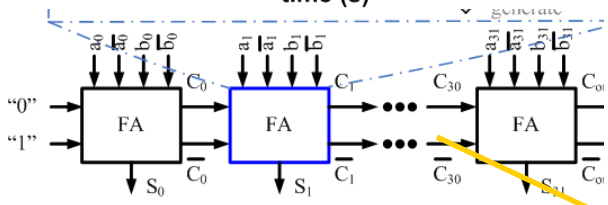
NEM Relay-based Circuits: First Test-chip

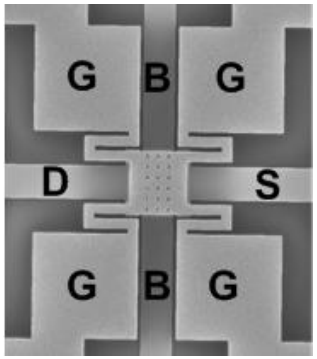


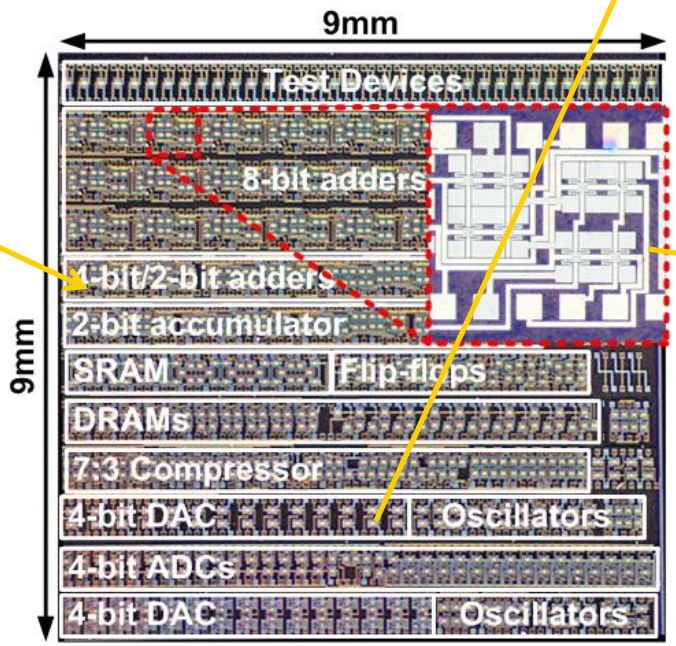


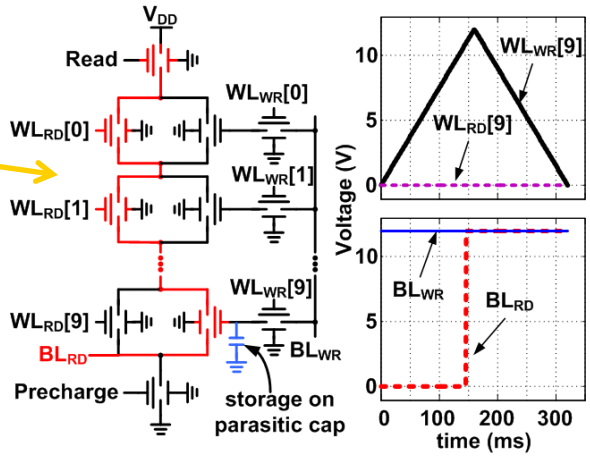








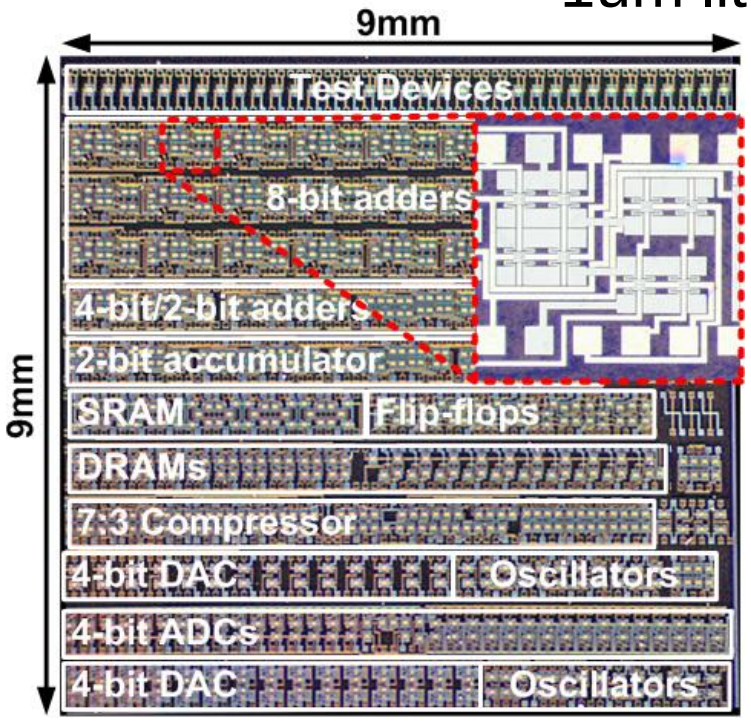




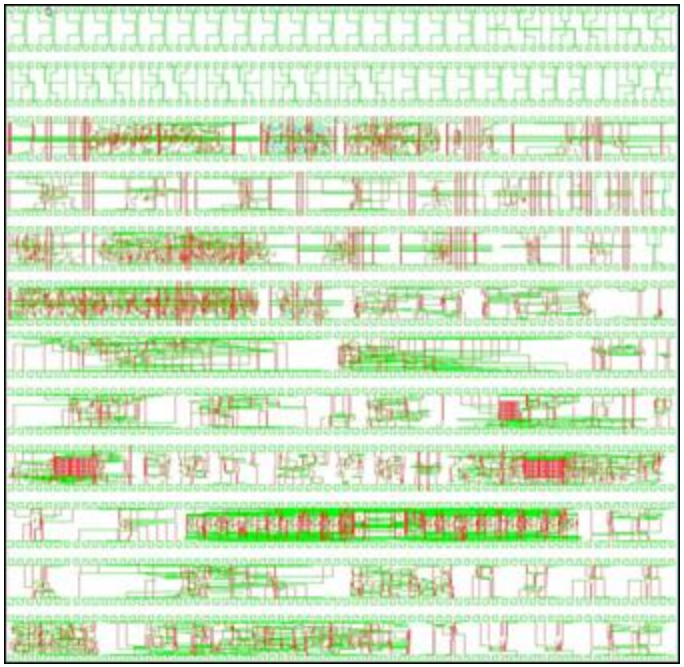
F. Chen *et al.*, "Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications," *ISSCC 2010*.

NEM Relay Scaling – Next Design

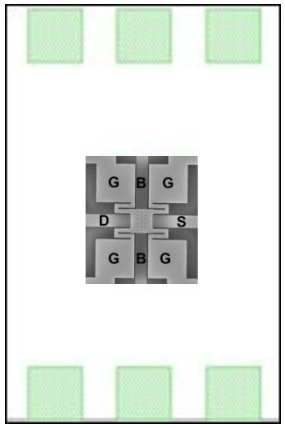
1um litho

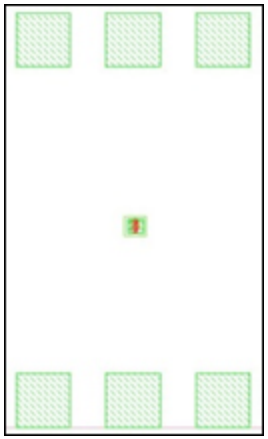


0.25um litho



NEM relay size
120um x 150um





Scaled NEM relay
20um x 20um

Conclusions

- NEMS unique features enable energy scaling beyond-CMOS
  - Nearly ideal I_{on}/I_{off}
  - Switching delay largely independent of electrical τ
  - Need to adapt circuit design style
- Reliability improving
  - Circuit level insights critical (contact R)
  - Demonstrated simple circuits
  - Can start thinking about building more complex systems
- Potentially order of magnitude lower E/op than CMOS
  - Next steps: scaling and improved device design, testing larger digital blocks

Acknowledgements

- Circuit design
  - Fred Chen, Hossein Fariborzi
  - Matthew Spencer, Abhinav Gupta
  - Cheng Wang, Kevin Dwan
- Device design
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  - FCRP (C2S2, MSD)
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